INTEGRATED CIRCUITS

Advanced Low Voltage CMOS Logic

Data Handbook IC24
1999

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Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

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In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

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All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Advanced Low Voltage CMOS Logic Data Handbook

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DEFINITIONS

Data Sheet Identification	Product Status	Definition (Note)
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.
Short-form specification	—	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such improper use or sale.

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NOTE: Always check with your local Philips Semiconductors Sales Office to be certain that you have the latest data sheet(s) before completing a design.

Preface

Advanced Low Voltage CMOS Logic

Philips Semiconductors Logic Products Group thanks you for your continued interest in our Advanced CMOS product lines. This handbook contains specifications for many new high performance, low power products from Philips.

This handbook replaces and updates the 1996 Low Voltage CMOS Logic Data Handbook (IC24). Specifications for a wide range of high performance product families in this handbook include the 3V CMOS families such as the LV, the 5V tolerant LVC, and the very high speed bus interface ALVC devices.

The products utilize Philips most advanced CMOS technologies which enable very high speed, high drive capabilities and excellent noise immunity all combined in a wide range of space saving surface mounted packages.

Other support material available from your local distributor, sales office, or sales representative includes a comprehensive SPICE I/O Model Manual and IBIS Models on newer part types.

On-Line support includes a Fax-On-Demand toll free number 1–800–282–2000 in North America, and a Web site for Logic Products at "www.philipslogic.com".

Our ongoing goal is to become your first choice for Logic Products.

August 1998

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General Information

Advanced Low Voltage CMOS Logic

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IC24: ADVANCED LOW VOLTAGE CMOS LOGIC

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Section 3 – Low Voltage CMOS Devices (LVC) (Continued)

Section 4 – Low Voltage CMOS 16-bit Devices (LVC16)

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Appendix A

Philips Low Voltage Logic Families DESIGNERS GUIDE

This databook provides device data of Philips Semiconductors Low Voltage CMOS logic families. The following families were introduced for the low voltage market: LV, LVC, and ALVC. All families are complete new designs for 3.3V or sub-3V operations.

ABOUT THE LVC (LOW VOLTAGE CMOS)

The LVC family has become a logic industry standard for 3.3V applications both in the telecom and EDP market segment. Manufactured in a CMOS process it offers direct interface with LVTTTL levels. It is specified and guaranteed for industrial operating temperatures. The LVCs provide 4.5 – 5ns speeds and 24mA drive capability while operating at 3V with very low static and dynamic power consumption. The family supports live insertion. Its 5V tolerance capabilities makes it extremely attractive for mixed 5V/3V systems. The LVC devices offer both non-bus hold and bus hold options with or without damping resistor features. With bus hold, the need for pull-up and pull-down resistors for floating inputs is eliminated. Series damping resistors help prevent signal undershoots and overshoots. The family product offering ranges from standard gates, octals to complex 16-bit bus interface functions used for buffering, multiplexing and interfacing in mixed 5V/3V systems. The broad portfolio and feature set of the LVC family provide designers with the flexibility and reliability necessary to minimize manufacturing costs, eliminate floating inputs and design "worry-free" systems.

ABOUT THE ALVC (ADVANCED LOW VOLTAGE CMOS)

One of the fastest low voltage CMOS family, the ALVC family is widely used in supporting memory interfacing and multiplexing. ALVC offers direct interface with LVTTTL levels. Industrial operating temperature is from –40°C to +85°C. ALVC features flow-through standard pin-out architecture and low inductance, noise and ground bounce properties. ALVC devices offer both non-bus hold and bus hold operation, with or without "damping resistor" features, indicating a large variety of bus interface functions. With bus hold, the need for pull-up or pull-down resistors for floating inputs is eliminated. Series damping resistors help prevent signal undershoots and overshoots. ALVC devices are widely used in memory buffering, multiplexing and interfacing to 3.3V synchronous DRAMs, demonstrating typical propagation delays of less than 3ns. With a standard 24mA drive capability at 3.3V and static power consumption of 40µ or less, ALVC is ideal for all types of low-voltage applications. Philips ALVC supports products that fulfill the PC100 logic interface requirements necessary to support next generation PC systems.

In Table 1, the nomenclature for the LVC and the ALVC families is summarized.

Table 1. Guidelines of the Philips nomenclature for the LVC and the ALVC families

OPTIONS	COMMENT	PHILIPS LVC	PHILIPS ALVC
Non-bus hold	In 8-bits In 16-bits	74LVCxxx 74LVC16XXX	– 74ALVC16xxx
Bus hold	In 8-bits	74LVCHxxx	–
Bus hold	In 16-bits	74LVCH16XXX	74ALVCH16xxx
Damping Resistor	In 8-bits In 16-bits	74LVC2xxx 74LVC162XXX	– 74ALVC162xxx
Bus hold + Damping Resistor	In 16-bits	74LVCH162XXX	74ALVCH162xxx

ORDERING INFORMATION

All datasheets have an ordering information table which is for Philips Internal Use Only.

All customers worldwide should use the **part name** as the **ordering part number**.

Only exception: For **North American Distribution Customers**, please use the **Disti-Price Book** part name.

FEATURE SUMMARY

In table 2, the major characteristics of the three low voltage families are summarized:

Table 2. Feature Summary

KEY PARAMETERS	LV	LVC	ALVC
Minimum V_{CC} V	1.0	1.2	1.2
Maximum V_{CC} V	5.5	3.6	3.6
Output current mA	±6	±24	±24
Quiescent current µA	10	10[2]	40
'244 delay times			
T_{PD} typ. ns	9	3.5	1.9
T_{PD} max. ns	14	5.8	3.0
Maximum ground bounce V	0.4	0.8	0.7
FEATURES			
Full CMOS	✓	✓	✓
Drive capability:			
135Ω	✓		
50Ω		✓	✓
Feature size:			
2.0 µm	✓		
0.7 µm		✓	
0.45 µm			✓
Corner supply pins	✓	✓	
Multiple V_{CC}/GND pins		✓	
TTL level input	✓	✓	✓
TTL level output	✓	✓	✓
5V Input capability		✓	✓[1]
5V Output capability		✓	
Live insertion		✓	
Input bus hold option		✓	
Damping resistor option		✓	
Packages:			
DIL	✓		
SO	✓	✓	
SSOP	✓	✓	✓
TSSOP	✓	✓	✓

NOTES:
1. For control pins only and for non-bus hold types; For bus hold input and output pins: $V_{IN\,max} = V_{CC} + 0.5V$.
2. 20 µA for 16–bits.

DESIGNERS' GUIDE

Electrical Characteristics

The following pages cover a number of electrical characteristics of the LVC and ALVC families. The parts chosen to be plotted are the 74LVC245A, 74LVC16245A, and the 74ALVC16245.

I. Propagation Delay versus Temperature

The effect of temperature on the propagation delay are plotted. The measurements were done under the following conditions:

- C_L = 50pF
- One output switching
- V_{CC} in the range of 2.7V – 3.6V

II. Propagation Delay versus C_L

The effect of the output load on the propagation delay are plotted for different switching conditions (i.e. one output switching or multiple outputs switching). The measurements were done under the following conditions:

- Temperature = 25°C
- V_{CC} = 3.3V
- R_L = 500Ω

III. Supply Current versus Frequency

The supply current is plotted for a frequency range of 10MHz – 100MHz. The results are based on the following conditions:

- C_L = 50pF
- All outputs switching
- Temperature = 25°C
- V_{CC} = 3.3V
- R_L = 500Ω

IV. V_{OLP}, V_{OLV}, V_{OHV}, V_{OHV} versus Load Capacitance

Ground bounce versus load capacitance

V. V_{OL} versus I_{OL}

The output low voltage is plotted versus the output low current.

VI. V_{OH} versus I_{OH}

The output high voltage is plotted versus the output high current.

VII. Pin Skew

The propagation delay skew is presented for all three devices.

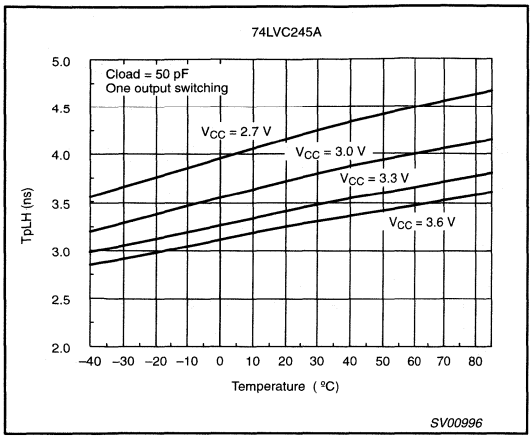
VIII. I_{INP} versus V_{INP}

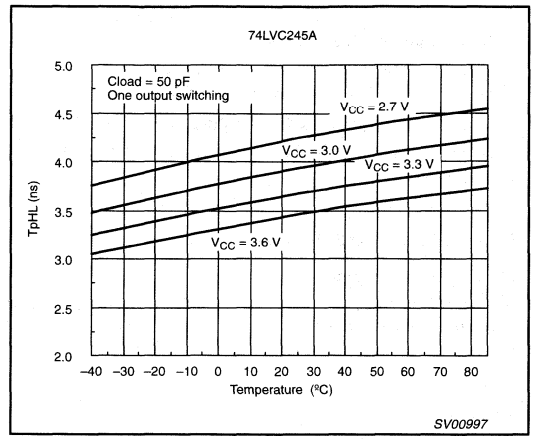
The input current is plotted versus the input voltage.

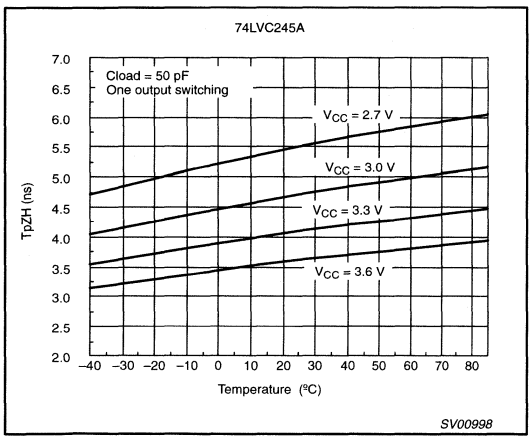
IX. I_{CC} versus V_{INP}

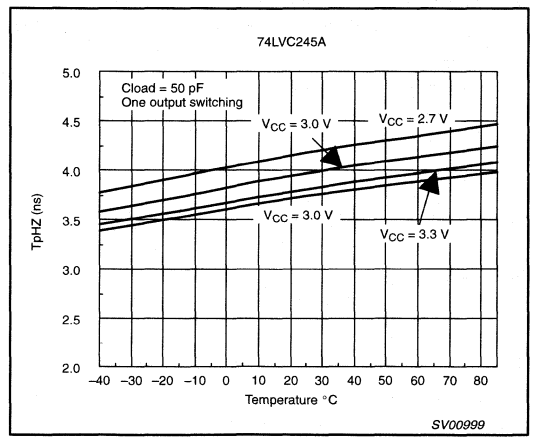
The input leakage current is plotted versus the input voltage.

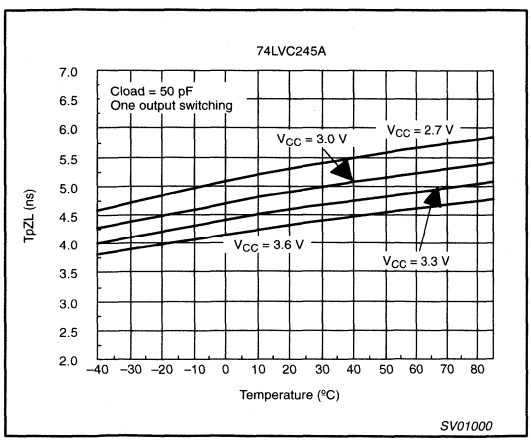
I. PROPAGATION DELAY VERSUS TEMPERATURE

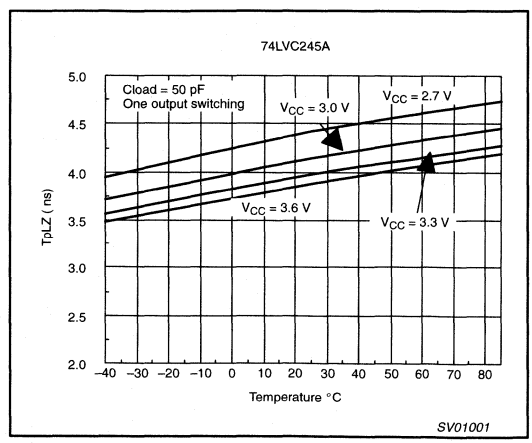


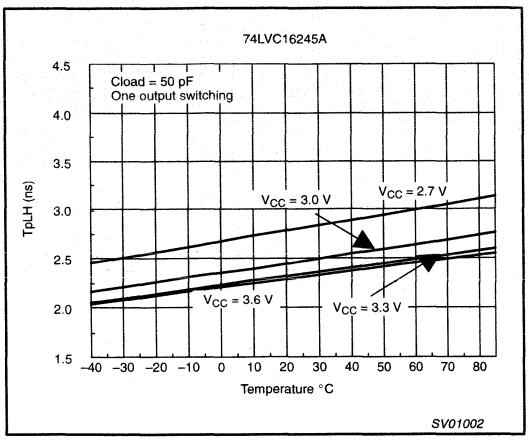








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One output switching
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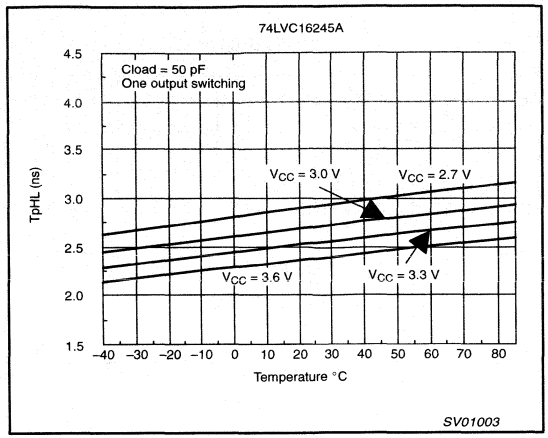
VCC = 3.0 V
VCC = 2.7 V
VCC = 3.6 V
VCC = 3.3 V
Temperature °C
SV01002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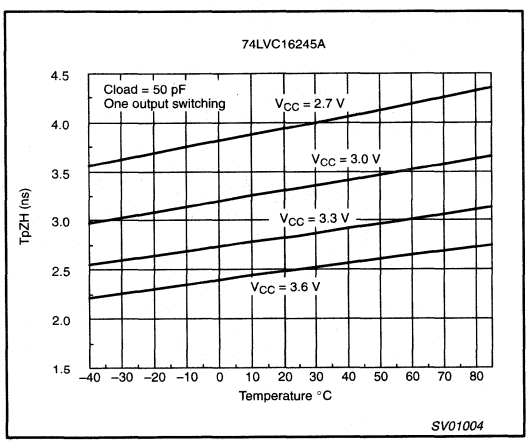
VCC = 2.7 V
VCC = 3.6 V
VCC = 3.3 V
Temperature °C
SV01003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Cload = 50 pF
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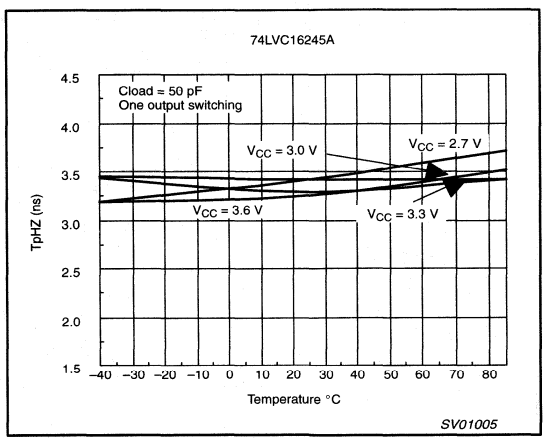
VCC = 3.0 V
VCC = 3.3 V
VCC = 3.6 V
Temperature °C
SV01004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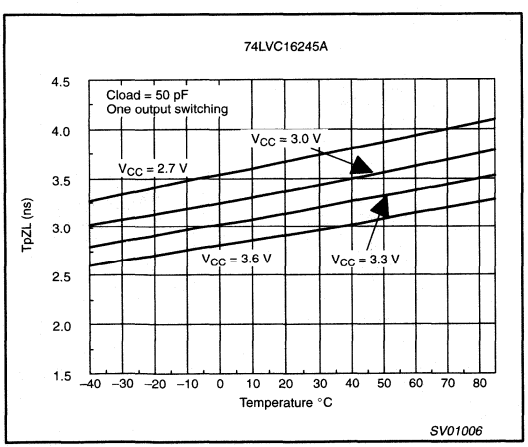
VCC = 3.6 V
VCC = 3.3 V
Temperature °C
SV01005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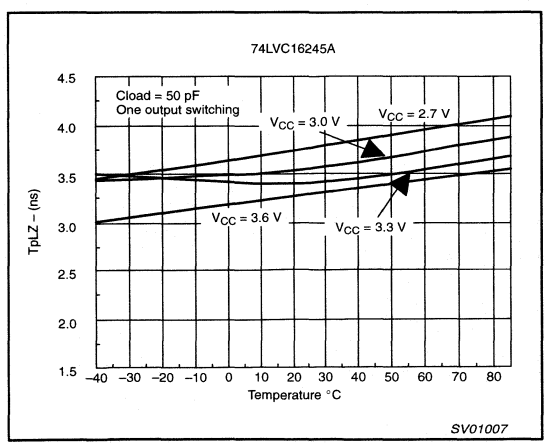
VCC = 2.7 V
VCC = 3.6 V
VCC = 3.3 V
Temperature °C
SV01006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Cload = 50 pF
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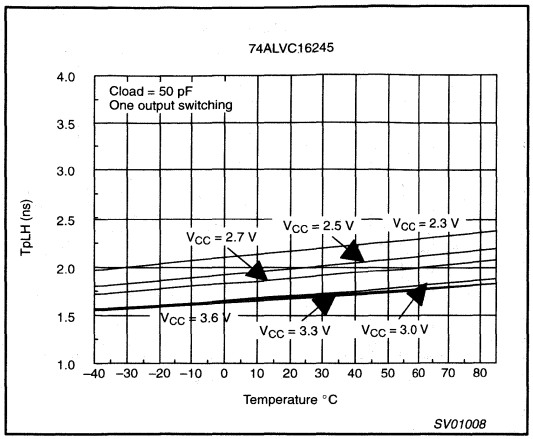
VCC = 2.7 V
VCC = 3.6 V
VCC = 3.3 V
Temperature °C
SV01007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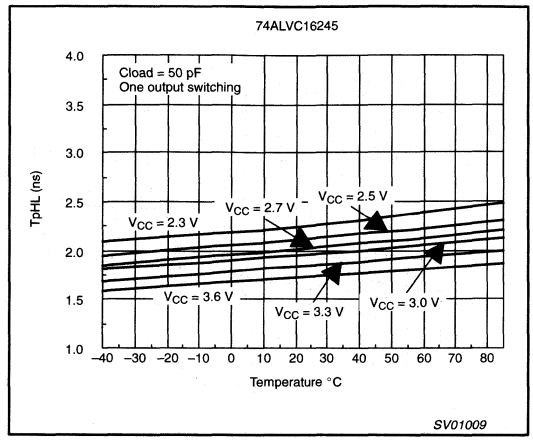
VCC = 3.3 V
VCC = 3.0 V
Temperature °C
SV01008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VCC = 2.3 V
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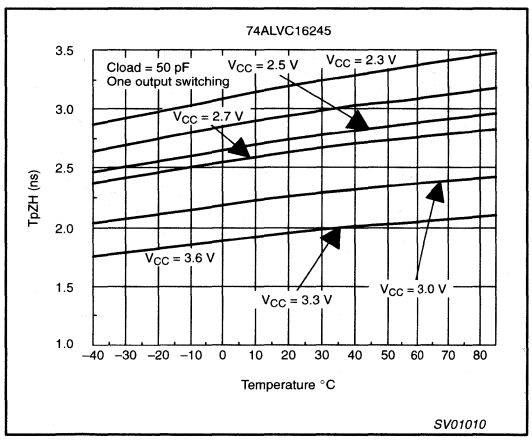
VCC = 3.3 V
VCC = 3.0 V
Temperature °C
SV01009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One output switching
TpZH (ns)
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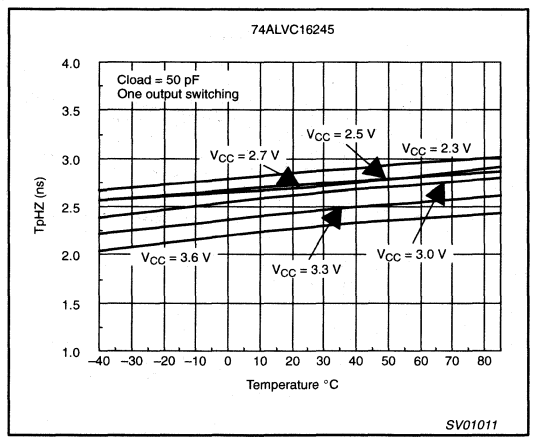
VCC = 2.3 V
VCC = 2.7 V
VCC = 3.6 V
VCC = 3.3 V
VCC = 3.0 V
Temperature °C
SV01010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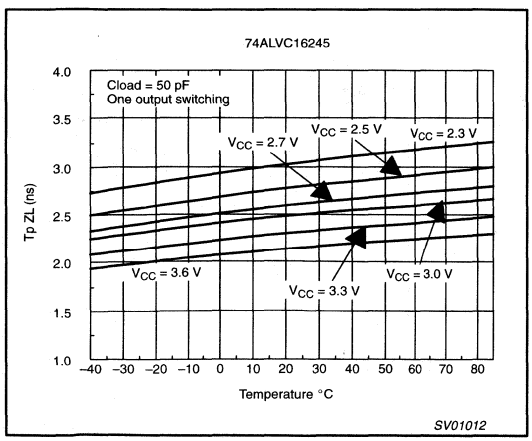
Cload = 50 pF
One output switching
TpHZ (ns)
VCC = 2.5 V
VCC = 2.7 V
VCC = 2.3 V
VCC = 3.6 V
VCC = 3.3 V
VCC = 3.0 V
Temperature °C
SV01011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Cload = 50 pF
One output switching
Tp ZL (ns)
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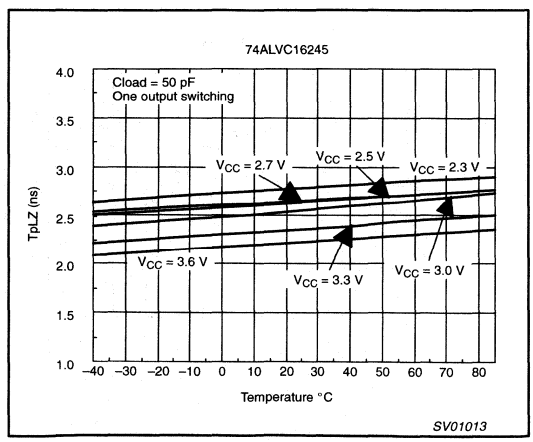
VCC = 2.3 V
VCC = 3.6 V
VCC = 3.3 V
VCC = 3.0 V
Temperature °C
SV01012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Cload = 50 pF
One output switching
TpLZ (ns)
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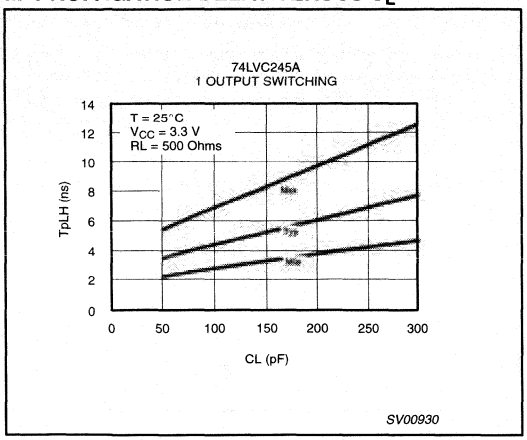
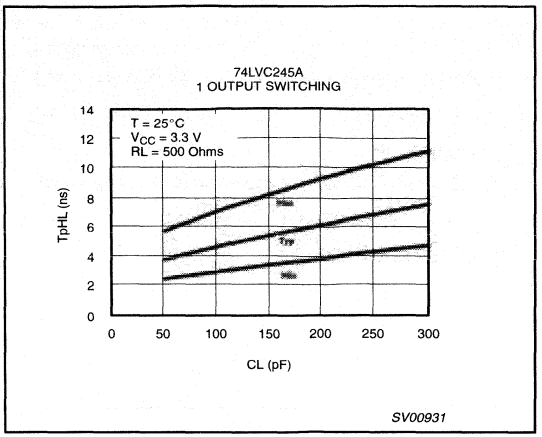
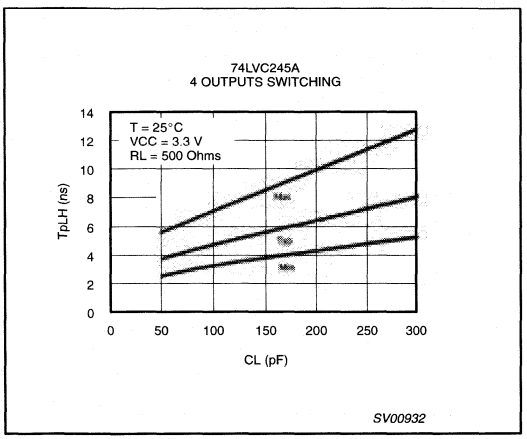
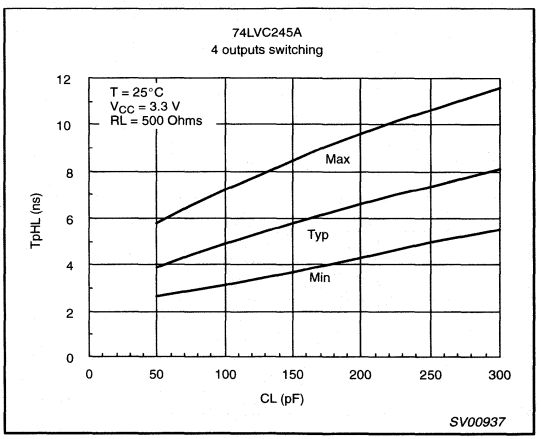
VCC = 2.5 V
VCC = 2.3 V
VCC = 3.6 V
VCC = 3.3 V
VCC = 3.0 V
Temperature °C
SV01013

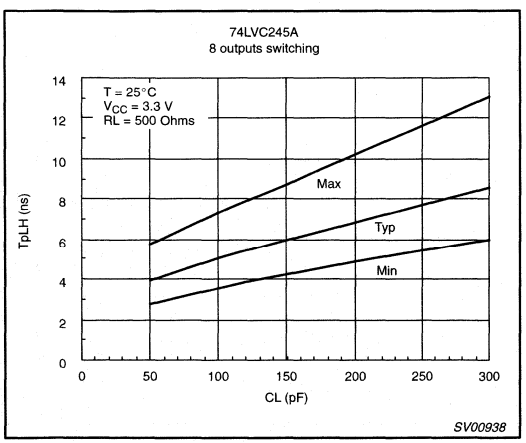
II. PROPAGATION DELAY VERSUS C_L

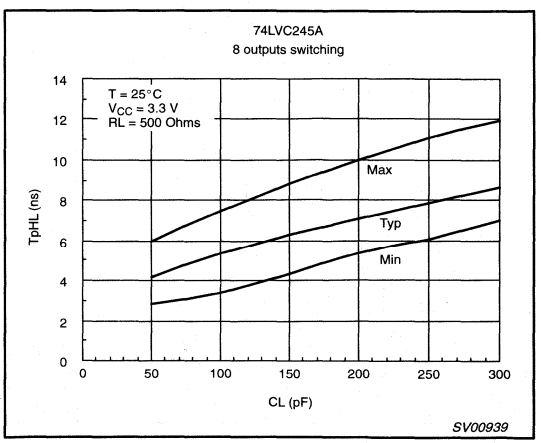


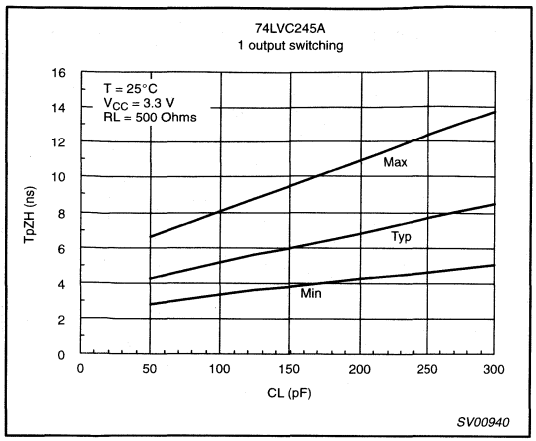


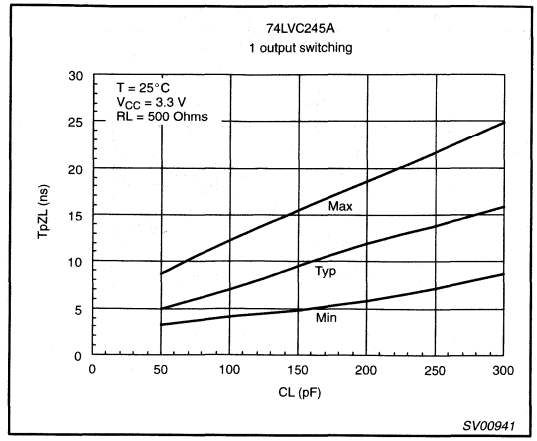


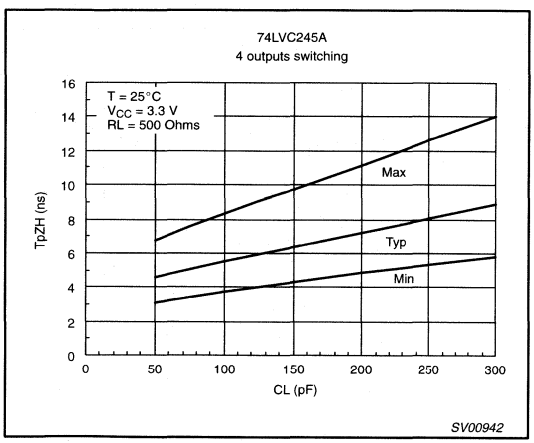


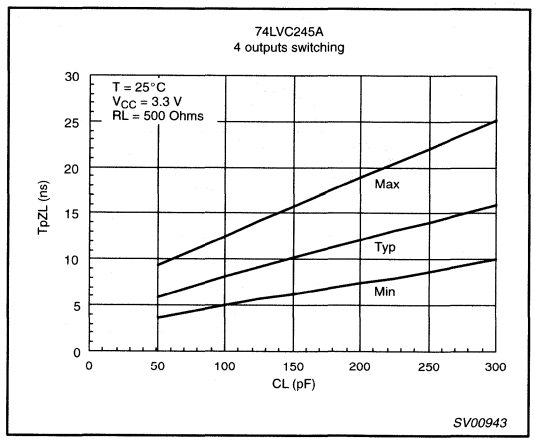


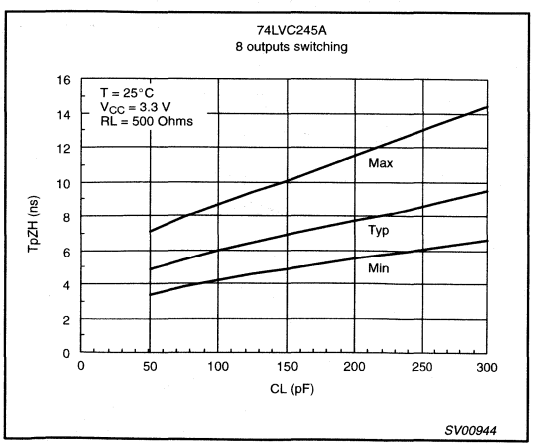


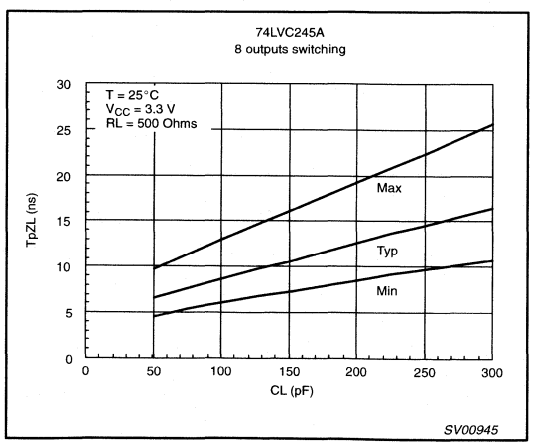

74LVC245A
1 output switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZH (ns)
CL (pF)
SV00940

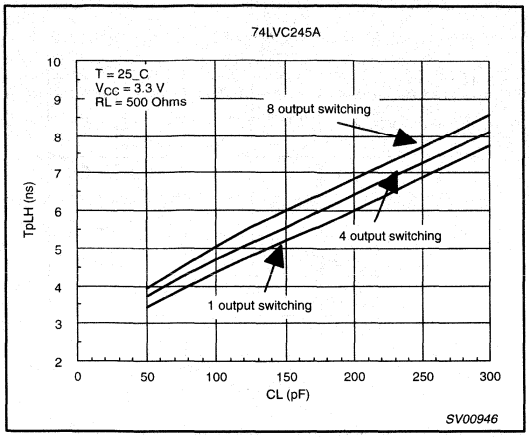

74LVC245A
1 output switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00941

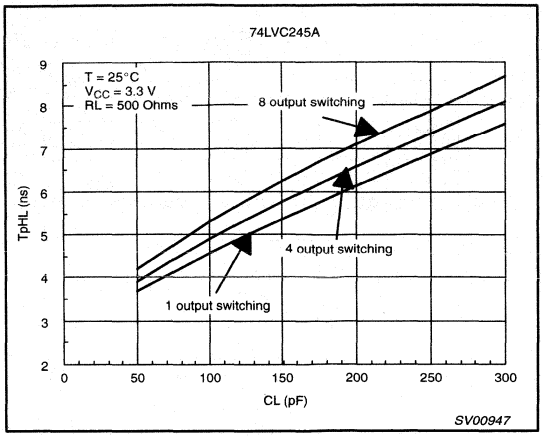

74LVC245A
4 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZH (ns)
CL (pF)
SV00942

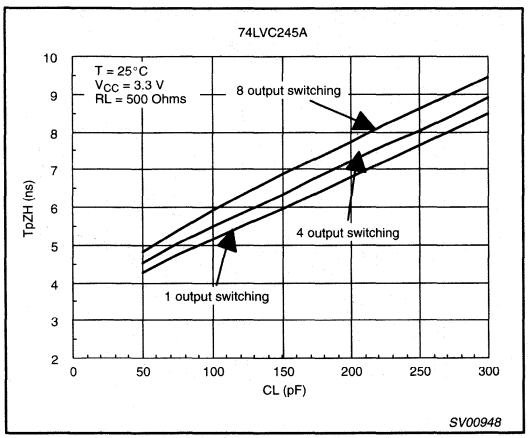

74LVC245A
4 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00943

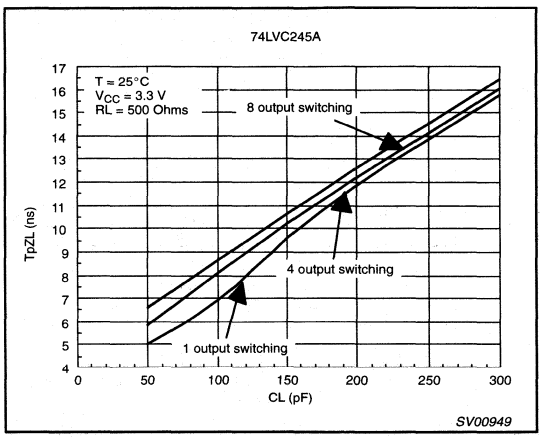

74LVC245A
8 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZH (ns)
CL (pF)
SV00944

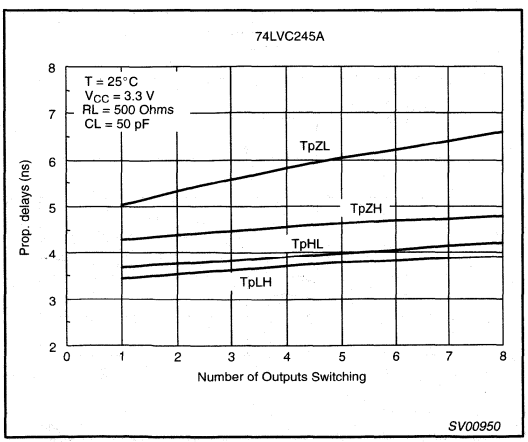

74LVC245A
8 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00945

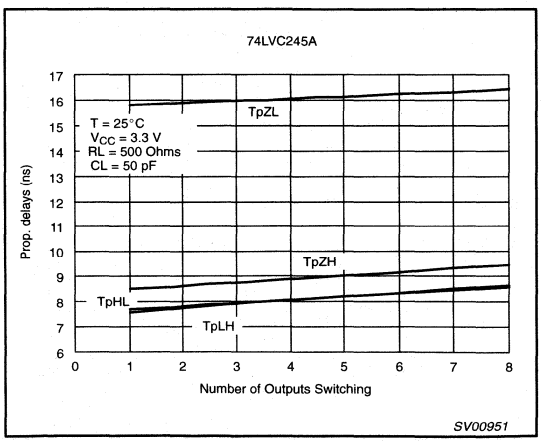

74LVC245A
T = 25_C
VCC = 3.3 V
RL = 500 Ohms
8 output switching
4 output switching
1 output switching
TpLH (ns)
CL (pF)
SV00946

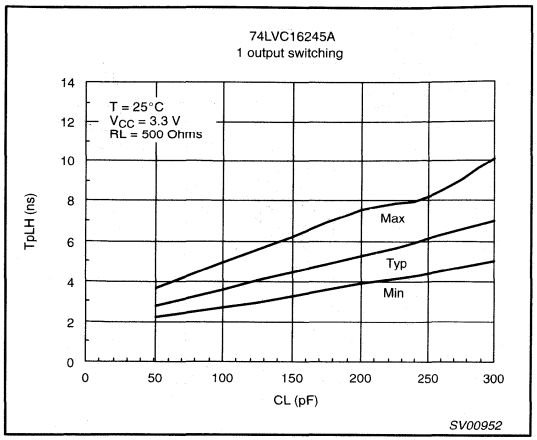

74LVC245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
8 output switching
4 output switching
1 output switching
TpHL (ns)
CL (pF)
SV00947

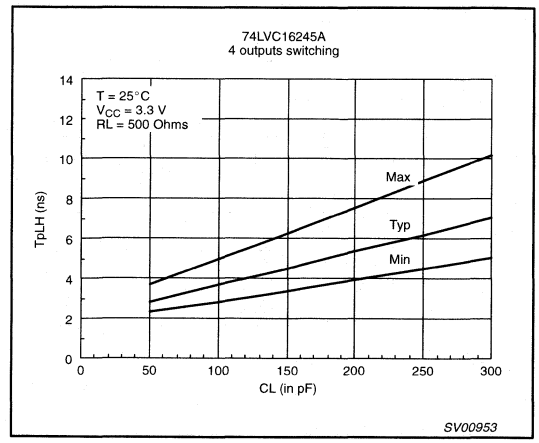

74LVC245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
8 output switching
4 output switching
1 output switching
TpZH (ns)
CL (pF)
SV00948

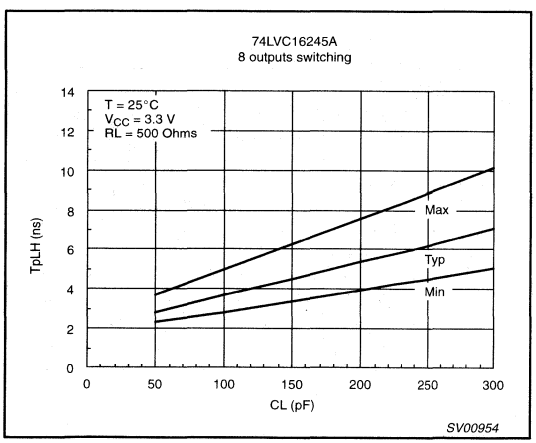

74LVC245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
8 output switching
4 output switching
1 output switching
TpZL (ns)
CL (pF)
SV00949

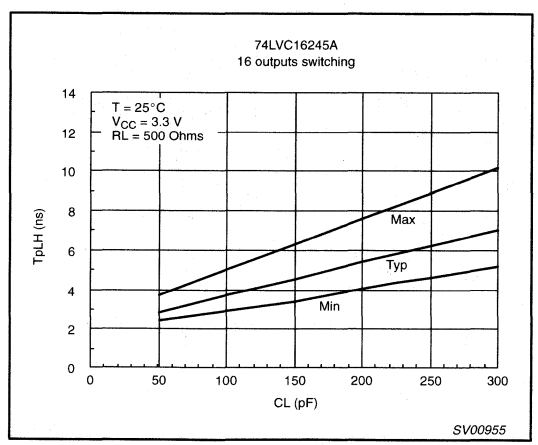

74LVC245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
CL = 50 pF
TpZL
TpZH
TpHL
TpLH
Prop. delays (ns)
Number of Outputs Switching
SV00950

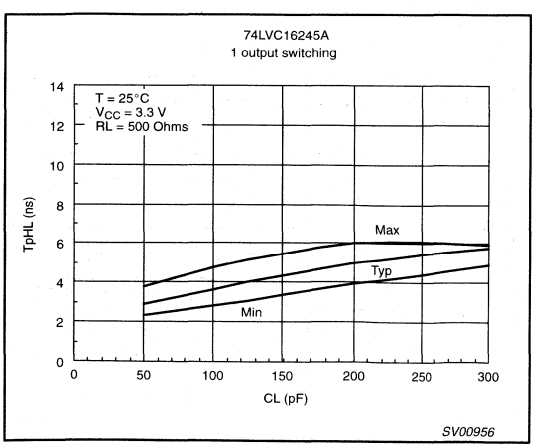

74LVC245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
CL = 50 pF
TpZL
TpZH
TpHL
TpLH
Prop. delays (ns)
Number of Outputs Switching
SV00951

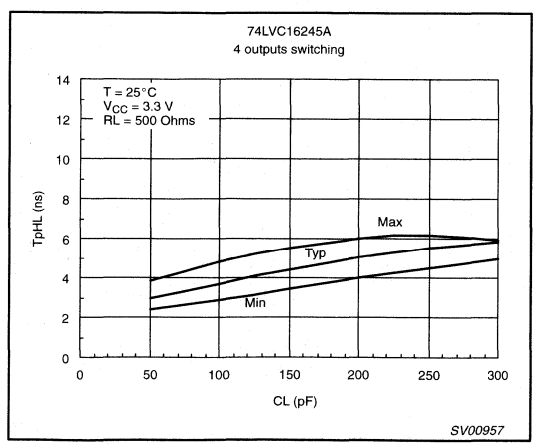

74LVC16245A
1 output switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpLH (ns)
CL (pF)
Max
Typ
Min
SV00952

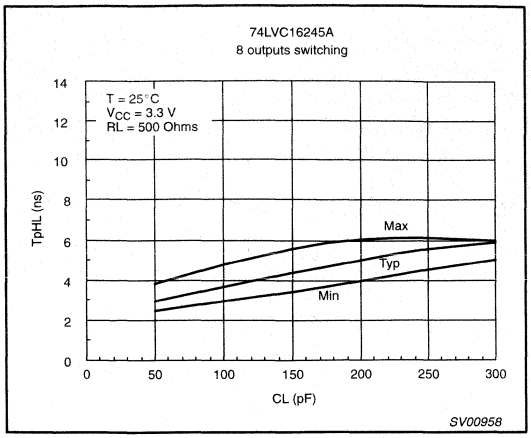

74LVC16245A
4 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpLH (ns)
CL (in pF)
Max
Typ
Min
SV00953

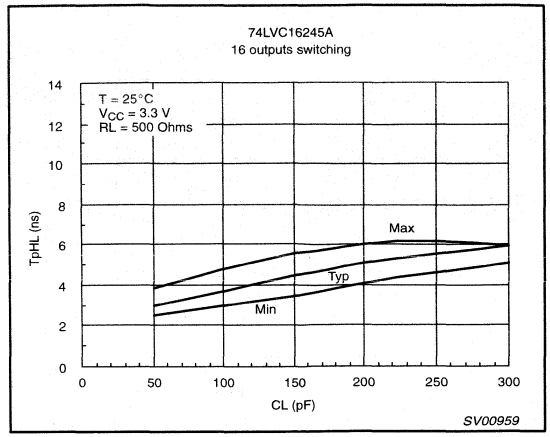

74LVC16245A
8 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpLH (ns)
CL (pF)
Max
Typ
Min
SV00954

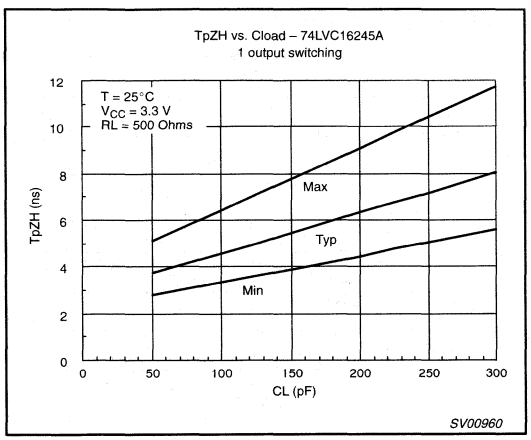

74LVC16245A
16 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpLH (ns)
CL (pF)
Max
Typ
Min
SV00955

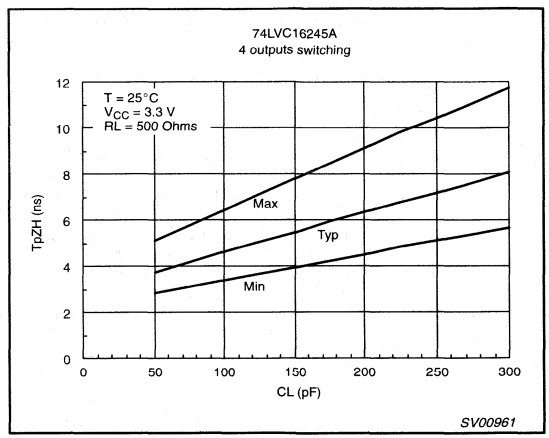

74LVC16245A
1 output switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpHL (ns)
CL (pF)
Max
Typ
Min
SV00956

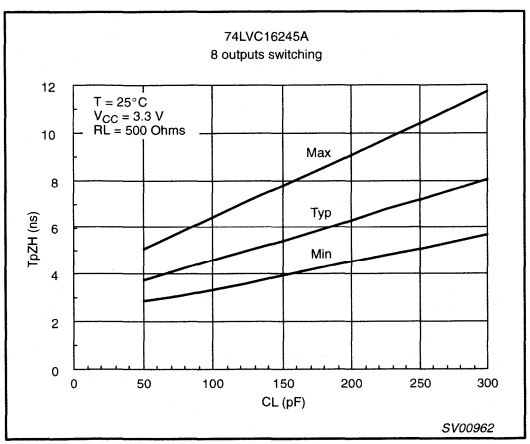

74LVC16245A
4 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpHL (ns)
CL (pF)
Max
Typ
Min
SV00957

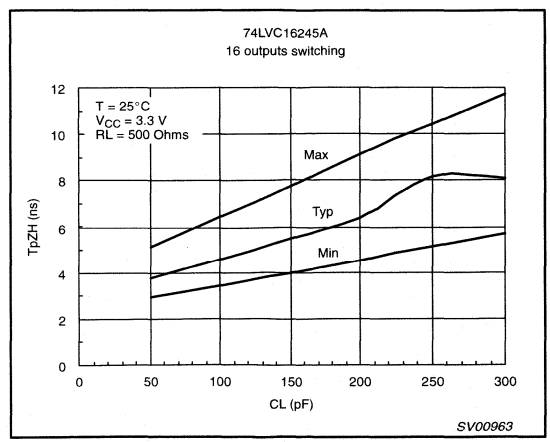

74LVC16245A
8 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpHL (ns)
CL (pF)
Max
Typ
Min
SV00958

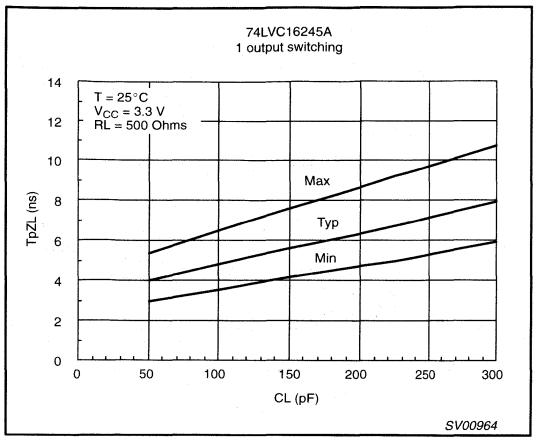

74LVC16245A
16 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpHL (ns)
CL (pF)
Max
Typ
Min
SV00959

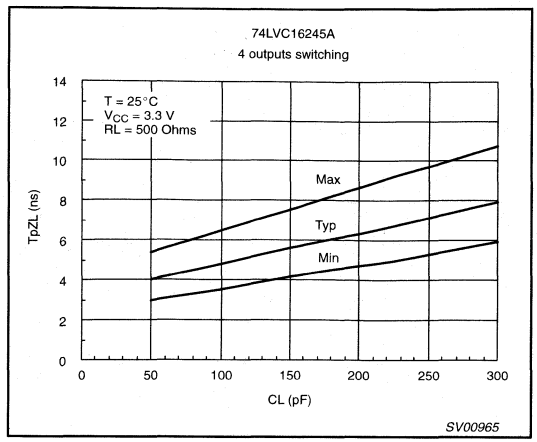

TpZH vs. Cload – 74LVC16245A
1 output switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpZH (ns)
CL (pF)
Max
Typ
Min
SV00960

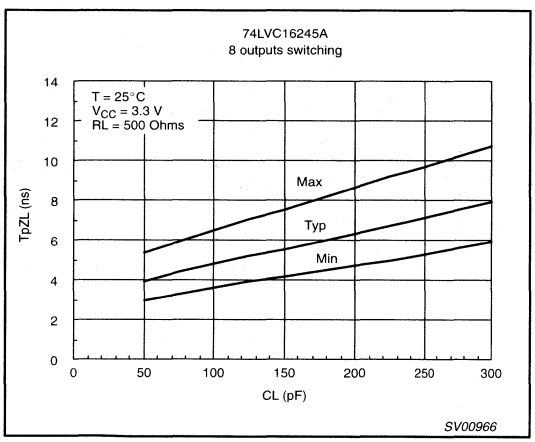

74LVC16245A
4 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpZH (ns)
CL (pF)
Max
Typ
Min
SV00961

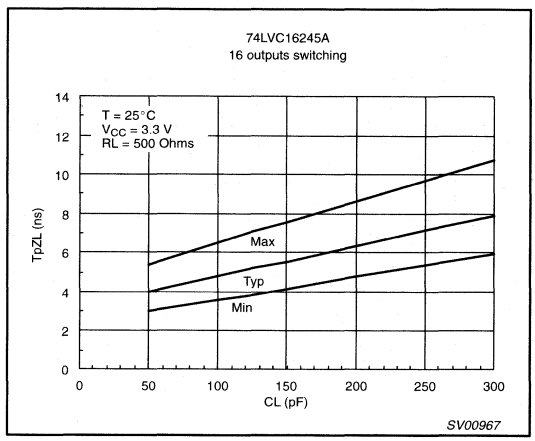

74LVC16245A
8 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpZH (ns)
CL (pF)
Max
Typ
Min
SV00962

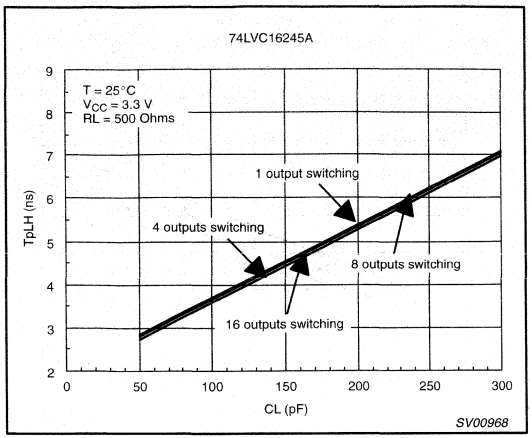

74LVC16245A
16 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
TpZH (ns)
CL (pF)
Max
Typ
Min
SV00963

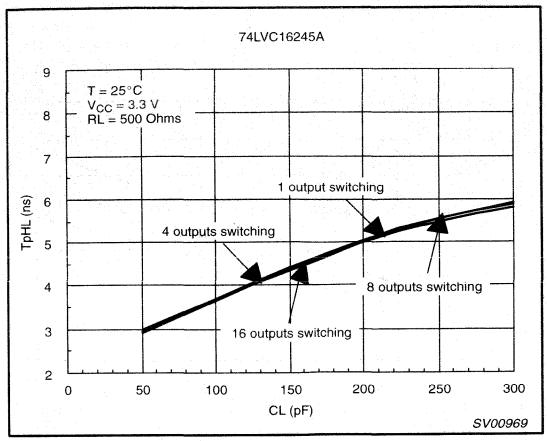

74LVC16245A
1 output switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00964

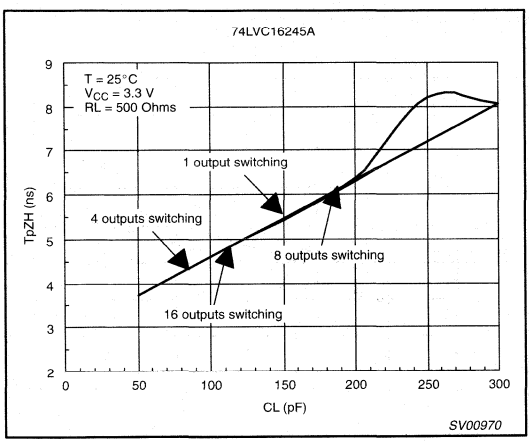

74LVC16245A
4 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00965

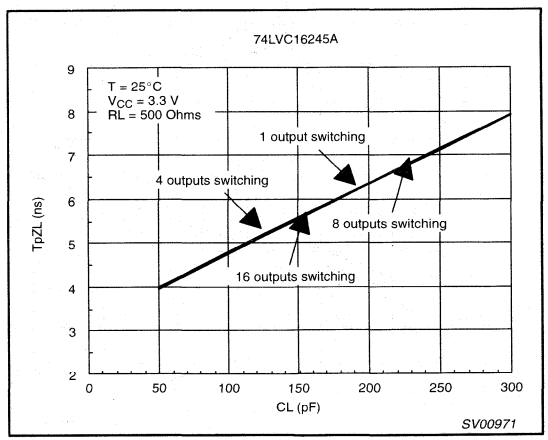

74LVC16245A
8 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00966

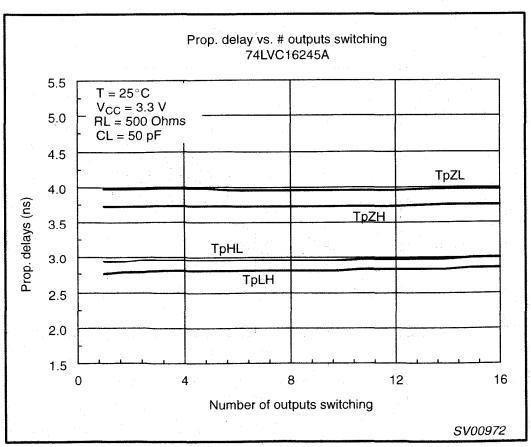

74LVC16245A
16 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00967

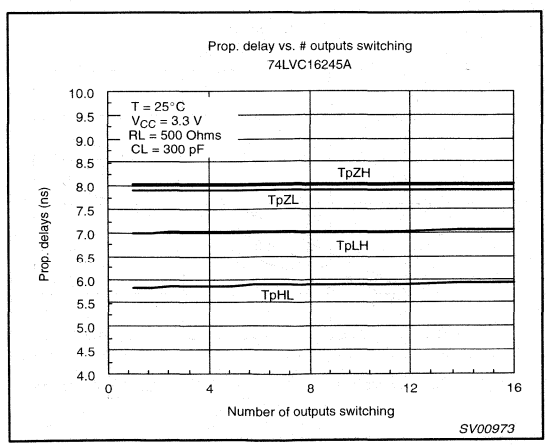

74LVC16245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
1 output switching
4 outputs switching
8 outputs switching
16 outputs switching
TpLH (ns)
CL (pF)
SV00968

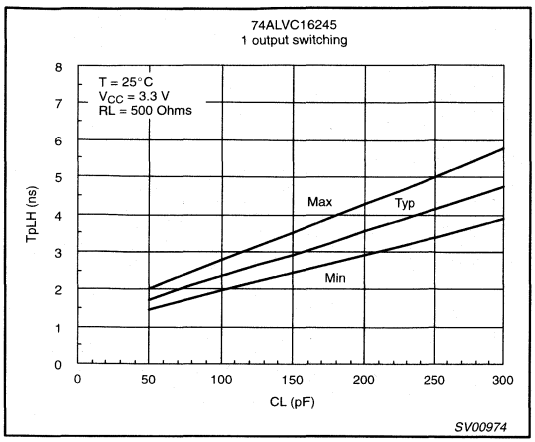

74LVC16245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
1 output switching
4 outputs switching
8 outputs switching
16 outputs switching
TpHL (ns)
CL (pF)
SV00969

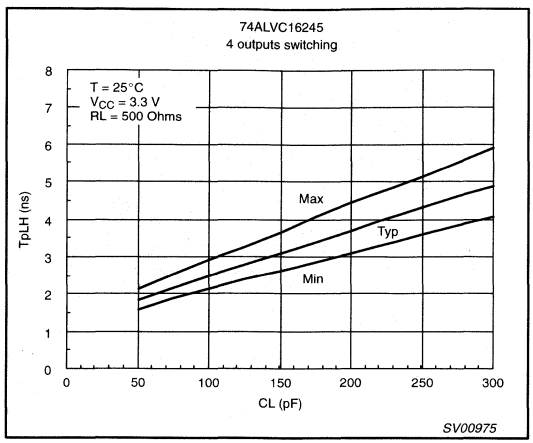

74LVC16245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
1 output switching
4 outputs switching
8 outputs switching
16 outputs switching
TpZH (ns)
CL (pF)
SV00970

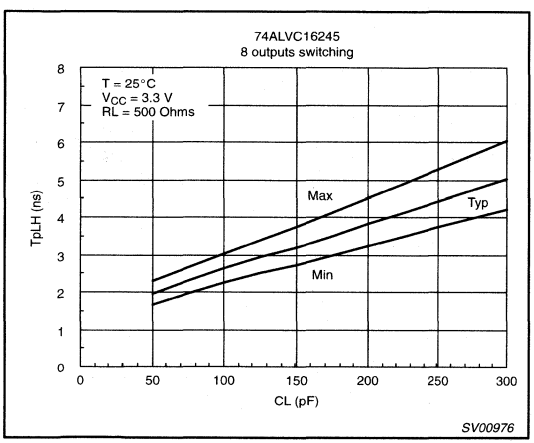

74LVC16245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
1 output switching
4 outputs switching
8 outputs switching
16 outputs switching
TpZL (ns)
CL (pF)
SV00971

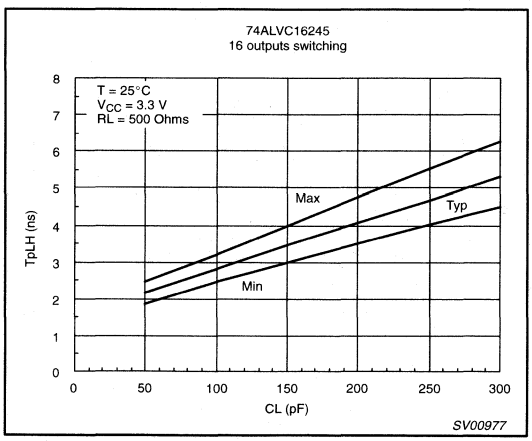

Prop. delay vs. # outputs switching
74LVC16245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
CL = 50 pF
TpZL
TpZH
TpHL
TpLH
Prop. delays (ns)
Number of outputs switching
SV00972

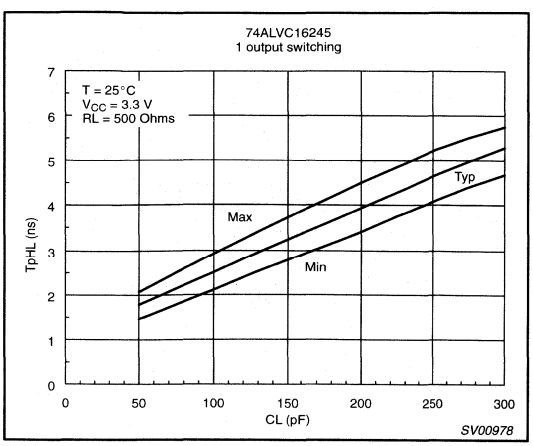

Prop. delay vs. # outputs switching
74LVC16245A
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
CL = 300 pF
TpZH
TpZL
TpLH
TpHL
Prop. delays (ns)
Number of outputs switching
SV00973

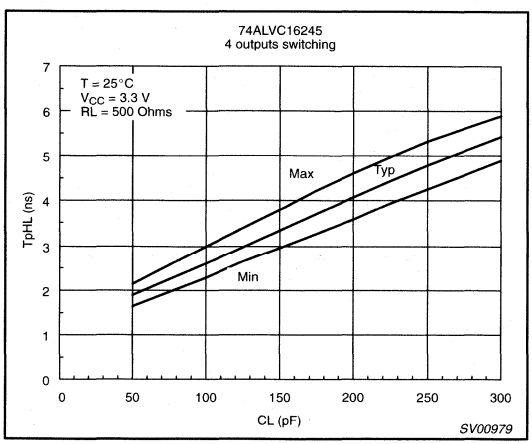

74ALVC16245
1 output switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpLH (ns)
CL (pF)
SV00974

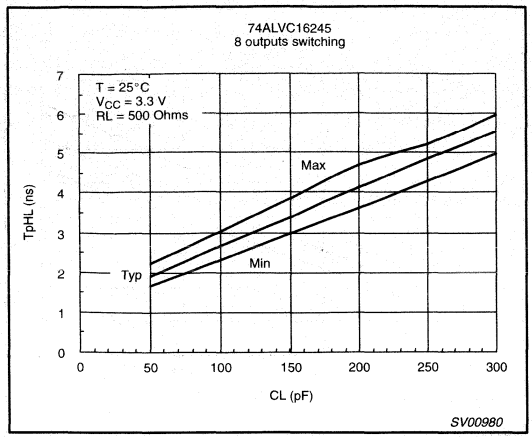

74ALVC16245
4 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpLH (ns)
CL (pF)
SV00975

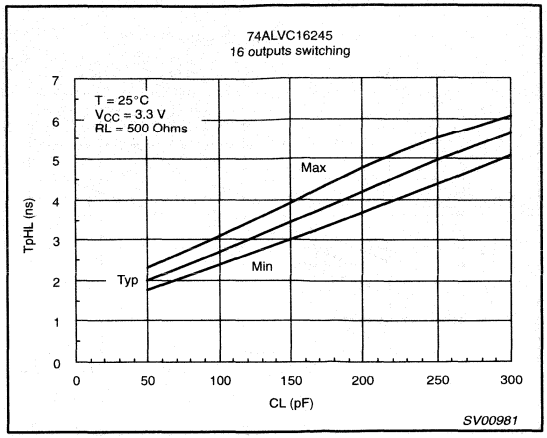

74ALVC16245
8 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpLH (ns)
CL (pF)
SV00976

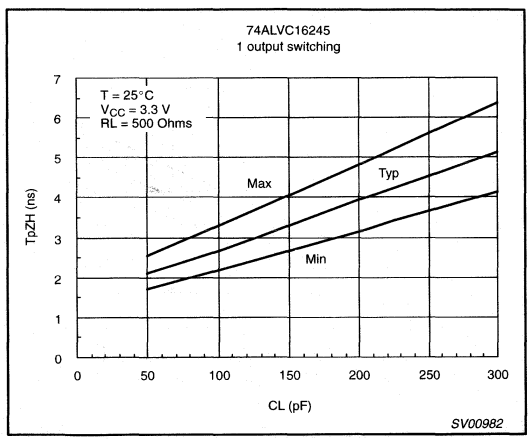

74ALVC16245
16 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpLH (ns)
CL (pF)
SV00977

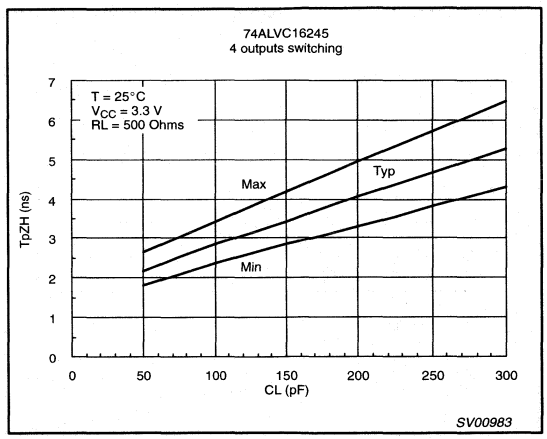

74ALVC16245
1 output switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpHL (ns)
CL (pF)
SV00978

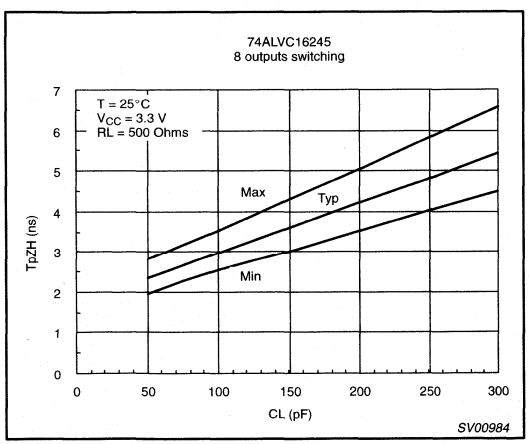

74ALVC16245
4 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpHL (ns)
CL (pF)
SV00979

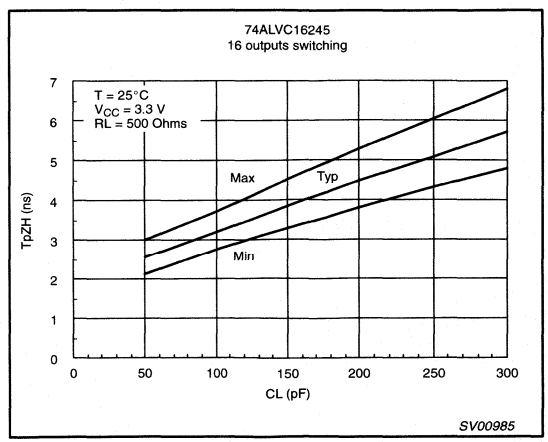

74ALVC16245
8 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpHL (ns)
CL (pF)
SV00980

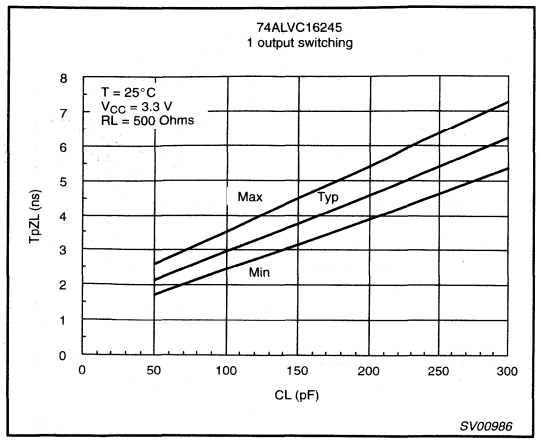

74ALVC16245
16 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpHL (ns)
CL (pF)
SV00981

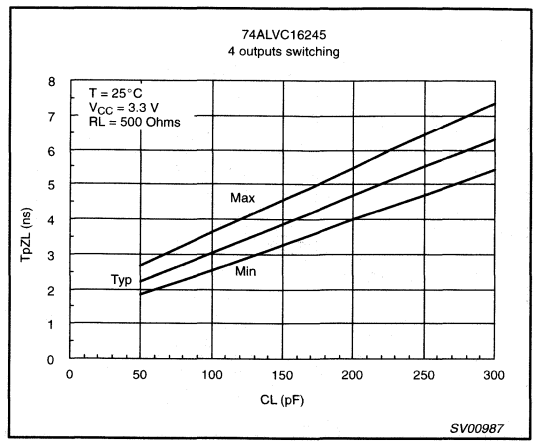

74ALVC16245
1 output switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZH (ns)
CL (pF)
SV00982

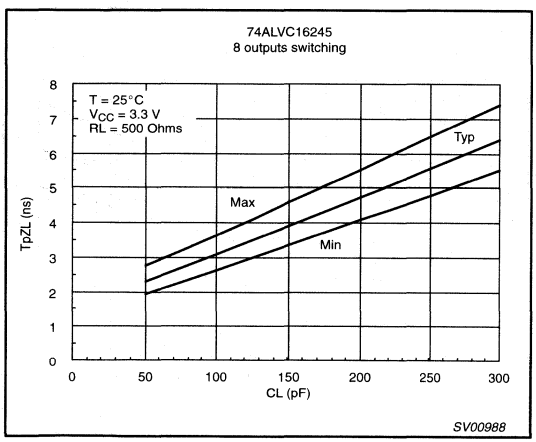

74ALVC16245
4 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZH (ns)
CL (pF)
SV00983

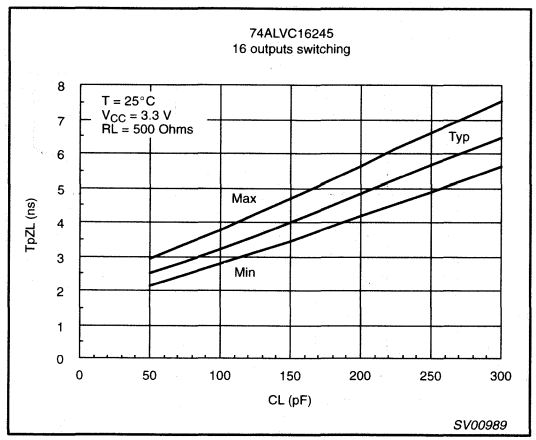

74ALVC16245
8 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZH (ns)
CL (pF)
SV00984

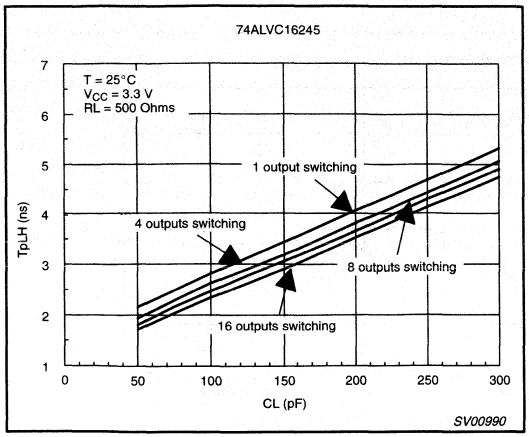

74ALVC16245
16 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZH (ns)
CL (pF)
SV00985

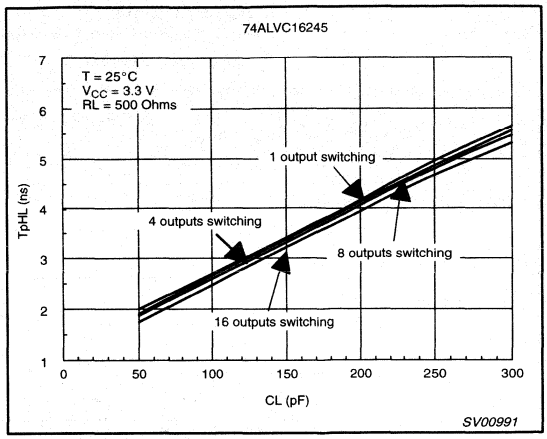

74ALVC16245
1 output switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00986

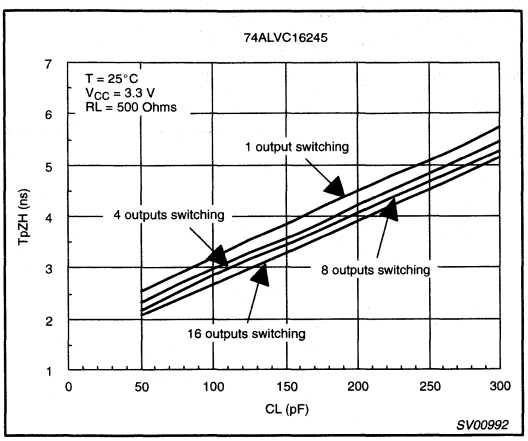

74ALVC16245
4 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00987

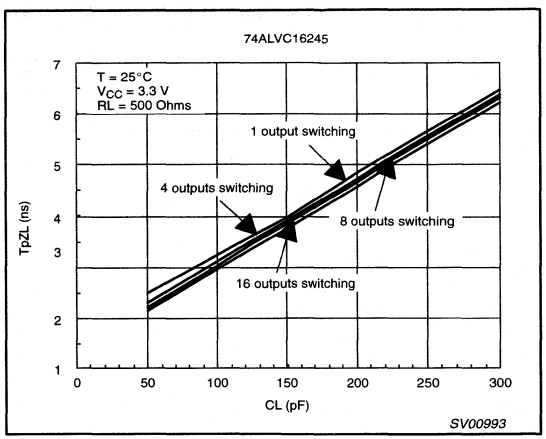

74ALVC16245
8 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00988

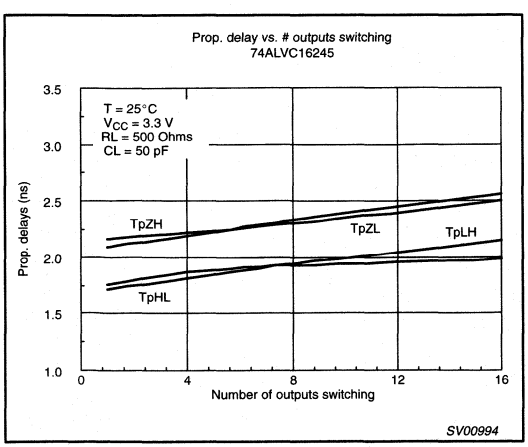

74ALVC16245
16 outputs switching
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
Max
Typ
Min
TpZL (ns)
CL (pF)
SV00989

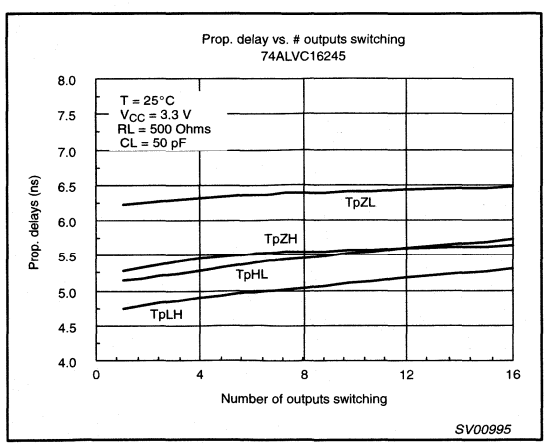

74ALVC16245
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
1 output switching
4 outputs switching
8 outputs switching
16 outputs switching
TpLH (ns)
CL (pF)
SV00990


74ALVC16245
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
1 output switching
4 outputs switching
8 outputs switching
16 outputs switching
TpHL (ns)
CL (pF)
SV00991

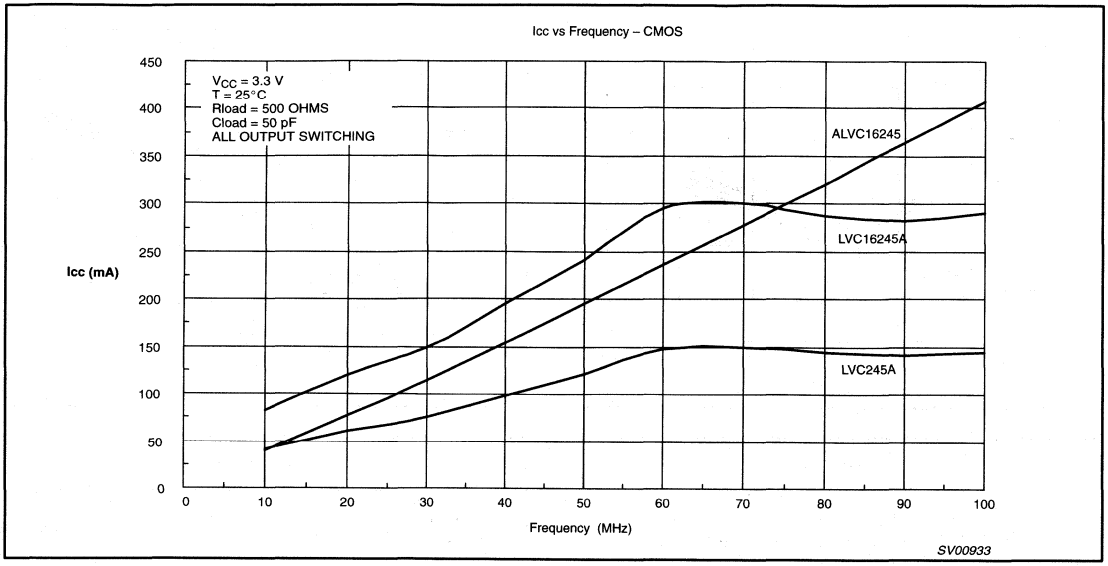

74ALVC16245
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
1 output switching
4 outputs switching
8 outputs switching
16 outputs switching
TpZH (ns)
CL (pF)
SV00992


74ALVC16245
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
1 output switching
4 outputs switching
8 outputs switching
16 outputs switching
TpZL (ns)
CL (pF)
SV00993


Prop. delay vs. # outputs switching
74ALVC16245
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
CL = 50 pF
TpZH
TpZL
TpLH
TpHL
Prop. delays (ns)
Number of outputs switching
SV00994


Prop. delay vs. # outputs switching
74ALVC16245
T = 25°C
VCC = 3.3 V
RL = 500 Ohms
CL = 50 pF
TpZL
TpZH
TpHL
TpLH
Prop. delays (ns)
Number of outputs switching
SV00995

III. SUPPLY CURRENT VERSUS FREQUENCY



IV. V_{OLP}, V_{OLV}, V_{OHV}, V_{OHP} VERSUS C_{LOAD} (C_L)

74LVC245A

General conditions

- T_{amb} = 25°C
- One output quiet, 7 outputs are switching same time.
- Package: SSOP

NOTE: The values are typical.

V_{CC} = 3.3 Volt

C_L (pF)	50	100	150	200	250	300
V_{OLP} (V)	0.628	0.577	0.518	0.467	0.425	0.390
V_{OLV} (V)	–0.87	–0.636	–0.501	–0.409	–0.320	–0.213
V_{OHV} (V)	2.664	2.788	2.869	2.924	2.963	2.993
V_{OHP} (V)	3.674	3.503	3.413	3.354	3.298	3.248

V_{CC} = 2.7 Volt

C_L (pF)	50	100	150	200	250	300
V_{OLP} (V)	0.357	0.340	0.312	0.91	0.272	0.253
V_{OLV} (V)	–0.542	–0.414	0.318	–0.242	–0.146	–0.055
V_{OHV} (V)	2.270	2.351	2.403	2.439	2.464	2.481
V_{OHP} (V)	2.902	2.789	2.726	2.684	2.642	2.625

V_{CC} = 2.5 Volt

C_L (pF)	50	100	150	200	250	300
V_{OLP} (V)	0.269	0.267	0.257	0.242	0.226	0.211
V_{OLV} (V)	–0.450	–0.345	–0.262	–0.182	–0.086	–0.013
V_{OHV} (V)	2.134	2.201	2.244	2.273	2.294	2.305
V_{OHP} (V)	2.646	2.553	0.502	2.461	2.426	2.425

74LVC16245A

General conditions

- T_{amb} = 25°C
- One output quiet, 15 outputs are switching same time.
- Package: SSOP

NOTE: The values are typical.

V_{CC} = 3.3 Volt

C_L (pF)	50	100	150	200	250	300
V_{OHV} (V)	2.79	2.94	3.01	3.05	3.08	3.10
V_{OHP} (V)	3.34	3.28	3.26	3.25	3.23	3.22

V_{CC} = 2.7 Volt

C_L (pF)	50	100	150	200	250	300
V_{OHV} (V)	2.36	2.45	2.49	2.52	2.54	2.55
V_{OHP} (V)	2.69	2.65	2.64	2.63	2.62	2.62

74ALVC16245

General conditions

- T_{amb} = 25°C
- One output quiet, 15 outputs are switching same time.
- Package: SSOP

NOTE: The values are typical.

V_{CC} = 3.3 Volt

C_L (pF)	50	100	150	200	250	300
V_{OLP} (mV)	400	275	210	169	142	122
V_{OLV} (mV)	–385	–177	–94	–66	–48	–36
V_{OHV} (V)	2.84	2.94	2.99	3.03	3.06	3.08
V_{OHP} (V)	3.58	3.42	3.36	3.32	3.30	3.28

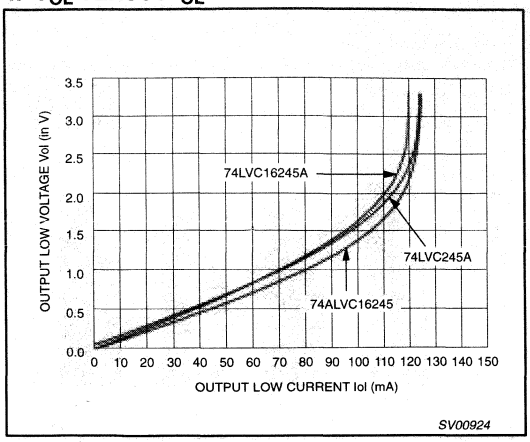
V_{CC} = 2.7 Volt

C_L (pF)	50	100	150	200	250	300
V_{OLP} (mV)	261	181	138	111	93	80
V_{OLV} (mV)	–246	–112	–57	–42	–30	–21
V_{OHV} (V)	2.37	2.44	2.49	2.51	2.53	2.54
V_{OHP} (V)	2.86	2.75	2.71	2.68	2.67	2.65

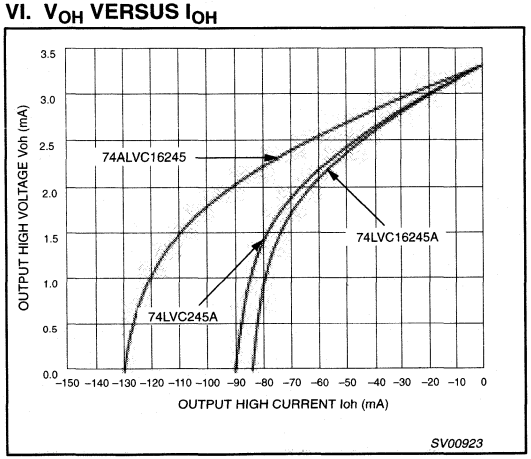
V_{CC} = 1.8 Volt

C_L (pF)	50	100	150	200	250	300
V_{OLP} (mV)	77	56	47	39	33	30
V_{OLV} (mV)	–73	–33	–19	–9	–4	–1
V_{OHV} (V)	1.65	1.68	1.69	1.70	1.70	1.71
V_{OHP} (V)	1.80	1.77	1.75	1.74	1.74	1.74

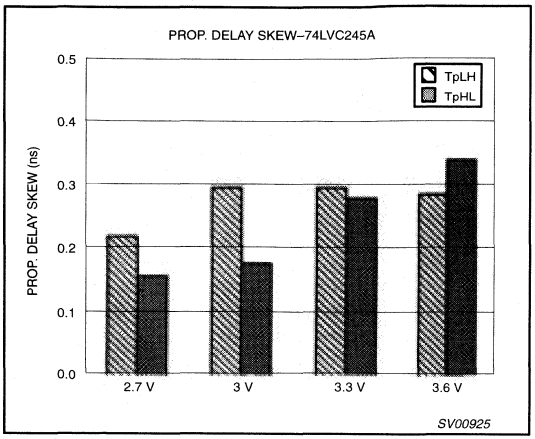
V. V_{OL} VERSUS I_{OL}

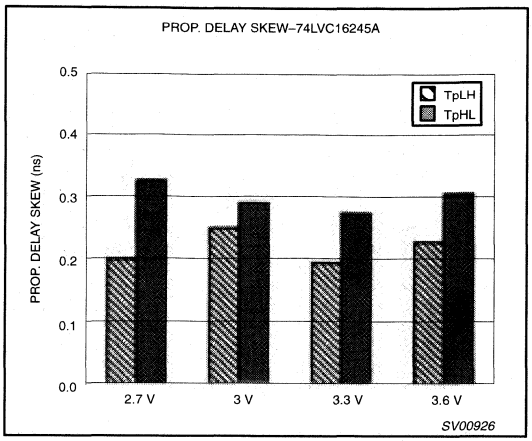


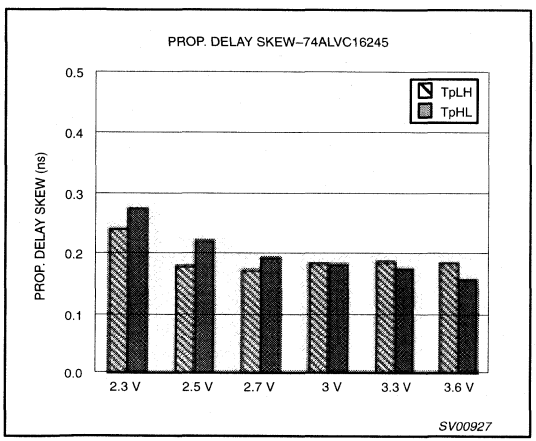
VI. V_{OH} VERSUS I_{OH}

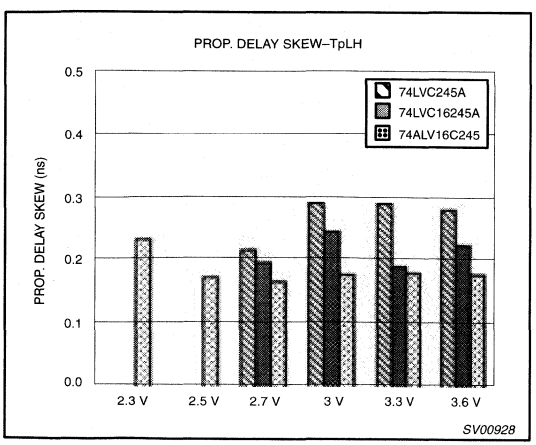


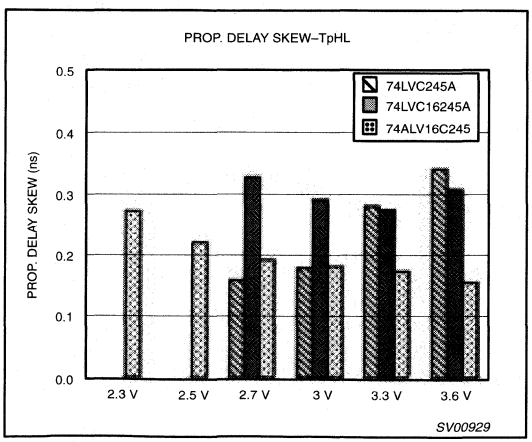
VII. PIN SKEW


PROP. DELAY SKEW–74LVC245A
PROP. DELAY SKEW (ns)
0.5
0.4
0.3
0.2
0.1
0.0
TpLH
TpHL
2.7 V
3 V
3.3 V
3.6 V
SV00925

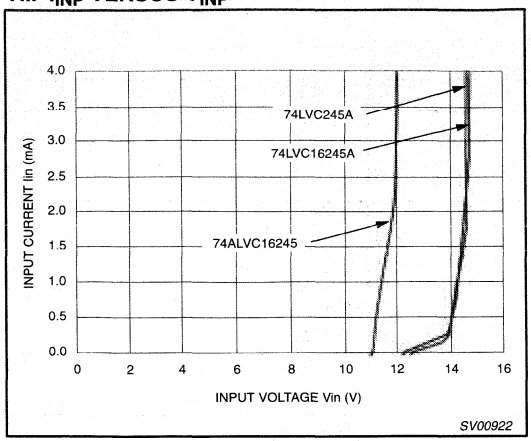

PROP. DELAY SKEW–74LVC16245A
PROP. DELAY SKEW (ns)
0.5
0.4
0.3
0.2
0.1
0.0
TpLH
TpHL
2.7 V
3 V
3.3 V
3.6 V
SV00926


PROP. DELAY SKEW–74ALVC16245
PROP. DELAY SKEW (ns)
0.5
0.4
0.3
0.2
0.1
0.0
TpLH
TpHL
2.3 V
2.5 V
2.7 V
3 V
3.3 V
3.6 V
SV00927

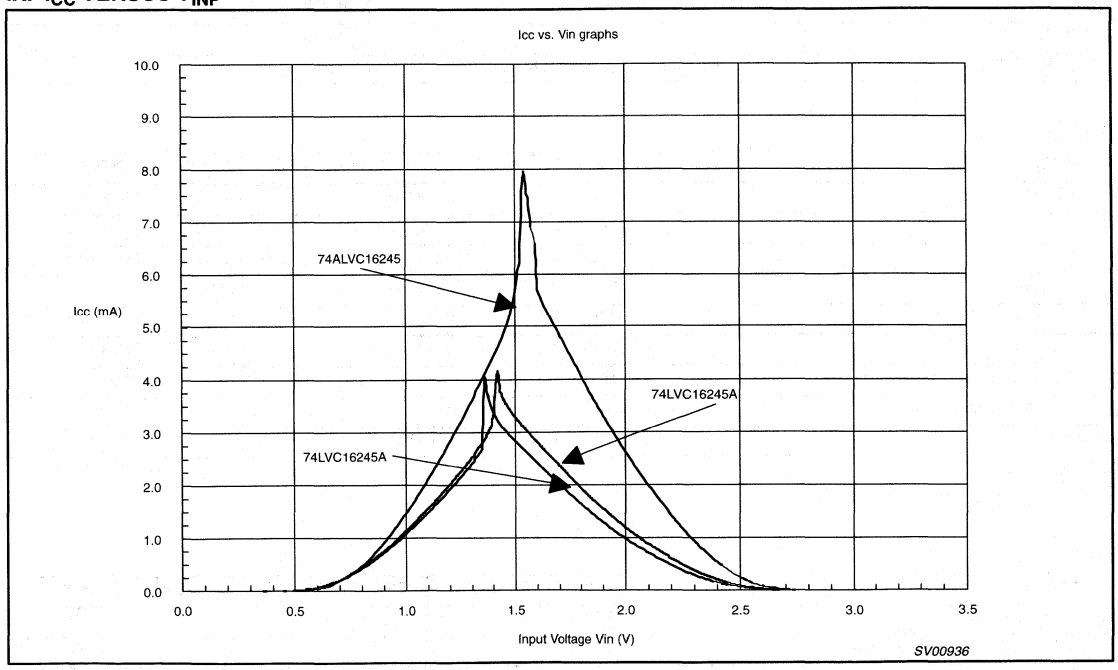

PROP. DELAY SKEW–TpLH
PROP. DELAY SKEW (ns)
0.5
0.4
0.3
0.2
0.1
0.0
74LVC245A
74LVC16245A
74ALV16C245
2.3 V
2.5 V
2.7 V
3 V
3.3 V
3.6 V
SV00928


PROP. DELAY SKEW–TpHL
PROP. DELAY SKEW (ns)
0.5
0.4
0.3
0.2
0.1
0.0
74LVC245A
74LVC16245A
74ALV16C245
2.3 V
2.5 V
2.7 V
3 V
3.3 V
3.6 V
SV00929

VIII I_{INP} VERSUS V_{INP}



IX. I_{CC} VERSUS V_{INP}



FUNCTION SELECTION GUIDE LV FAMILY

GATES

FUNCTION		DEVICE NUMBER
INVERTERS	Hex Inverter	74LV04
	Hex Inverter (unbuffered)	74LVU04
	Hex Inverter (Schmitt-Trigger)	74LV14
NAND	Quad 2-input	74LV00
	Quad 2-input (Open Drain)	74LV03
	Triple 3-input	74LV10
	Dual 4-input	74LV20
	Quad 2-input (Schmitt-Trigger)	74LV132
AND	Quad 2-input	74LV08
	Triple 3-input	74LV11
NOR	Quad 2-input	74LV02
	Triple 3-input	74LV27
OR	Quad 2-input	74LV32
EXCLUSIVE-OR	Quad 2-input	74LV86
MULTIVIBRATOR	Dual retriggerable monostable with reset	74LV123

FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	RESET	OUTPUT
Dual D-type	74LV74	positive	LOW	LOW	NINV INV
Dual J-K	74LV107	negative	–	LOW	NINV INV
Dual J-K	74LV109	positive	LOW	LOW	NINV INV
Hex D-type	74LV174	positive	–	LOW	NINV
Quad D-type	74LV175	positive	–	LOW	NINV INV
Octal D-type	74LV273	positive	–	LOW	NINV
Octal D-type, 3-state	74LV374	positive	–	–	NINV
Octal D-type, data enable	74LV377	positive	–	–	NINV
Octal D-type, 3-state	74LV574	positive	–	–	NINV

NOTE

1. INV = inverting; NINV = non-inverting

LATCHES

FUNCTION	DEVICE NUMBER	RESET LEVEL	ENABLE LEVEL	OUTPUT
8-bit Addressable	74LV259	LOW	LOW	NINV
Octal D-type transparent, 3-state	74LV373	–	HIGH	NINV
Octal D-type transparent, 3-state	74LV573	–	HIGH	NINV

NOTE

1. INV = inverting; NINV = non-inverting

FUNCTION SELECTION GUIDE LV FAMILY (continued)

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	SELECT INPUTS	ENABLE LEVEL	OUTPUT
Dual 4 to 1	74LV153	2 (HIGH)	2 (LOW)	NINV
Quad 2-Input	74LV157	1 (HIGH)	1 (LOW)	NINV
8 to 1, 3-state	74LV251	3 (HIGH)	–	NINV INV
Quad 2 to 1, 3-state	74LV257	1 (HIGH)	–	NINV

NOTE

1. INV = inverting; NINV = non-inverting

DECODERS/MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE LEVEL	OUTPUT
3-to-8 line Decoder/Demultiplexer	74LV138	3	2 (LOW) + 1 (HIGH)	INV
Dual 2-to-4 line Decoder/Demultiplexer	74LV139	2 + 2	1 (LOW) + 1 (LOW)	INV
4-to-16 line Decoder/Demultiplexer	74LV154	4	2 (LOW)	INV

NOTE

1. INV = inverting; NINV = non-inverting

SWITCHES/MULTIPLEXERS/DEMULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE LEVEL	OUTPUT
8-channel analog Multiplexer/Demultiplexer	74LV4051	3	1 (LOW)	NINV
Dual 4-channel analog Multiplexer/Demultiplexer	74LV4052	2	1 (LOW)	NINV
Triple 2-channel analog Multiplexer/Demultiplexer	74LV4053	3	1 (LOW)	NINV
Quad bilateral Switches	74LV4066	–	4 (HIGH)	NINV
16-channel analog Multiplexer/Demultiplexer	74LV4067	4	1 (LOW)	NINV
Quad bilateral analog Switches	74LV4316	4	1 (LOW)	NINV

NOTE

1. INV = inverting; NINV = non-inverting

BUFFERS, DRIVERS, AND TRANSCEIVERS, 3-STATE

FUNCTION	DEVICE NUMBER	OUTPUT ENABLE LEVEL	OUTPUT
Quad buffer/line driver	74LV125	4 (LOW)	NINV
Quad buffer/line driver	74LV126	4 (HIGH)	NINV
Dual Quad buffer/line driver	74LV240	2 (LOW)	INV
Dual Quad buffer/line driver	74LV241	1 (LOW) + 1 (HIGH)	NINV
Dual Quad buffer/line driver	74LV244	2 (LOW)	NINV
Octal bus transceiver	74LV245	LOW	NINV
Hex buffer/line driver	74LV365	2 (LOW)	NINV
4- plus 2 bit buffer/line driver	74LV367	2 (LOW)	NINV
4- plus 2 bit buffer/line driver	74LV368	2 (LOW)	INV
Octal buffer/line driver	74LV541	2 (LOW)	NINV

NOTE

1. INV = inverting; NINV = non-inverting

FUNCTION SELECTION GUIDE LV FAMILY (continued)

SHIFT REGISTERS

FUNCTION	DEVICE NUMBER	BITS	CLOCK	MASTER RESET	OUTPUT
Serial-In / parallel-out	74LV164	8	positive	LOW	NINV
Parallel-In / Serial-out with clock enable	74LV165	8	positive	–	NINV INV
Serial-In / Serial or Parallel-out with output latches, 3-state	74LV595	8	positive	LOW	NINV
Shift-and-store bus register, 3-state	74LV4094	8	positive	–	NINV

NOTE

1. INV = inverting; NINV = non-inverting

COUNTERS

FUNCTION	DEVICE NUMBER	BITS	CLOCK	MASTER RESET	PRESETTABLE
Synchronous 4-bit binary, asynchrounous reset	74LV161	4	positive	LOW	yes
Synchronous 4-bit binary, synchrounous reset	74LV163	4	positive	LOW	yes
Dual 4-bit binary ripple counter	74LV393	4	negative	HIGH	–
14-stage binary ripple counter	74LV4020	14	negative	HIGH	–
12-stage binary ripple counter	74LV4040	12	negative	HIGH	–
14-stage binary ripple counter with oscillator	74LV4060	14	positive	HIGH	–

NOTE

1. INV = inverting; NINV = non-inverting

ARITHMETIC FUNCTION

FUNCTION	DEVICE NUMBER	OUTPUT ENABLE LEVEL
8-bit Magnitude Comparator	74LV688	LOW

SPECIAL FUNCTION

FUNCTION	DEVICE NUMBER	NUMBER OF CELLS
Timer for NiCd and NiMH chargers	74LV4799	1 to 4

FUNCTION SELECTION GUIDE LVC FAMILY

GATES

FUNCTION		DEVICE NUMBER
INVERTERS	Hex Inverter	74LVC04A
	Hex Inverter (unbuffered)	74LVCU04A
	Hex Inverter (Schmitt-Trigger)	74LVC14
NAND	Quad 2-input	74LVC00A
	Triple 3-input	74LVC10A
AND	Quad 2-input	74LVC08A
	Triple 3-input	74LV11
NOR	Quad 2-input	74LVC02A
	Triple 3-input	74LVC27
OR	Quad 2-input	74LVC32A
EXCLUSIVE-OR	Quad 2-input	74LVC86A

FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	RESET	OUTPUT
Dual D-type	74LVC74A	positive	LOW	LOW	NINV INV
Dual J-K	74LVC109	positive	LOW	LOW	NINV INV
Octal D-type	74LVC273	positive	–	LOW	NINV
Octal D-type, 3-State	74LVC374A	positive	–	–	NINV
Octal D-type, data enable	74LVC377	positive	–	–	NINV
Octal D-type, 3-State	74LVC574A	positive	–	–	NINV
10-Bit D-type, 3-State	74LVC821A	positive	–	–	NINV
9-Bit D-type, 3-State	74LVC823A	positive	–	LOW	NINV

NOTE

1. INV = inverting; NINV = non-inverting

LATCHES, 3-STATE

FUNCTION	DEVICE NUMBER	OUTPUT ENABLE LEVEL	INPUT ENABLE LEVEL	OUTPUT
Octal D-type transparent	74LVC373A	LOW	HIGH	NINV
Octal D-type transparent	74LVC573A	LOW	HIGH	NINV
10-bit transparent latch	74LVC841A	LOW	HIGH	NINV

NOTE

1. INV = inverting; NINV = non-inverting

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	SELECT INPUTS	ENABLE LEVEL	OUTPUT
Quad 2-Input	74LVC157A	1 (HIGH)	1 (LOW)	NINV
Quad 2 to 1, 3-State	74LVC257A	1 (HIGH)	–	NINV

NOTE

1. INV = inverting; NINV = non-inverting

FUNCTION SELECTION GUIDE LVC FAMILY (continued)

DECODERS/DEMULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE LEVEL	OUTPUT
3-to-8 line Decoder/Demultiplexer	74LVC138A	3	2 (LOW)+1 (HIGH)	INV
Dual 2-to-4 line Decoder/Demultiplexer	74LVC139	2 + 2	1 (LOW)+1 (LOW)	INV

NOTE

1. INV = inverting; NINV = non-inverting

REGISTERS, 3-STATE

FUNCTION	DEVICE NUMBER	BITS	LATCH ENABLE	OUTPUT
Octal D-type registered transceiver	74LVC543A	8	LOW	NINV
Octal registered transceiver	74LVC544A	8	LOW	INV
Octal bus transceiver/register	74LVC646A	8	–	NINV
Octal bus transceiver/register	74LVC652	8	–	NINV
Octal registered transceiver	74LVC2952A	8	–	NINV

NOTE

1. INV = inverting; NINV = non-inverting

LATCHES, COUNTERS

FUNCTION	DEVICE NUMBER	BITS	CLOCK EDGE	MASTER RESET	PRESETTABLE
Synchronous 4-bit binary, asynchrounous reset	74LVC161	4	positive	LOW	yes
Synchronous 4-bit binary, synchrounous reset	74LVC163	4	positive	LOW	yes
Synchronous 4-bit binary, up/down binary counter	74LVC169	4	positive	–	yes

BUFFERS, DRIVERS, AND TRANSCEIVERS, 3-STATE

FUNCTION	DEVICE NUMBER	OUTPUT ENABLE LEVEL	BUS HOLD	OUTPUT
4-bit buffer/line driver	74LVC125A	4 (LOW)	–	NINV
4-bit buffer/line driver	74LVC126A	4 (HIGH)	–	NINV
4-bit buffer/line driver	74LVC240A	2 (LOW)	–	INV
4-bit buffer/line driver	74LVC241A	1 (LOW)+1 (HIGH)	–	NINV
4-bit buffer/line driver	74LVC244A	2 (LOW)	–	NINV
8-bit buffer/line driver	74LVCH244A	2 (LOW)	yes	NINV
Octal bus transceiver	74LVC245A	LOW	–	NINV
Octal bus transceiver	74LVCH245A	LOW	yes	NINV
Octal buffer/line driver	74LVC541A	2 (LOW)	–	NINV
Octal transceiver	74LVC623A	1 (LOW)+1 (HIGH)	–	NINV
10-bit buffer/line driver	74LVC827A	2 (LOW)	–	NINV

NOTE

1. INV = inverting; NINV = non-inverting

FUNCTION SELECTION GUIDE **LVC FAMILY (continued)**

16-BIT BUFFERS, DRIVERS, AND TRANSCEIVERS, 3-STATE

FUNCTION	DEVICE NUMBER	OUTPUT ENABLE LEVEL	BUS HOLD	30 Ω SERIES RESISTOR	OUTPUT
16-bit Buffer/Line driver	74LVC16240A	4 (LOW)	–	–	INV
16-bit Buffer/Line driver	74LVC16241A	2 (LOW) + 2 (HIGH)	–	–	NINV
16-bit Buffer/Line driver	74LVC16244A	4 (LOW)	–	–	NINV
16-bit Buffer/Line driver	74LVCH16244A	4 (LOW)	yes	–	NINV
16-bit Buffer/Line driver	74LVC162244A	4 (LOW)	–	yes	NINV
16-bit Buffer/Line driver	74LVCH162244A	4 (LOW)	yes	yes	NINV
16-bit Buffer/Line driver	74LVCH16541A	2 (LOW) +2 (LOW)	yes	–	NINV
16-bit bus transceiver	74LVC16245A	2 (LOW)	–	–	NINV
16-bit bus transceiver	74LVCH16245A	2 (LOW)	yes	–	NINV
16-bit bus transceiver	74LVC162245A	2 (LOW)	–	yes	NINV
16-bit bus transceiver	74LVCH162245A	2 (LOW)	yes	yes	NINV

NOTE

1. INV = inverting; NINV = non-inverting

16-BIT FLIP-FLOPS, 3-STATE

FUNCTION	DEVICE NUMBER	OUTPUT ENABLE LEVEL	BUS HOLD	CLOCK EDGE	OUTPUT
16-bit D-type positive edge triggered	74LVC16374A	2 (LOW)	–	positive	NINV
16-bit D-type positive edge triggered	74LVCH16374A	2 (LOW)	yes	positive	NINV

NOTE

1. INV = inverting; NINV = non-inverting

16-BIT LATCHES, 3-STATE

FUNCTION	DEVICE NUMBER	OUTPUT ENABLE LEVEL	BUS HOLD	LATCH ENABLE	OUTPUT
16-bit D-type transparent latch	74LVC16373A	2 (LOW)	–	2 (HIGH)	NINV
16-bit D-type transparent latch	74LVCH16373A	2 (LOW)	yes	2 (HIGH)	NINV

NOTE

1. INV = inverting; NINV = non-inverting

SPECIAL FUNCTION

FUNCTION	DEVICE NUMBER
Parallel printer Interface transceiver, buffer	74LVC1284
8-Bit dual supply translating transceiver, 3-State	74LVC4245A

FUNCTION SELECTION GUIDE ALVCFAMILY

MULTI-BIT BUFFERS, DRIVERS, AND TRANSCEIVERS, 3-STATE

FUNCTION	DEVICE NUMBER	OUTPUT ENABLE LEVEL	BUS HOLD	30 Ω TERMINATION RESISTOR	OUTPUT[1]
16-bit buffer/line driver	74ALVC16244	4 (LOW)	–	–	NINV
16-bit buffer/line driver	74ALVCH16244	4 (LOW)	YES	–	NINV
16-bit buffer/line driver	74ALVCH162244	4 (LOW)	YES	YES	NINV
16-bit bus transceiver	74ALVC16245	2 (LOW)	–	–	NINV
16-bit bus transceiver	74ALVCH16245	2 (LOW)	YES	–	NINV
16-bit bus transceiver	74ALVCH162245	2 (LOW)	YES	YES	NINV
18-bit Universal Bus transceiver	74ALVCH16500	1 (LOW) + 1 (HIGH)	YES	–	NINV
18-bit Universal Bus transceiver	74ALVCH16501	1 (LOW) + 1 (HIGH)	YES	–	NINV
16-bit buffer/line driver	74ALVCH16540	2 (LOW) + 2 (LOW)	YES	–	INV
18-bit Universal Bus transceiver	74ALVCH16600	2 (LOW)	YES	–	NINV
18-bit Universal Bus transceiver	74ALVCH16601	2 (LOW)	YES	–	NINV
16-bit bus transceiver	74ALVCH16623	1 (LOW) + 1 (HIGH)	YES	–	NINV
18-bit buffer/driver	74ALVCH16825	2 (LOW) + 2 (LOW)	YES	–	NINV
20-bit buffer/driver	74ALVCH16827	2 (LOW) + 2 (LOW)	YES	–	NINV
20-bit buffer/driver	74ALVCH162827	2 (LOW) + 2 (LOW)	YES	YES	NINV
18-bit buffer/driver	74ALVC16835	1 (LOW)	–	–	NINV
18-bit buffer/driver	74ALVC162835	1 (LOW)	–	YES	NINV

NOTE

1. INV = inverting; NINV = non-inverting

MULTI-BIT FLIP-FLOPS, 3-STATE

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	RESET	BUS HOLD	OUTPUT[1]
16-bit D-type	74ALVCH16374	positive	–	–	YES	NINV
20-bit D-type	74ALVCH16821	positive	–	–	YES	NINV
18-bit D-type	74ALVCH16823	positive	–	LOW	YES	NINV

NOTE

1. NINV = non-inverting

MULTI-BIT LATCH, 3-STATE

FUNCTION	DEVICE NUMBER	OUTPUT ENABLE LEVEL	INPUT ENABLE LEVEL	BUS HOLD	OUTPUT[1]
16–bit D–type transparent latch	74ALVCH16373	2 (LOW)	2 (HIGH)	YES	NINV
20–bit D–type transparent latch	74ALVCH16841	2 (LOW)	2 (HIGH)	YES	NINV
18–bit latch with set and reset	74ALVCH16843	2 (LOW)	2 (HIGH)	YES	NINV

NOTE

1. NINV = non-inverting

FUNCTION SELECTION GUIDE ALVC FAMILY (continued)

REGISTERS, 3-STATE

FUNCTION	DEVICE NUMBER	INPUT ENABLE LEVEL	OUTPUT ENABLE LEVEL	BUS HOLD	OUTPUT[1]
16–bit D–type registered transceiver	74ALVCH16543	2 (LOW) + 2 (LOW)	2 (LOW) + 2 (LOW)	YES	NINV
16–bit transceiver/register	74ALVCH16646	–	1 (LOW) + 1 (LOW)	YES	NINV
16–bit transceiver/register	74ALVCH16652	–	2 (LOW) + 2 (HIGH)	YES	NINV
16–bit transceiver/register	74ALVCH16952	–	2 (LOW) + 2 (LOW)	YES	NINV

NOTE

1. NINV = non-inverting

SPECIAL FUNCTION

FUNCTION	DEVICE NUMBER
16–Bit dual supply translating transceiver, 3–state	74ALVC164245

REPLACEMENT LIST LVC TO LVCXXXA

LVC PART TYPE	Function	Improvement	Replacement
74LVC00	2–Input NAND Gate	speed	74LVC00A
74LVC02	2–Input NOR Gate	speed	74LVC02A
74LVC04	Hex Inverter Gate	speed	74LVC04A
74LVCU04	Hex Inverter Gate	rename	74LVCU04A
74LVC08	2–Input AND Gate	speed	74LVC08A
74LVC10	Triple 3–Input NAND Gate	rename	74LVC10A
74LVC32	2–Input OR Gate	speed	74LVC32A
74LVC74	Dual D-type Flip–Flop	speed	74LVC74A
74LVC86	2–Input XOR Gate	speed	74LVC86A
74LVC125	Quad Buffer	5V tolerance/speed	74LVC125A
74LVC138	3-to-8 Line Decoder/Demultiplexer; inverting	rename	74LVC138A
74LVC139	Dual 2-to-4 Decoder/Demultiplexer	rename	74LVC139A
74LVC157	2–1 Data Selector/MUX	speed	74LVC157A
74LVC240	Octal Buffer	5V I/O tolerance/speed	74LVC240A
74LVC241	Octal Buffer	5V I/O tolerance/speed	74LVC241A
74LVC244	Octal Buffer	5V I/O tolerance/speed	74LVC244A
74LVC245	Octal Transceivers	5V I/O tolerance/speed	74LVC245A
74LVC257	MUX	5V I/O tolerance/speed	74LVC257A
74LVC373	Octal Latch	5V I/O tolerance/speed	74LVC373A
74LVC374	Octal Flip–Flop	5V I/O tolerance/speed	74LVC374A
74LVC541	Octal Buffer/Line Driver	5V I/O tolerance/speed	74LVC541A
74LVC543	Octal Transceiver	5V I/O tolerance/speed	74LVC543A
74LVC544	Octal Latched Transceiver	5V I/O tolerance/speed	74LVC544A
74LVC573	Octal Latch	5V I/O tolerance/speed	74LVC573A
74LVC574	Octal Flip–Flop	5V I/O tolerance/speed	74LVC574A
74LVC623	Octal Transceiver	5V I/O tolerance/speed	74LVC623A
74LVC646	Octal Bus Transceiver	5V I/O tolerance/speed	74LVC646A
74LVC4245	Octal Dual supply Translating Transceiver	rename	74LVC4245A

NOTE:
1. 5V input tolerant

REPLACEMENT LIST LVCH16 TO LVCH16XXXA

LVCH16 PART TYPE	Function	Improvement	Replacement
74LVCH16240	16-bit Buffer Inverting	5V tolerance	74LVCH16240A
74LVCH16241	16-bit Buffer	5V tolerance	74LVCH16241A
74LVCH16244	16-bit Octal Buffer	5V tolerance	74LVCH16244A
74LVC162244	16-bit Buffer with termination resistors	5V tolerance	74LVC162244A
74LVCH162244	16-bit Buffer with termination resistors	5V tolerance	74LVCH162244A
74LVC16245	16-bit Octal Transceiver	5V tolerance	74LVC16245A
74LVCH16245	16-bit Octal Transceiver	5V tolerance	74LVCH16245A
74LVC162245	16-bit Transceiver with termination resistors	5V tolerance	74LVC162245A
74LVCH162245	16-bit Transceiver with termination resistors	5V tolerance	74LVCH162245A

REPLACEMENT LIST LVCH16 TO LVCH16XXXA (Continued)

LVCH16 PART TYPE	Function	Improvement	Replacement
74LVC16373	16-bit transparent Latch	5V tolerance	74LVC16373A
74LVCH16373	16-bit transparent Latch	5V tolerance	74LVCH16373A
74LVC16374	16-bit edge triggered D-type Flip-Flop	5V tolerance	74LVC16374A
74LVCH16374	16-bit edge triggered D-type Flip-Flop	5V tolerance	74LVCH16374A
74LVCH16541	16-bit Buffer/Line Driver	5V tolerance	74LVCH16541A

Ordering Information

LOW VOLTAGE (3.3V CMOS) LOGIC – LV

Example: 74LVXXX D

Package Code
Device Number

TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE CODE
T_{amb} = –40°C to +85°C	74LVXXX	N = Plastic Dual In-Line D = Plastic SO DB = Shrink Small Outline (SSOP) PW = Thin Shrink Small Outline (TSSOP)

LOW VOLTAGE (3.3V CMOS) LOGIC – LVC

Example: 74LVCXXX D

Package Code
Device Number

TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE CODE
T_{amb} = –40°C to +85°C	74LVCXXX	D = Plastic SO DB = Shrink Small Outline (SSOP) PW =Thin Shrink Small Outline (TSSOP)

LOW VOLTAGE (3.3V CMOS) LOGIC – LVC16

Example: 74LVC16XXX DL

Package Code
Device Number

TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE CODE
T_{amb} = –40°C to +85°C	74LVC16XXX	DL = Plastic SSOP DGG =Thin Shrink Small Outline (TSSOP)

LOW VOLTAGE (3.3V CMOS) LOGIC – ALVC16

Example: 74ALVC16XXX DL

Package Code
Device Number

TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE CODE
T_{amb} = –40°C to +85°C	74ALVC16XXX	DL = Shrink Small Outline (SSOP) DGG=Thin Shrink Small Outline (TSSOP)

TOTAL QUALITY MANAGEMENT

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Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

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The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

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- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

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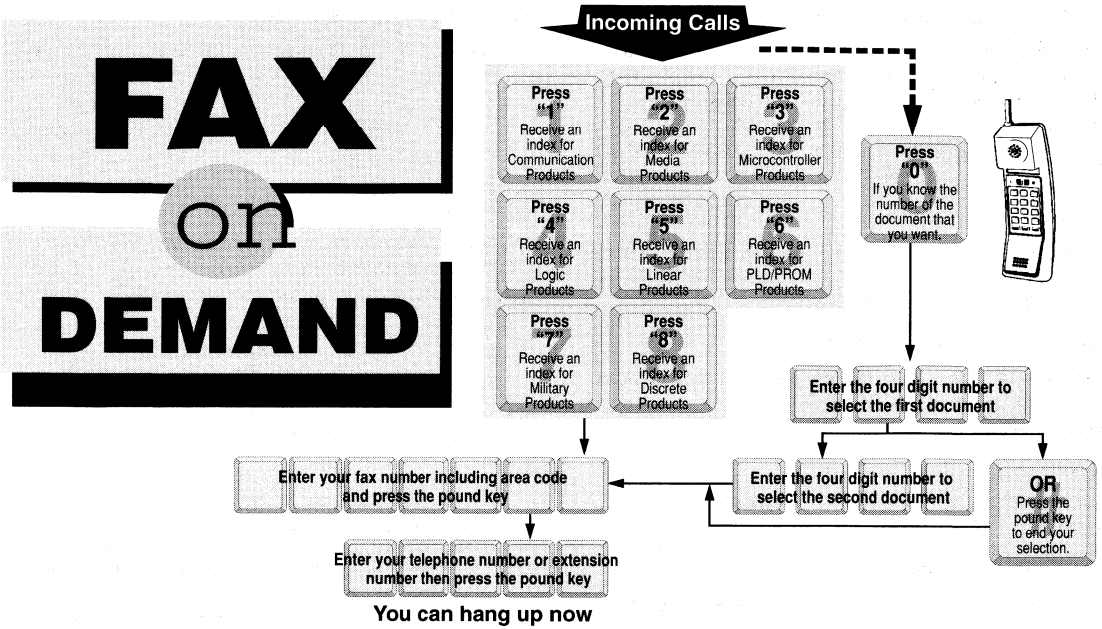

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ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor
- All mains-powered electrical equipment should be connected via an earth leakage switch
- Equipment cases should be earthed
- Relative humidity should be maintained between 50 and 65%
- An ionizer should be used to neutralize objects with immobile static charges

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

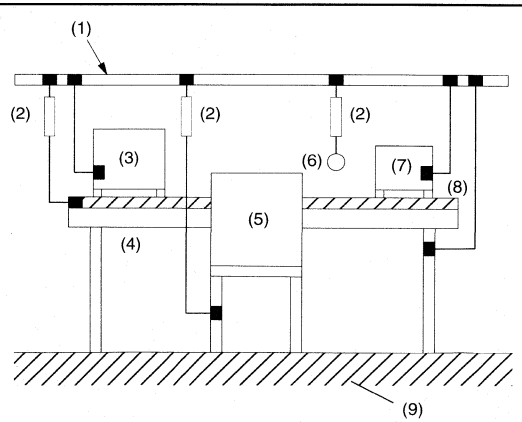
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair
(6) Wrist strap.
(7) Electrical equipment.
(8), (9) Conductive surface/antistatic sheet.

Figure 1. Protected work station

SPICE / Behavorial/IBIS models

SPICE Models

SPICE models are available for Philips logic families. These models play an important role in optimizing applications and improving understanding of practical details so that designers can take better measures to improve their designs. Design changes and optimization can be done prior to circuit board layout, saving time and effort.

SPICE may be used to test behavior in exceptional circumstances or situations that are not covered in the data sheets of the parts. For instance it is possible to see the effect of higher capacitive loading of the outputs. Also, testing of waveforms inside a package is virtually impossible, but with SPICE one may actually check waveforms and currents inside the IC. This may be very helpful in estimating noise voltage developed across bonding wires (ground bounce) and EMC aspects. Last but not least, SPICE models are very helpful in testing an application with worst case devices. The worst case models are actually worse than the worst case parts delivered to customers. This allows for the design of very safe applications in a variety of environmental conditions.

You can request the SPICE libraries with a modeling manual through your Philips Semiconductors representative. Model updates can be downloaded from the Logic Products Group Web site at: www.semiconductors.philips.com/logic/support.

Behavioral/IBIS Models

Behavioral models are another signal integrity tool that designers can use to predict circuit behavior. Third party models are offered through Mentor Graphics for various Philips logic product families. Mentor generates ICX MasterModel Digital Logic Libraries based on measurements from actual parts. Models are available for Interconnectix, Quad, Cadence, Hyperlynx, Veribest, and IBIS compatible simulators. For information, visit Mentor's web site at www.mentorg.com/icx/icx_models/product.html.

IBIS model generation within the Logic Products group is in progress for logic product types, so check the Logic Products Group Web site for updates.

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire 74LV/74LVU family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

This low-voltage CMOS logic family is based on Philips'well-known HCMOS (HC) range and uses the same well-proven fabrication process with only slight modifications.

It operates from a typical supply voltage of 3.3 V but can be used within the supply voltage range 1.0 V to 3.6 V. With a 3.3 V supply, the speed and performance is the same as HCMOS with a 5 V supply.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire LV 5V family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

This low-voltage CMOS logic family is based on Philips'well-known HCMOS (HC) range and uses the same well-proven fabrication process with only slight modifications.

It operates from a typical supply voltage of 3.3 V but can be used within the supply voltage range 1.0 V to 5.5 V. With a 3.3 V supply, the speed and performance is the same as HCMOS with a 5 V supply.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire LVC family, unless otherwise specified in the individual device data sheet.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
$V_{I/O}$	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –6mA[10]	V_{CC} – 0.5			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA[10]	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA[10]	V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 6mA[10]			0.40	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA[10]		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 12mA[10]			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND[6]		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND[9]		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V			±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0[7]		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0[8]		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 3.0V; V_I = 0.8V[2, 3, 4]	75			µA
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 3.0V; V_I = 2.0V[2, 3, 4]	–75			µA
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2, 3, 5]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2, 3, 5]	–500			µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.
7. Valid for LVC(H)-A / LVC(H)2-A.
8. Valid for LVC(H)16-A / LVC(H)162-A.
9. For I/O parts, the parameter I_{OZ} includes the input leakage current.
10. For data outputs of damping resistor parts (LVC(H)2 and LVC(H)162 only)

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire ALVC family, unless otherwise specified in the individual device data sheet.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range[1]		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

NOTE:
1. For non-bus hold ALVC types, the maximum input voltage range is 5.5V.

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA[4]	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA[4]	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA[4]	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA[4]	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA[4]	V_{CC} – 1.0	V_{CC} – 0.28		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –4mA[5]	V_{CC} – 0.4	V_{CC} – 0.11		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA[5]	V_{CC} – 0.6	V_{CC} – 0.17		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –4mA[5]	V_{CC} – 0.5	V_{CC} – 0.09		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –8mA[5]	V_{CC} – 0.7	V_{CC} – 0.19		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA[5]	V_{CC} – 0.6	V_{CC} – 0.13		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA[5]	V_{CC} – 1.0	V_{CC} – 0.27		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA[4]		0.07	0.40	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA[4]		0.15	0.70	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA[4]		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA[4]		0.27	0.55	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 4mA[5]		0.07	0.40	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA[5]		0.11	0.55	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 4mA[5]		0.06	0.40	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA[5]		0.13	0.60	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA[5]		0.09	0.55	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA[5]		0.19	0.80	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND (Not for I/O pins)		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = V_{CC} or GND[3]		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[5]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[5]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[5]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[5]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.
3. For I/O ports, teh parameter I_{OZ} includes the input leakage current.
4. Valid for ALVC(H)16, standard output parts..
5. Valid for ALVC(H)162, termination resistor parts.

Section 2
Low Voltage HCMOS Devices (LV)

Advanced Low Voltage CMOS Logic

CONTENTS

Section 2
Low Voltage HCMOS Devices (LV)

Advanced Low Voltage CMOS Logic

Quad 2-input NAND gate 74LV00

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV00 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT00.

The 74LV00 provides the 2-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 3.3 V	7	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	22	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV00 N	74LV00 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV00 D	74LV00 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV00 DB	74LV00 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV00 PW	74LV00PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

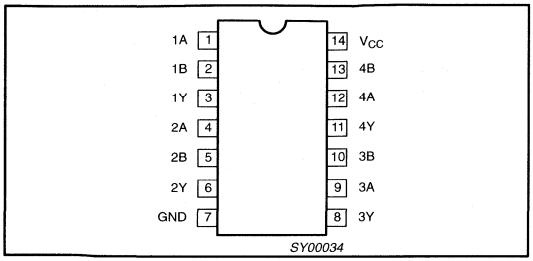
FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

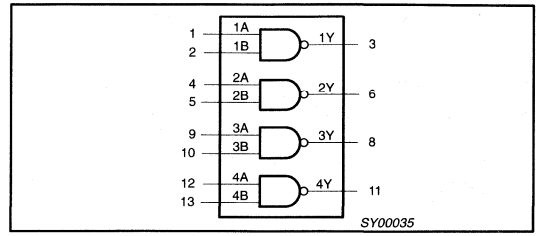
NOTES:

H = HIGH voltage level
L = LOW voltage level

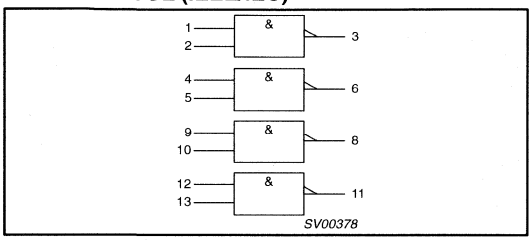
PIN CONFIGURATION



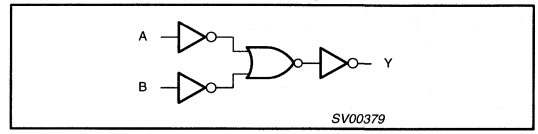
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	$0.7*V_{CC}$			$0.7*V_{CC}$		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			$0.3*V_{CC}$		$0.3*V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
$t_{PHL/PLH}$	Propagation delay nA, nB to nY	Figures 1, 2	1.2		45				ns
			2.0		15	26		31	
			2.7		11	18		23	
			3.0 to 3.6		9[2]	15		18	
			4.5 to 5.5		6.5[3]	11		14	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C.
2. Typical values are measured at V_{CC} = 3.3 V.
3. Typical values are measured at V_{CC} = 5.0 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V and $\geq$ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

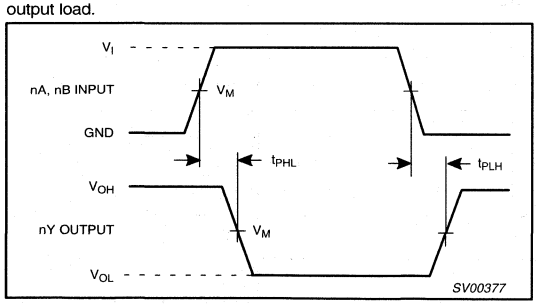


Figure 1. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT

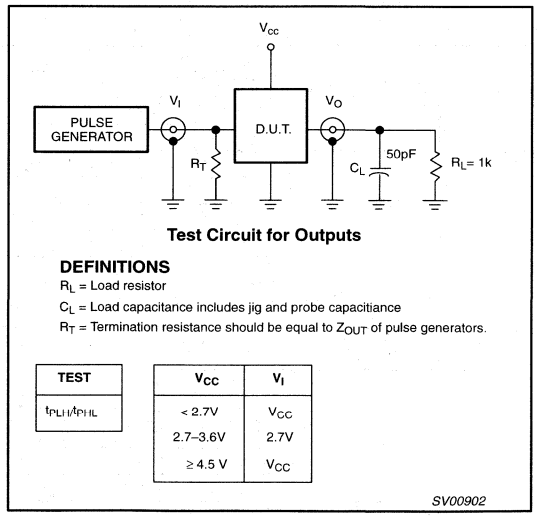


Figure 2. Load circuitry for switching times.

Quad 2-input NOR gate 74LV02

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 5.5 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV02 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT02.

The 74LV02 provides the 2-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 3.3 V	6	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	22	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV02 N	74LV02 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV02 D	74LV02 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV02 DB	74LV02 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV02 PW	74LV02PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 10, 13	1Y – 4Y	Data outputs
2, 5, 8, 11	1A – 4A	Data inputs
3, 6, 9, 12	1B – 4B	Data inputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

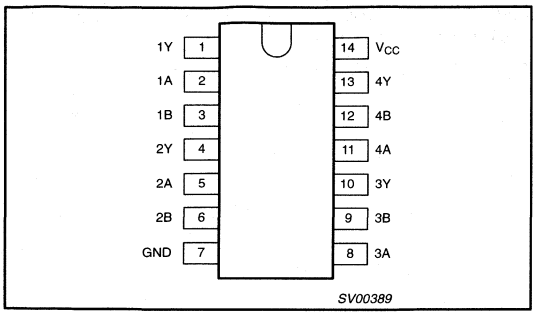
FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

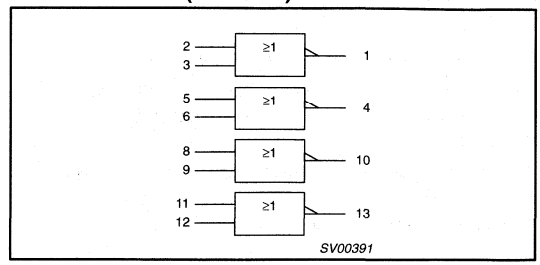
NOTES:

H = HIGH voltage level
L = LOW voltage level

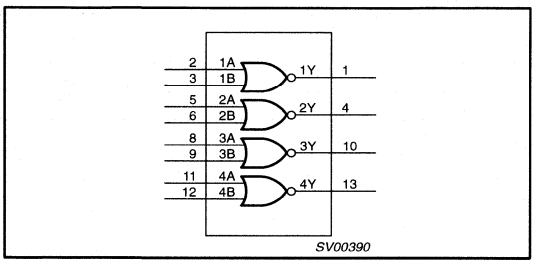
PIN CONFIGURATION



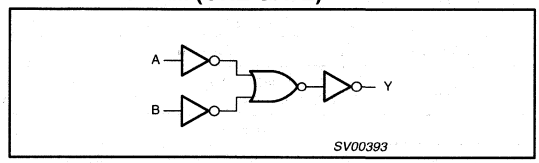
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM (ONE GATE)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP.[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	$0.7*V_{CC}$			$0.7*V_{CC}$		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			$0.3*V_{CC}$		$0.3*V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND			1.0		1.0	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP.[1]	MAX	MIN	MAX	
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} −0.6V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP.[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	Figures 1, 2	1.2		40				ns
			2.0		14	21		26	
			2.7		10	15		19	
			3.0 to 3.6		7.5[2]	12		15	
			4.5 to 5.5		6.0[3]	10		13	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.
3. Typical values are measured at V_{CC} = 5.0 V.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V and ≤ 3.6 V;
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V and ≥ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

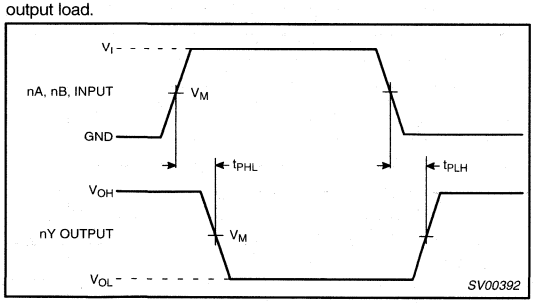


Figure 1. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT

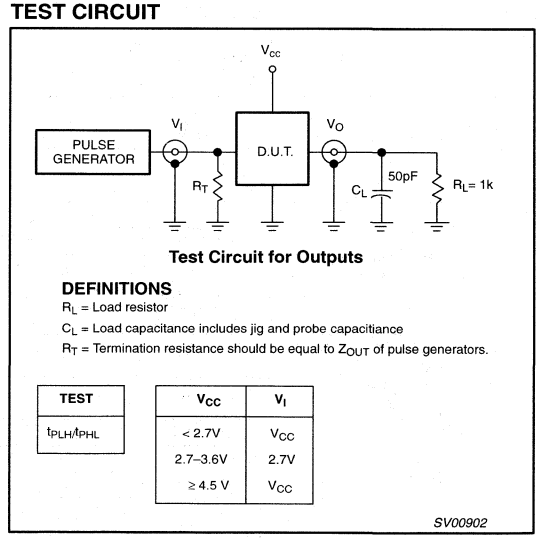


Figure 2. Load circuitry for switching times.

Quad 2-input NAND gate 74LV03

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Level shifter capability
- Output capability: standard (open drain)
- I_{CC} category: SSI

DESCRIPTION

The 74LV03 is a low–voltage Si–gate CMOS device and is pin and function compatible with 74HC/HCT03.

The 74LV03 provides the 2–input NAND function.

The 74LV03 has open–drain N–transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF–state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW–to–HIGH or HIGH–to–LOW level shifter. For digital operation and OR–tied output applications, these devices must have a pull–up resistor to establish a logic HIGH level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZL}/t_{PLZ}	Propagation delay nA, nB to nY	C_L = 15pF V_{CC} = 3.3V	8	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	4	pF

NOTES:

1 C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacitance in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2 The condition is V_I = GND to V_{CC}
3 The given value of C_{PD} is obtained with : C_L = 0 pF and $R_L = \infty$

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV03 N	74LV03 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV03 D	74LV03 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV03 DB	74LV03 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV03 PW	74LV03PW DH	SOT402-1

PIN DESCRIPTION

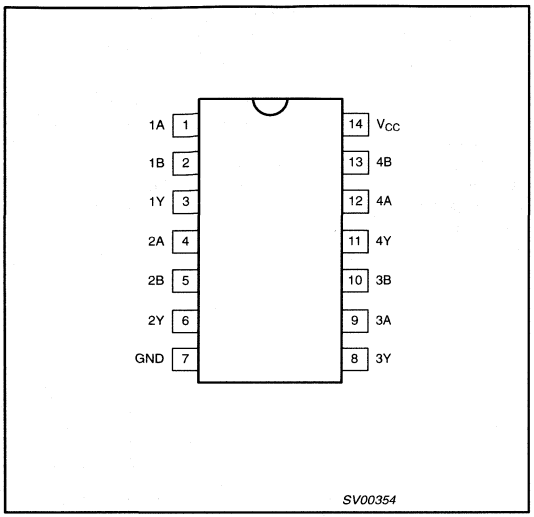
PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

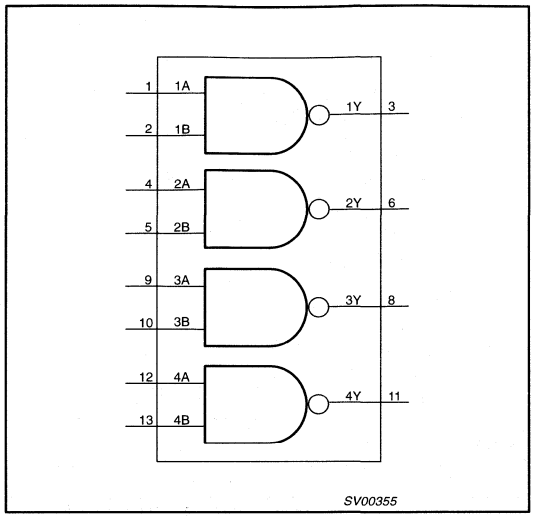
INPUTS		OUTPUT
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
Z = High impedance OFF-state

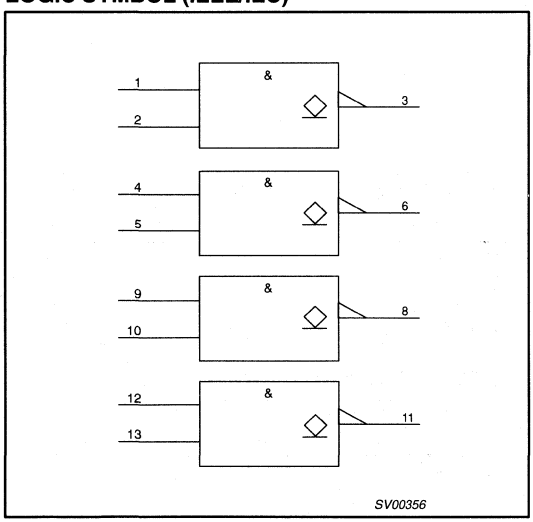
PIN CONFIGURATION



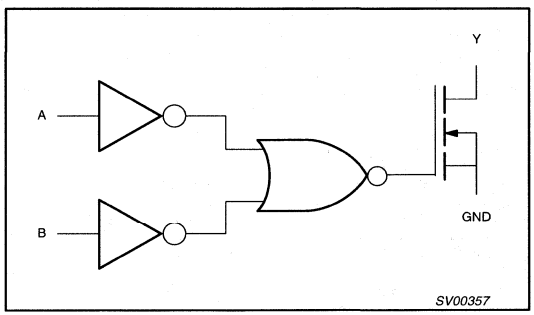
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTES:
1 The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_{OZ}	HIGH level output leakage current	V_{CC} = 2.0 to 3.6V; $V_I = V_{IL}$; $V_O = V_{CC}$ or GND			5.0		10	µA
I_{OZ}	HIGH level output leakage current	V_{CC} = 2.0 to 3.6V; $V_I = V_{IL}$; V_O = 6.0V[2]			10		20	µA
I_I	Input leakage current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V			500		850	µA

NOTES:

1 All typical values are measured at T_{amb} = 25°C.

2 The maximum operating output voltage ($V_{O(max)}$) is 6.0V.

AC CHARACTERISTICS FOR 74LV03

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PZL}/t_{PLZ}	Propagation delay nA, nB, to nY	Figures, 1, 2	1.2	–	50	–	–	–	ns
			2.0	–	17	26	–	31	
			2.7	–	13	19	–	23	
			3.0 to 3.6	–	10[2]	16	–	19	
			4.5 to 5.5	–	–[3]	13	–	16	

NOTE:

1 Unless otherwise stated, all typical values are at T_{amb} = 25°C.

2 Typical value measured at V_{CC} = 3.3V.

3 Typical value measured at V_{CC} = 5.0V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq 2.7V \leq 3.6V$

V_M = 0.5V * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq 2.7V \leq 3.6V$

$V_X = V_{OL}$ + 0.1 * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V

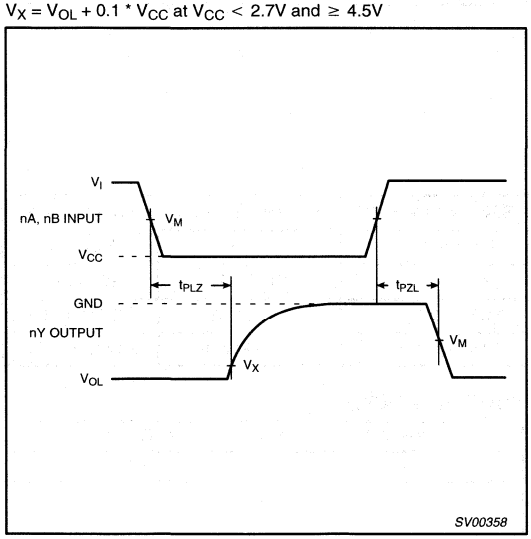
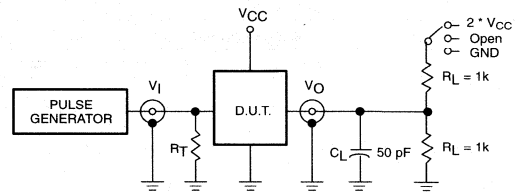


Figure 1. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitiance.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5V	V_{CC}

SV00896

Figure 2. Load circuitry for switching times

Hex inverter 74LV04

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV04 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT04.

The 74LV04 provides six inverting buffers.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 15 pF; V_{CC} = 3.3 V	6	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	21	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_1 is V_1 = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV04 N	74LV04 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV04 D	74LV04 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV04 DB	74LV04 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV04 PW	74LV04PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 3, 5, 9, 11, 13	1A – 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y – 6Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

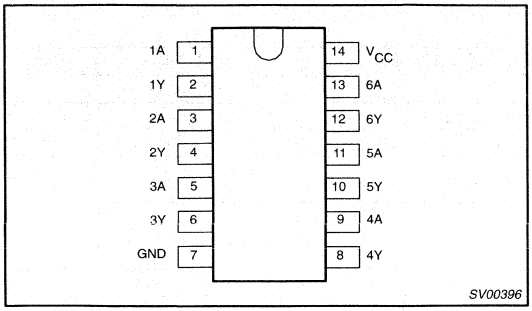
FUNCTION TABLE

INPUTS	OUTPUTS
nA	nY
L	H
H	L

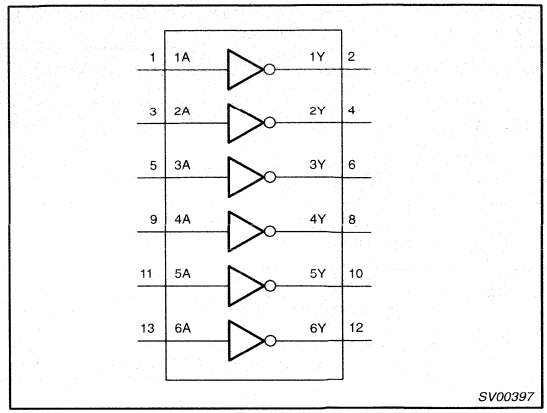
NOTES:

H = HIGH voltage level
L = LOW voltage level

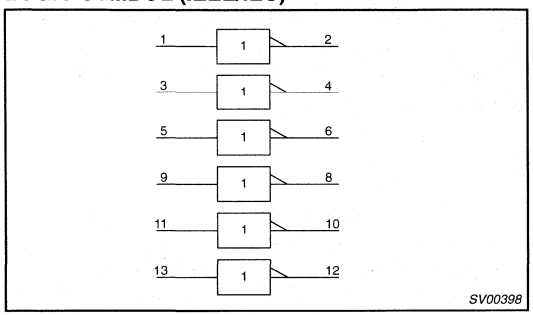
PIN CONFIGURATION



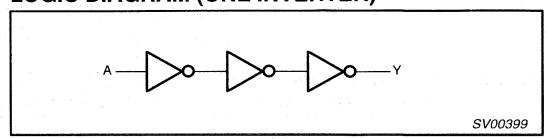
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE INVERTER)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP.[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP.[1]	MAX	MIN	MAX	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85°C			–40 to +125°C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA to nY	Figure 1	1.2		40				ns
			2.0		14	20		25	
			2.7		10	15		19	
			3.0 to 3.6		8[2]	12		15	
			4.5 to 5.5			9		11	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V and $\geq$ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

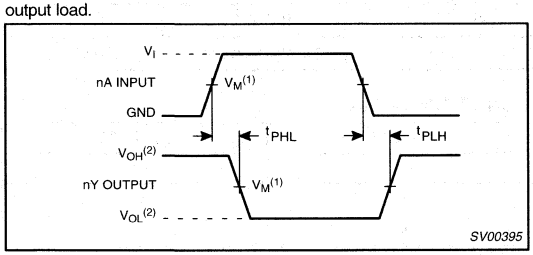
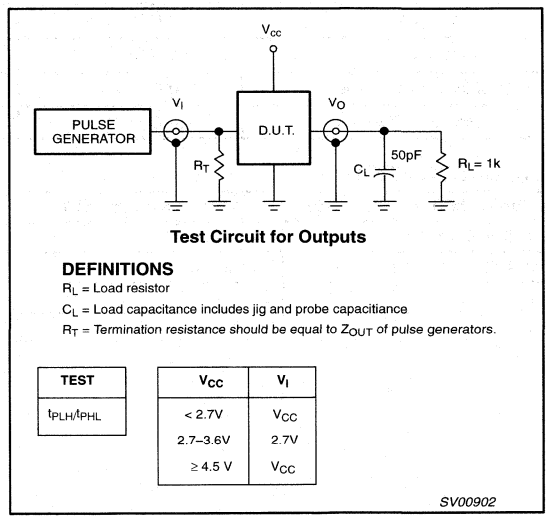


Figure 1. Input (nA) to output (nY) propagation delays and output transition times.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitiance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V
	≥ 4.5 V	V_{CC}

Figure 2. Load circuitry for switching times

Hex inverter | 74LVU04

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LVU04 is a low-voltage, Si-gate CMOS device and is pin compatible with the 74HCU04.

The 74LVU04 is a general purpose hex inverter. Each of the six inverters is a single stage with unbuffered outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 15 pF; V_{CC} = 3.3 V	6	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	18	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LVU04 N	74LVU04 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LVU04 D	74LVU04 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LVU04 DB	74LVU04 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LVU04 PW	74LVU04PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A – 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y – 6Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

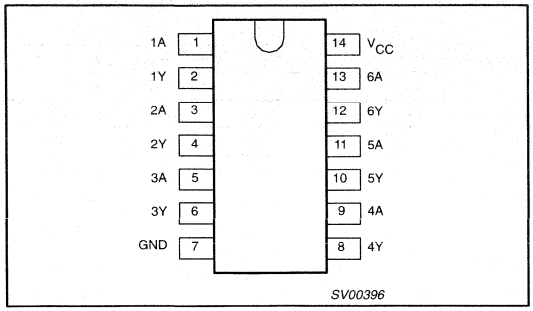
FUNCTION TABLE

INPUTS	OUTPUTS
nA	nY
L	H
H	L

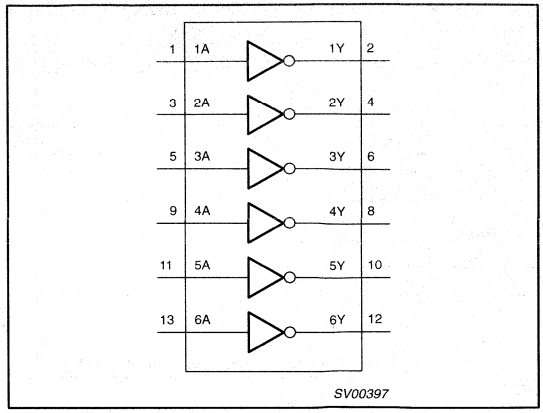
NOTES:

H = HIGH voltage level
L = LOW voltage level

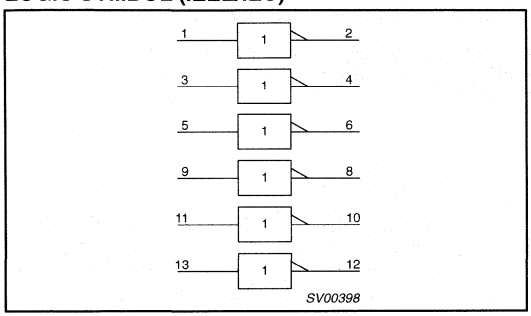
PIN CONFIGURATION



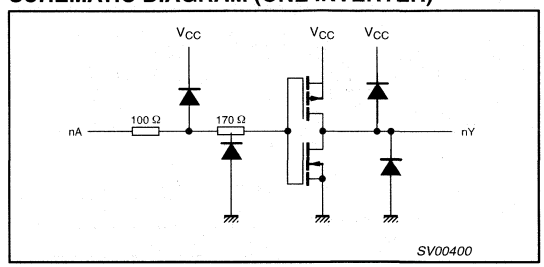
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



SCHEMATIC DIAGRAM (ONE INVERTER)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTE:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	1.0			1.0		V
		V_{CC} = 2.0V	1.6			1.6		
		V_{CC} = 2.7 to 3.6V	2.4			2.4		
		V_{CC} = 4.5 to 5.5V	0.8 * V_{CC}			0.8 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.2		0.2	V
		V_{CC} = 2.0V			0.4		0.4	
		V_{CC} = 2.7 to 3.6V			0.5		0.5	
		V_{CC} = 4.5 to 5.5			0.2 * V_{CC}		0.2 * V_{CC}	
V_{OH}	HIGH level output voltage	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{OL}	LOW level output voltage	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
$\pm I_I$	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40.0	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} −0.6V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
$t_{PHL/PLH}$	Propagation delay nA to nY	Figure 1	1.2		35				ns
			2.0		12	14		17	
			2.7		9	10		13	
			3.0 to 3.6		7[2]	8		10	
			4.5 to 5.5			7		9	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V and ≤ 3.6 V
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V and ≥ 4.5 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

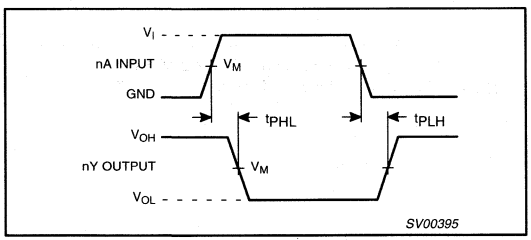


Figure 1. Input (nA) to output (nY) propagation delays and output transition times.

TYPICAL TRANSFER CHARACTERISTICS

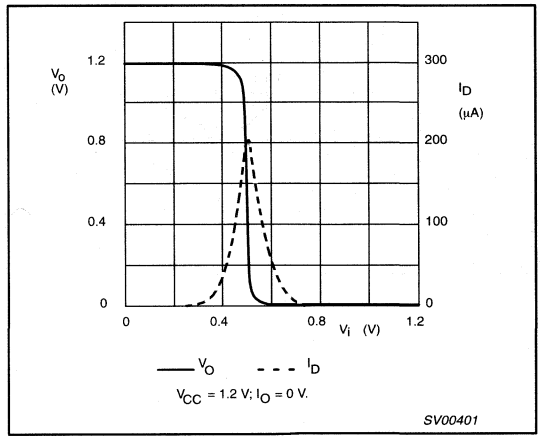


Figure 2.

TYPICAL TRANSFER CHARACTERISTICS (*Continued*)

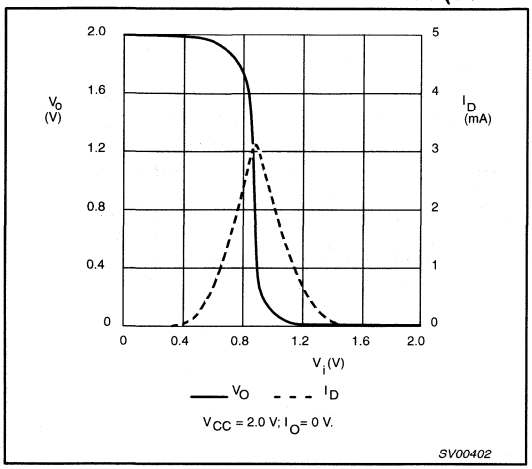


Figure 3.

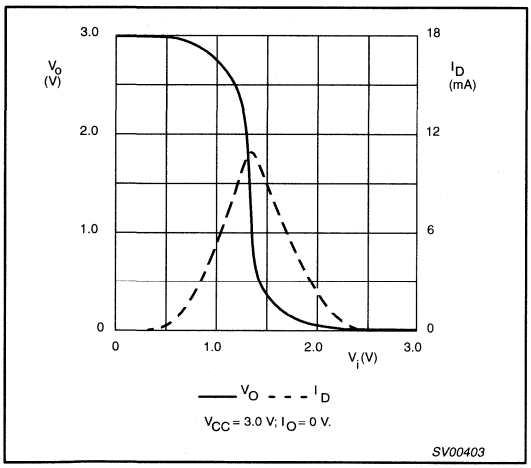


Figure 4.

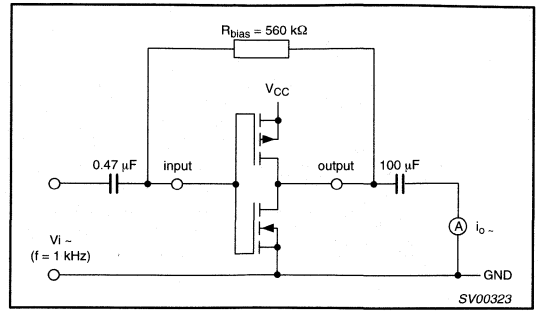


Figure 5. Test set-up for measuring forward transconductance $g_{fs} = di_O/dv_I$ at v_O is constant (see also graph Figure 6).

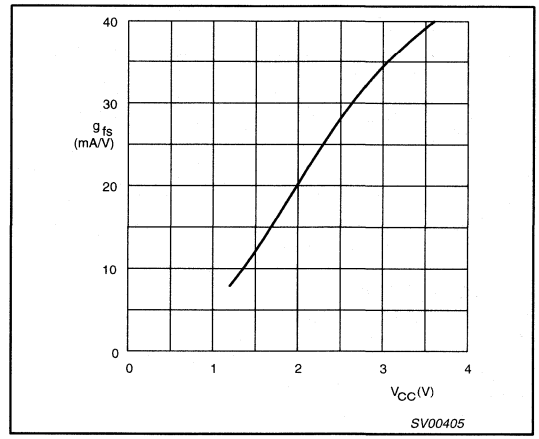


Figure 6. Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25°C.

APPLICATION INFORMATION

Some applications for the 74LVU04 are:

- Linear amplifier (see Figure 7)
- In crystal oscillator designs (see Figure 8)
- Astable multivibrator (see Figure 9)

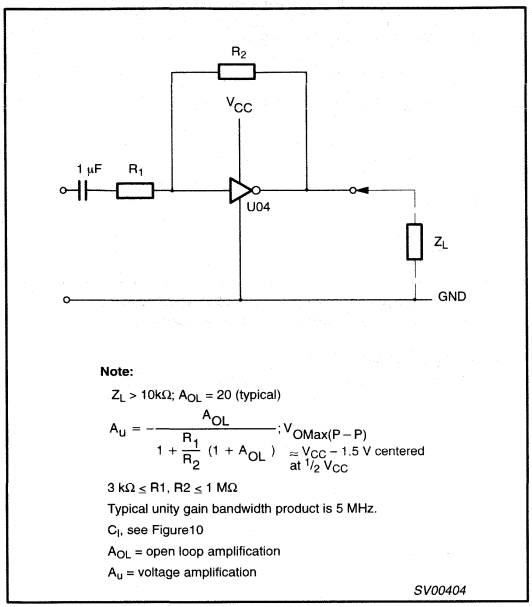


Figure 7. LVU04 used as a linear amplifier.

EXTERNAL COMPONENTS FOR RESONATOR (f < 1 mHz)

FREQUENCY (kHz)	R_1(MΩ)	R_2 (KΩ)	C_1 (pF)	C_2 (pF)
10 .. 15.9	2.2	220	56	20
16 .. 24.9	2.2	220	56	10
25 .. 54.9	2.2	100	56	10
55 .. 129.9	2.2	100	47	5
130 .. 199.9	2.2	47	47	5
200 .. 349.9	2.2	47	47	5
350 .. 600	2.2	47	47	5

WHERE:
All values given are typical and must be used as an initial set-up.

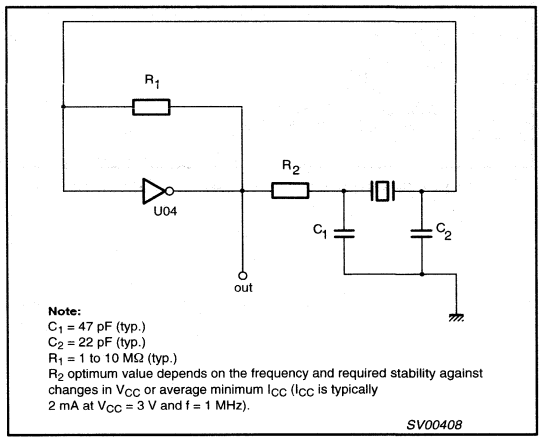


Figure 8. Crystal oscillator configuration.

OPTIMUM VALUE FOR R_2

FREQUENCY (MHz)	R_2 (kΩ)	Optimum
3	2.0 8.0	Minimum required I_{CC} Minimum influence due to change in V_{CC}
6	1.0 4.7	Minimum I_{CC} Minimum influence by V_{CC}
10	0.5 2.0	Minimum I_{CC} Minimum influence by V_{CC}
14	0.5 1.0	Minimum I_{CC} Minimum influence by V_{CC}
> 14	Replace R_2 by C_3 with a typical value of 35 pF	

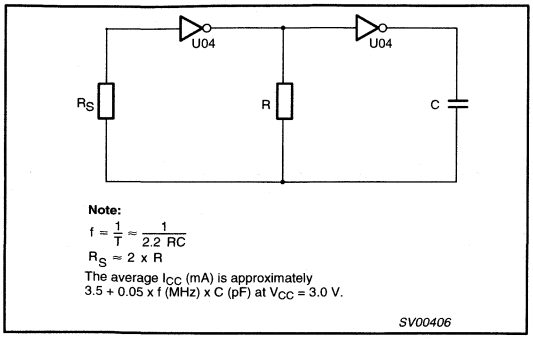


Figure 9. LVU04 used as an astable multivibrator.

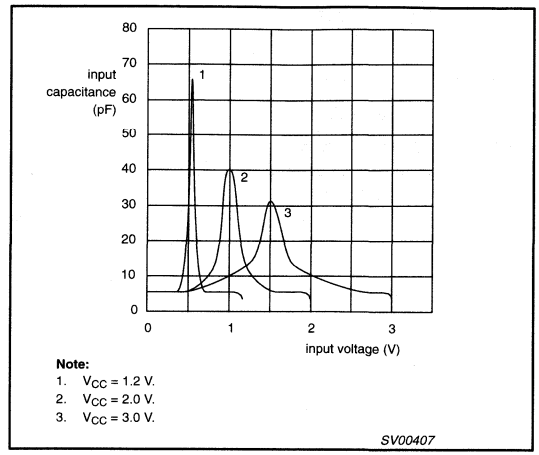


Figure 10. Typical input capacitance as function of input voltage.

Note for Application Information
All values given are typical unless otherwise specified.

Quad 2-input AND gate 74LV08

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV08 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT08.

The 74LV08 provides the 2-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 3.3 V	7	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	10	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV08 N	74LV08 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV08 D	74LV08 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV08 DB	74LV08 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV08 PW	74LV08PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1Y – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

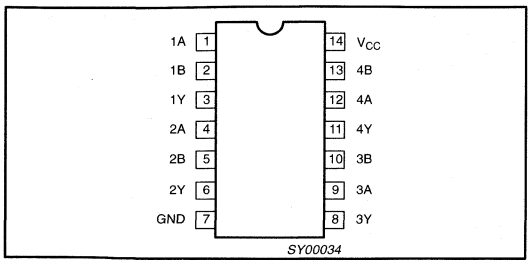
FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

NOTES:

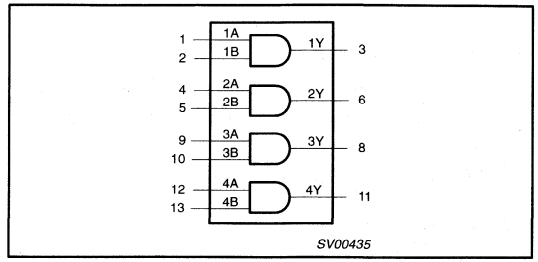
H = HIGH voltage level
L = LOW voltage level

PIN CONFIGURATION



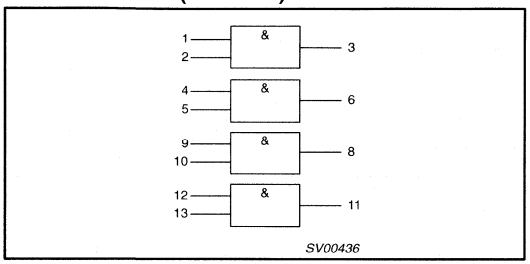
SY00034

LOGIC SYMBOL



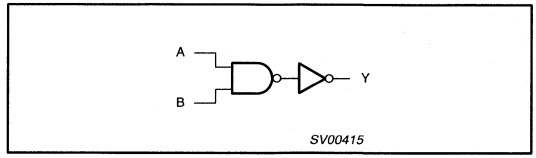
SV00435

LOGIC SYMBOL (IEEE/IEC)



SV00436

LOGIC DIAGRAM (ONE GATE)



SV00415

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP.[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	$0.7*V_{CC}$			$0.7*V_{CC}$		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			$0.3*V_{CC}$		$0.3*V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP.[1]	MAX	MIN	MAX	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	Figures 1, 2	1.2		45				ns
			2.0		15	26		33	
			2.7		11	17		21	
			3.0 to 3.6		9[2]	15		19	
			4.5 to 5.5			11		14	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C.
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V and ≤ 3.6 V;
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V and ≥ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

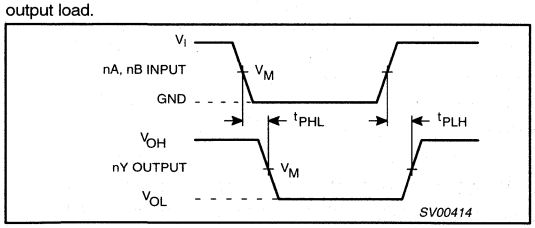
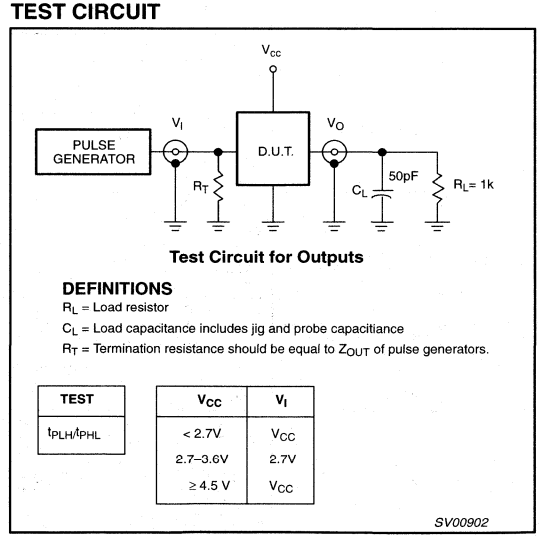


Figure 1. Input (nA, nB) to output (nY) propagation delays and output transition times.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V
	≥ 4.5 V	V_{CC}

Figure 2. Load circuitry for switching times.

Triple 3-input NAND gate 74LV10

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV10 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT10.

The 74LV10 provides the 3-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 3.3 V	9	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	12	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV10 N	74LV10 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV10 D	74LV10 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV10 DB	74LV10 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV10 PW	74LV10PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
13, 5, 11	1C – 3C	Data inputs
14	V_{CC}	Positive supply voltage

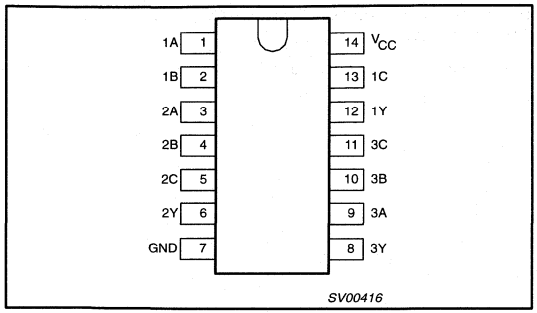
FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

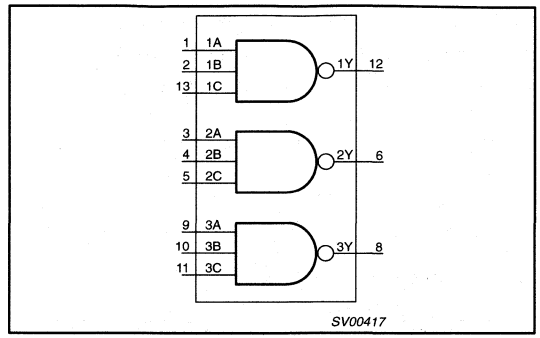
NOTES:

H = HIGH voltage level
L = LOW voltage level

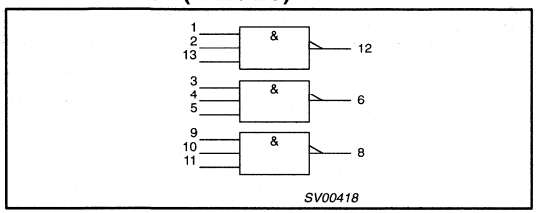
PIN CONFIGURATION



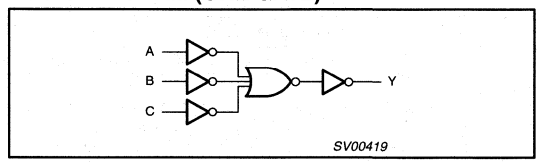
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		40	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V			500		850	μA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
$t_{PHL/PLH}$	Propagation delay nA, nB, nC to nY	Figure 1, 2	1.2		55				ns
			2.0		19	36		44	
			2.7		14	26		33	
			3.0 to 3.6		10[2]	21		26	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C.
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

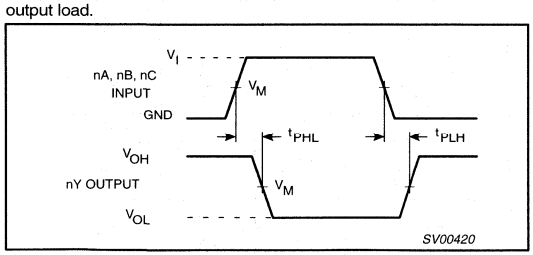
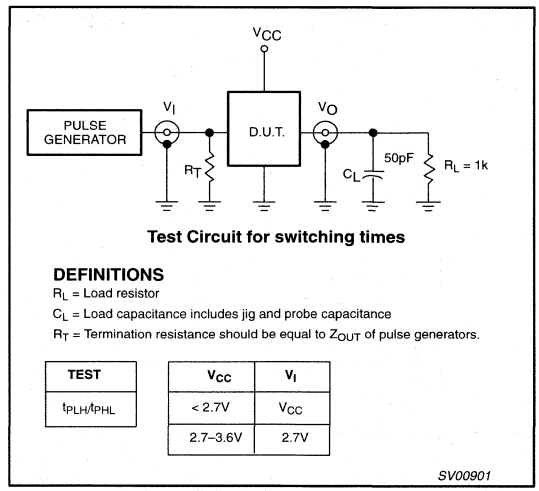


Figure 1. Input (nA, nB, nC) to output (nY) propagation delays.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V

Figure 2. Load circuitry for switching times.

Triple 3-input AND gate 74LV11

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV11 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT11.

The 74LV11 provides the 3-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 3.3 V	10	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	18	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV11 N	74LV11 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV11 D	74LV11 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV11 DB	74LV11 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV11 PW	74LV11PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
13, 5, 11	1C – 3C	Data inputs
14	V_{CC}	Positive supply voltage

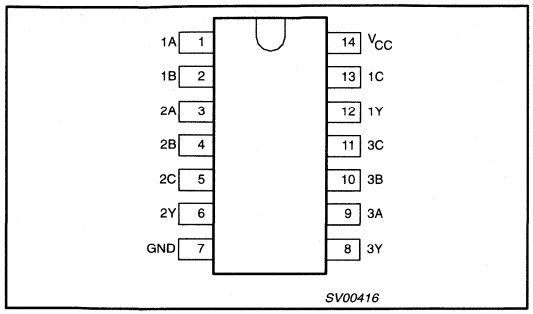
FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

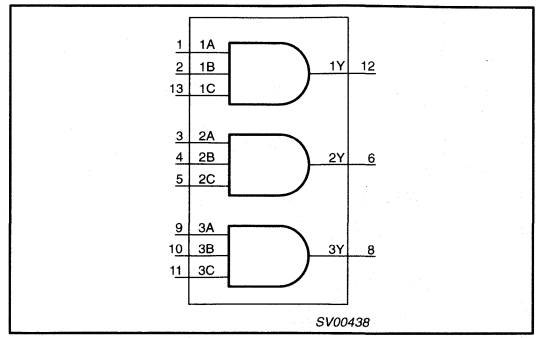
NOTES:

H = HIGH voltage level
L = LOW voltage level

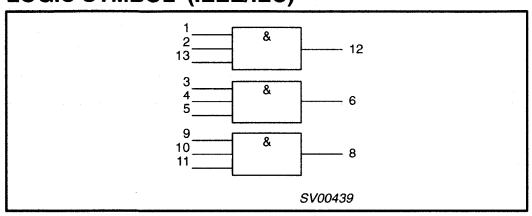
PIN CONFIGURATION



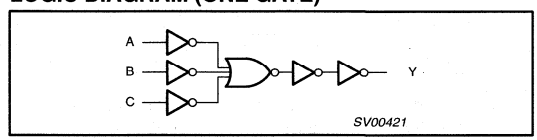
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			1.0		1.0	µA

DC CHARACTERISTICS FOR THE LV FAMILY (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
I_{CC}	Quiescent supply current; SSI	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0			20.0		40	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	μA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
$t_{PHL/PLH}$	Propagation delay nA, nB, nC to nY	Figures 1, 2	1.2		60				ns
			2.0		20	39		46	
			2.7		15	29		34	
			3.0 to 3.6		11[2]	23		27	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C.
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

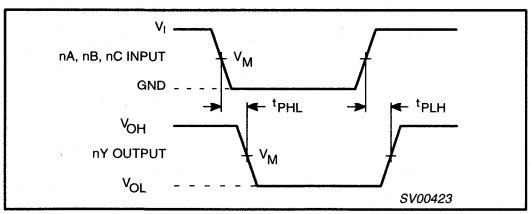


Figure 1. Input (nA, nB, nC) to output (nY) propagation delays.

TEST CIRCUIT

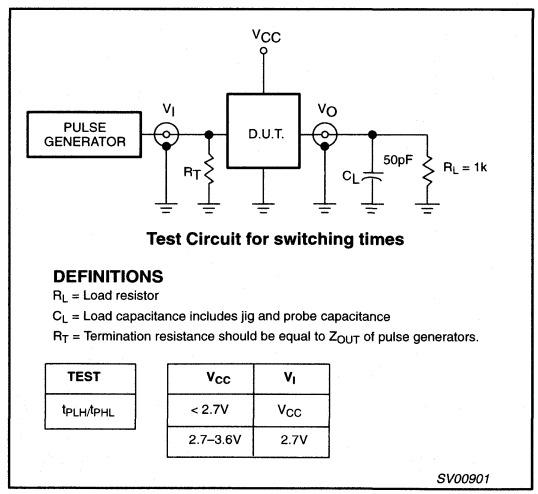


Figure 2. Load circuitry for switching times.

Hex inverting Schmitt-trigger 74LV14

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Output capability: standard
- I_{CC} category: SSI

APPLICATIONS

- Wave and pulse shapers for highly noisy environments

DESCRIPTION

The 74LV14 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT14.

The 74LV14 provides six inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 15 pF; V_{CC} = 3.3 V	13	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	15	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV14 N	74LV14 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV14 D	74LV14 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV14 DB	74LV14 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV14 PW	74LV14PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A – 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y – 6Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

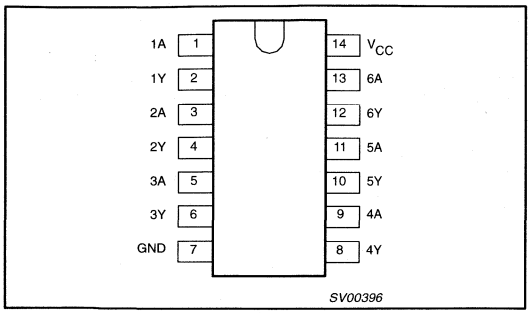
FUNCTION TABLE

INPUT	OUTPUT
nA	**nY**
L	H
H	L

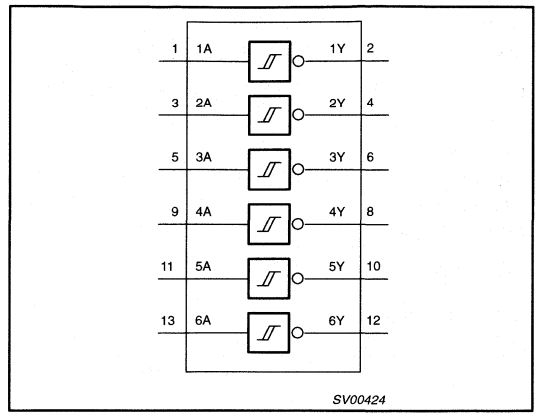
NOTES:

H = HIGH voltage level
L = LOW voltage level

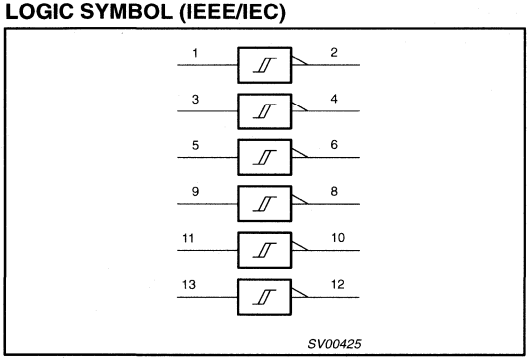
PIN CONFIGURATION



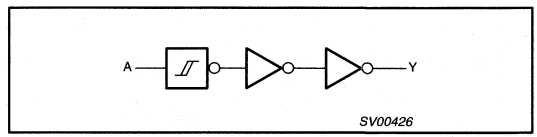
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC} - 0.6V$			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

TRANSFER CHARACTERISTICS

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS	
		−40 TO +85			−40 TO +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MIN.			
V_{T+}	Positive-going threshold	–	0.70	–	–	–	V	1.2	Figure 1 and 2
		0.8	1.10	1.4	0.8	1.4		2.0	
		1.0	1.45	2.0	1.0	2.0		2.7	
		1.2	1.60	2.2	1.2	2.2		3.0	
		1.5	1.95	2.4	1.5	2.4		3.6	
		1.7	2.50	3.15	1.7	3.15		4.5	
		2.1	3.00	3.85	2.1	3.85		5.5	
V_{T-}	Negative-going threshold	–	0.34	–	–	–	V	1.2	Figure 1 and 2
		0.3	0.65	0.9	0.3	0.9		2.0	
		0.4	0.90	1.4	0.4	1.4		2.7	
		0.6	1.05	1.5	0.6	1.5		3.0	
		0.8	1.30	1.8	0.8	1.8		3.6	
		0.9	1.60	2.0	0.9	2.0		4.5	
		1.1	2.00	2.6	1.1	2.6		5.5	
V_H	Hysteresis ($V_{T+} - V_{T-}$)	–	0.30	–	–	–	V	1.2	Figure 1 and 2
		0.2	0.55	0.8	0.2	0.8		2.0	
		0.3	0.60	1.1	0.3	1.1		2.7	
		0.4	0.65	1.2	0.4	1.2		3.0	
		0.4	0.70	1.2	0.4	1.2		3.6	
		0.4	0.80	1.4	0.4	1.4		4.5	
		0.6	1.00	1.5	0.6	1.5		5.5	

NOTES:
1. All typical values are measured at T_{amb} = 25°C
2. The V_{IH} and V_{IL} from the DC family characteristics are superseded by the V_{T+} and V_{T-}.

AC CHARACTERISTICS

GND = 0V; $t_r \leq t_f$ = 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
$t_{PHL/PLH}$	Propagation delay nA to nY	Figure 6	1.2		80				ns
			2.0		27	37		48	
			2.7		20	28		35	
			3.0 to 3.6		15[2]	22		28	
			4.5 to 5.5			18		23	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

TRANSFER CHARACTERISTIC WAVEFORMS

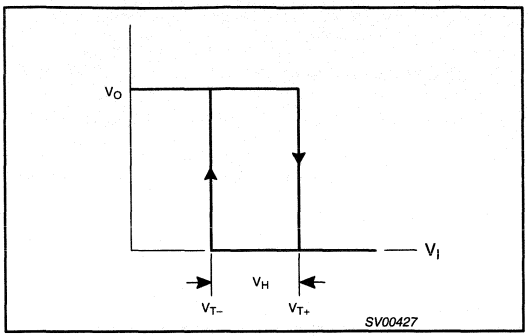


Figure 1. Transfer characteristic.

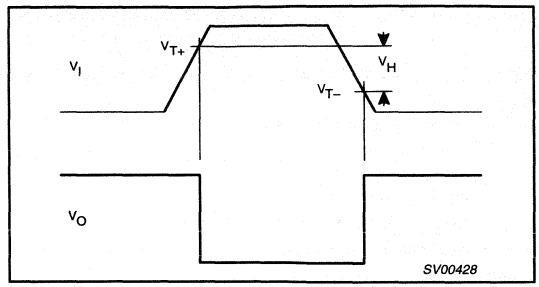


Figure 2. Definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%

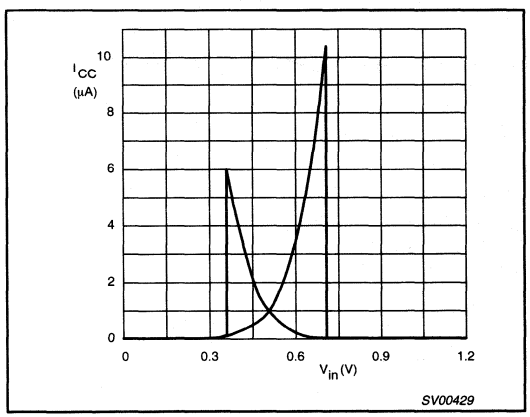


Figure 3. Typical 74LV14 transfer characteristics; V_{CC} = 1.2V.

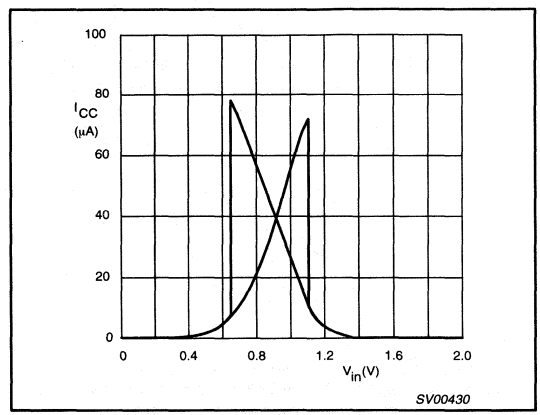


Figure 4. Typical 74LV14 transfer characteristics; V_{CC} = 2.0V.

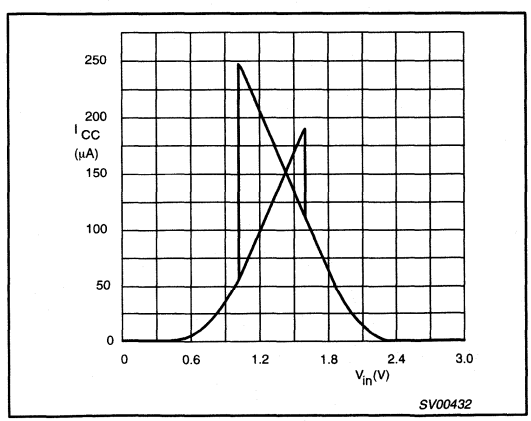


Figure 5. Typical 74LV14 transfer characteristics; V_{CC} = 3.0V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

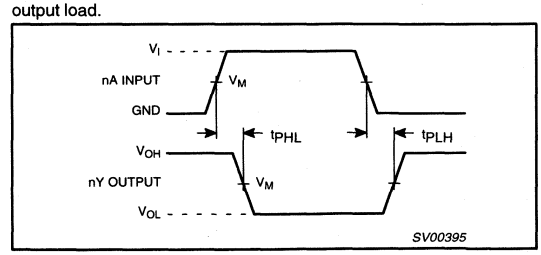


Figure 6. Input (nA) to output (nY) propagation delays.

APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$.

Where:

P_{ad} = additional power dissipation (μW)
f_i = input frequency (MHz)
t_r = input rise time (ns); 10% – 90%
t_f = input fall time (ns); 10% – 90%
I_{CCa} = average additional supply current (μA)

Average I_{CCa} differs with positive or negative input transitions, as shown in Figure 7.

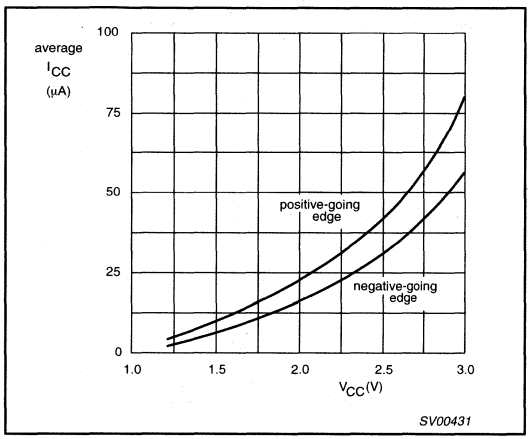


Figure 7. Average I_{CC} for LV Schmitt-trigger devices; linear change of V_I between 0.1 V_{CC} to 0.9 V_{CC}.

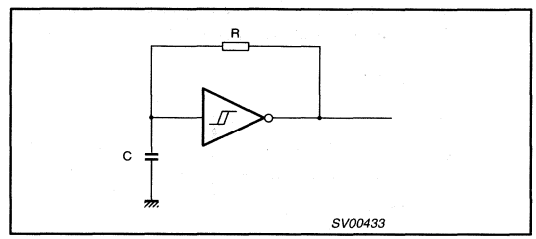


Figure 8. Relaxation oscillator using the LV14.

Note to application information:

All values given are typical unless otherwise specified.

Note to Figure 8

$$f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$$

Dual 4-input NAND gate 74LV20

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV20 is a low–voltage Si–gate CMOS device and is pin and function compatible with 74HC/HCT20.

The 74LV20 provides the 4–input NAND function.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC, nD to nY	C_L = 15pF; V_{CC} = 3.3V	8	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	22	pF

NOTES:

1 C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacitance in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2 The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV20 N	74LV20 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV20 D	74LV20 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV20 DB	74LV20 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV20 PW	74LV20PW DH	SOT402-1

PIN DESCRIPTION

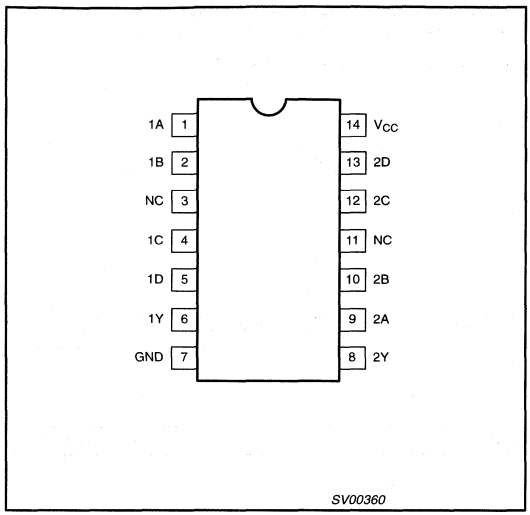
PIN NUMBER	SYMBOL	FUNCTION
1, 9	1A to 2A	Data inputs
2, 10	1B to 2B	Data inputs
3, 11	NC	No connection
4, 12	1C to 2C	Data inputs
5, 13	1D to 2D	Data inputs
6, 8	1Y to 2Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

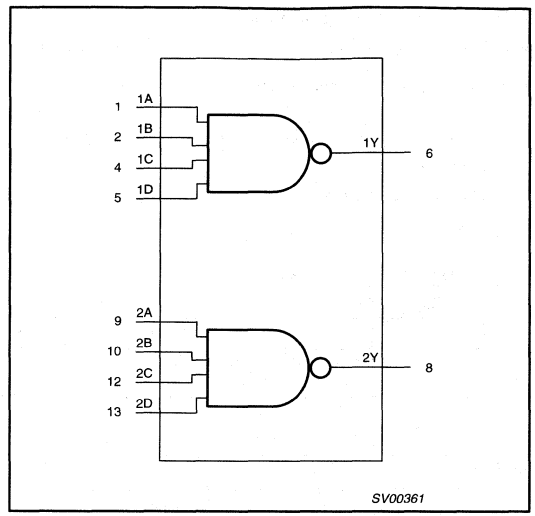
INPUTS				OUTPUTS
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care

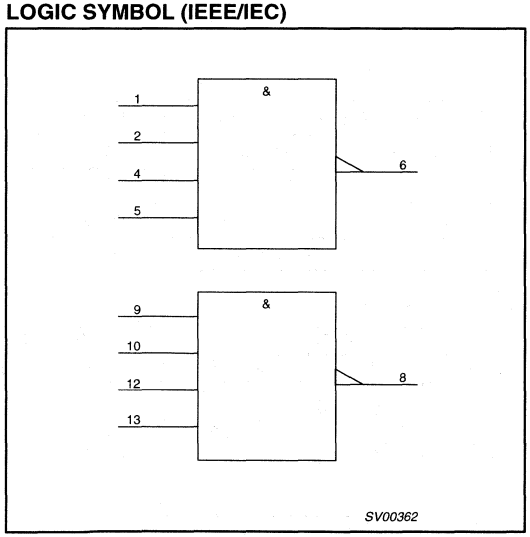
PIN CONFIGURATION



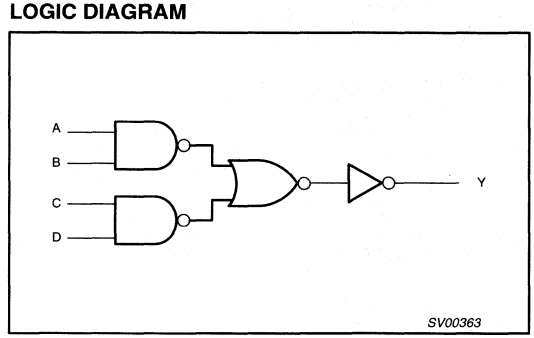
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – – –	500 200 100	ns/V

NOTES:
1 The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V;$V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V;$V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V			500		850	µA

NOTE:

1 All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq$ 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC, nD to nY	Figures 1, 2	1.2	–	50	–	–	–	ns
			2.0	–	17	32	–	39	
			2.7	–	13	24	–	29	
			3.0 to 3.6	–	10[2]	19	–	23	

NOTE:

1 Unless otherwise stated, all typical values are at T_{amb} = 25°C.

2 Typical value measured at V_{CC} = 3.3V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V $\leq$ 3.6V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

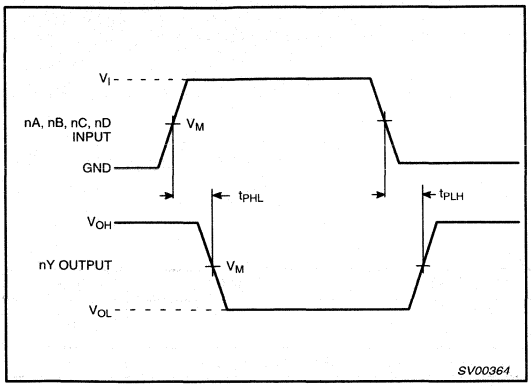
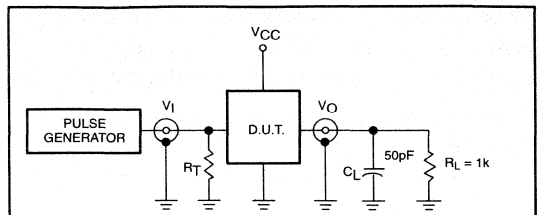


Figure 1.Input (nA, nB, nC, nD) to output (nY) propagation delays.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V

SV00901

Figure 2. Load circuitry for switching times

Triple 3-input NOR gate 74LV27

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV27 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT27.

The 74LV27 provides the 3-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	C_L = 15 pF; V_{CC} = 3.3 V	8	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	24	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV27 N	74LV27 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV27 D	74LV27 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV27 DB	74LV27 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV27 PW	74LV27PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
13, 5, 11	1C – 3C	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
14	V_{CC}	Positive supply voltage

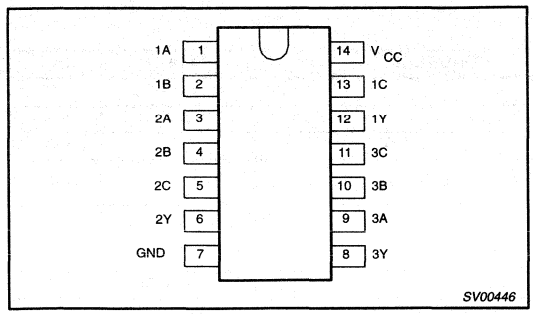
FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

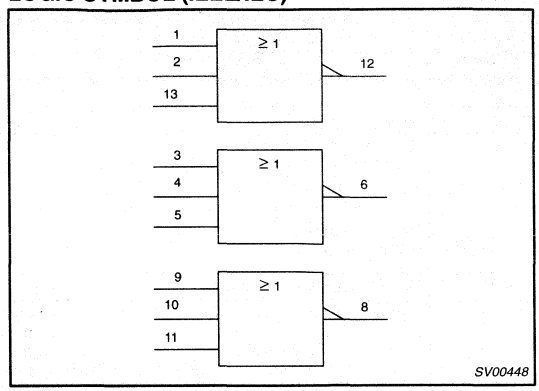
NOTES:

H = HIGH voltage level
L = LOW voltage level
X = don't care

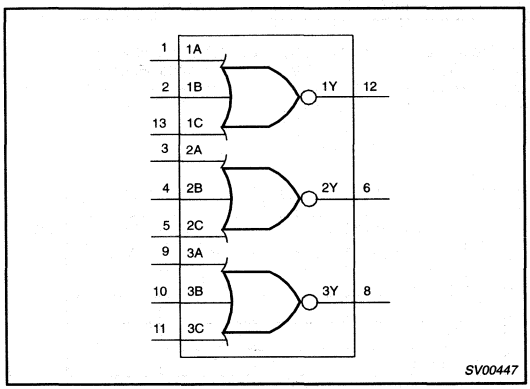
PIN CONFIGURATION



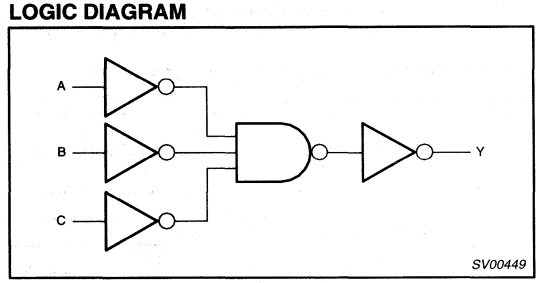
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND			1.0		1.0	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq$ 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
$t_{PHL/PLH}$	Propagation delay nA, nB, nC to nY	Figures 1, 2	1.2		50				ns
			2.0		17	22		27	
			2.7		13	16		20	
			3.0 to 3.6		10[2]	13		16	
			4.5 to 5.5			11		14	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V and $\geq$ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

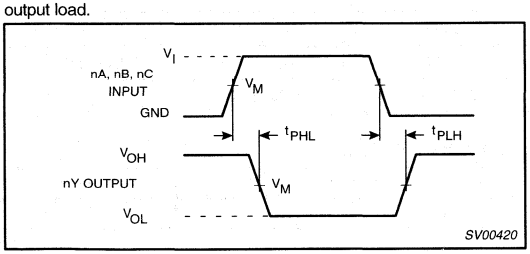
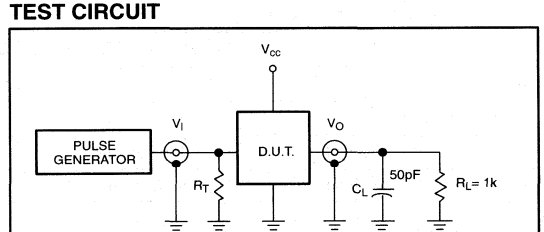


Figure 1. Input (nA, nB, nC) to output (nY) propagation delays.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitiance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V
	≥ 4.5 V	V_{CC}

SV00902

Figure 2. Load circuitry for switching times.

Quad 2-input OR gate | 74LV32

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{AMB} = 25°C.
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV32 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT32.

The 74LV32 provides the 2-input OR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 3.3 V	6	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC} [1]	16	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV32 N	74LV32 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV32 D	74LV32 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV32 DB	74LV32 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV32 PW	74LV32PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data Outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

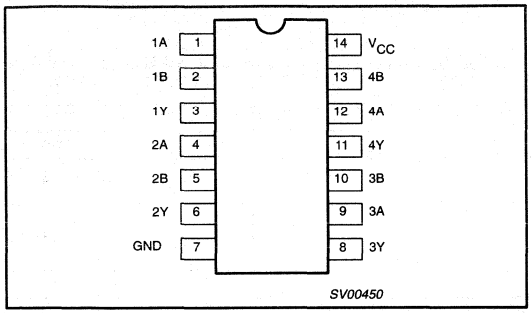
FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

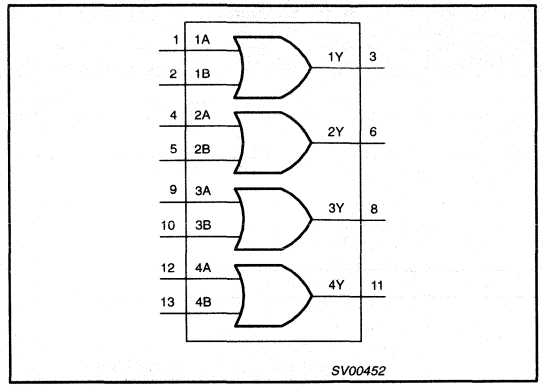
H = HIGH voltage level
L = LOW voltage level

Quad 2-input OR gate 74LV32

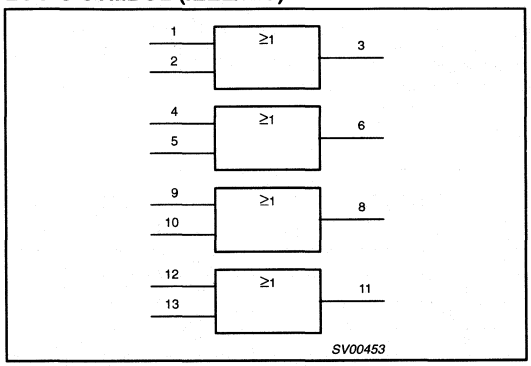
PIN CONFIGURATION



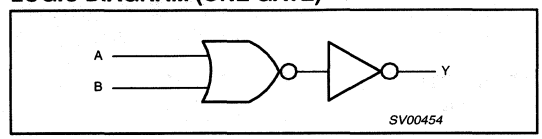
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTE:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}	0.6		V_{CC}		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V		0.4	GND		GND	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND			1.0		1.0	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTES:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
$t_{PHL/PLH}$	Propagation delay nA, nB to nY	Figures 1, 2	1.2		40				ns
			2.0		14	22		28	
			2.7		10	16		20	
			3.0 to 3.6		8[2]	13		16	
			4.5 to 5.5			10		13	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V and ≤ 3.6 V;
V_M = 0.5 V × V_{CC} at V_{CC} < 2.7 V and ≥ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

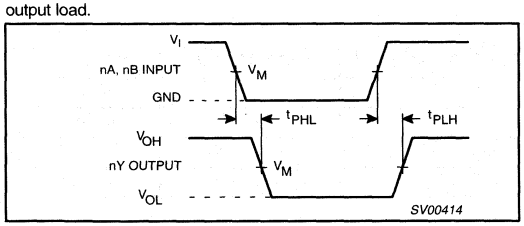
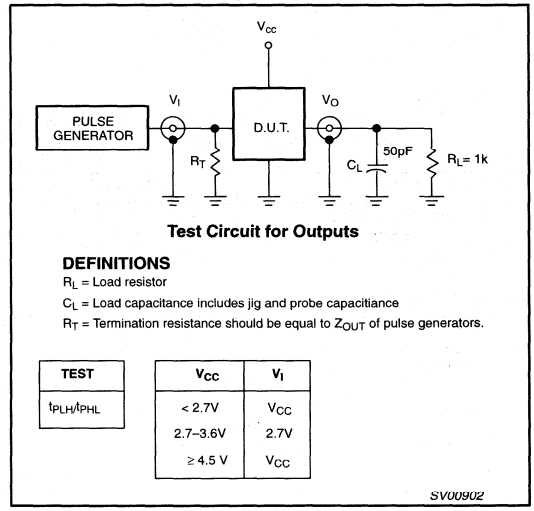


Figure 1. Input (nA, nB) to output (nY) propagation delays and output transition times.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5 V	V_{CC}

Figure 2. Load circuitry for switching times.

Dual D-type flip-flop with set and reset; positive edge-trigger

74LV74

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: flip-flops

DESCRIPTION

The 74LV74 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT74.

The 74LV74 is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15pF V_{CC} = 3.3V	11 14 14	ns
f_{max}	Maximum clock frequency	C_L = 15pF V_{CC} = 3.3V	76	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	24	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV74 N	74LV74 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV74 D	74LV74 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV74 DB	74LV74 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV74 PW	74LV74PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 13	1$\overline{R}_D$, 2$\overline{R}_D$	Asynchronous reset-direct input (active-LOW)
2, 12	1D, 2D	Data inputs
3, 11	1CP, 2CP	Clock input (LOW-to-HIGH), edge-triggered)
4, 10	1$\overline{S}_D$, 2$\overline{S}_D$	Asynchronous set-direct input (active-LOW)
5, 9	1Q, 2Q	True flip-flop outputs
6, 8	1$\overline{Q}$, 2$\overline{Q}$	Complement flip-flop outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

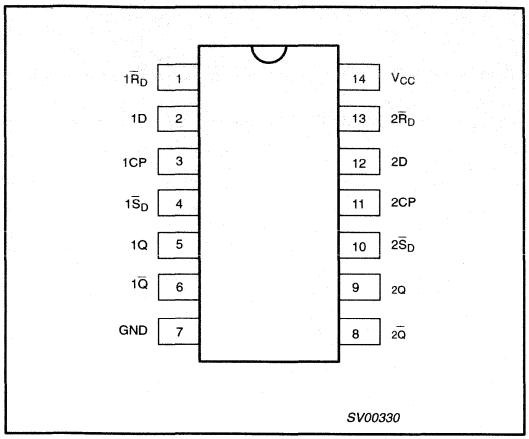
INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

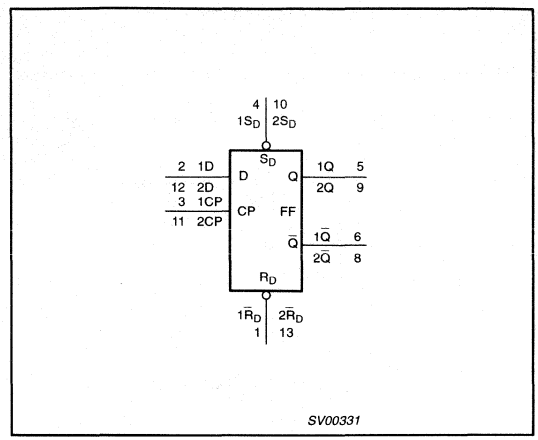
Dual D-type flip-flop with set and reset; positive edge-trigger

74LV74

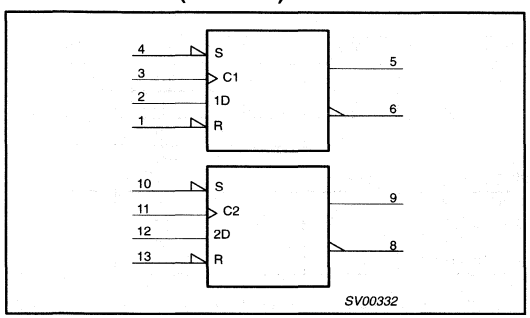
PIN CONFIGURATION



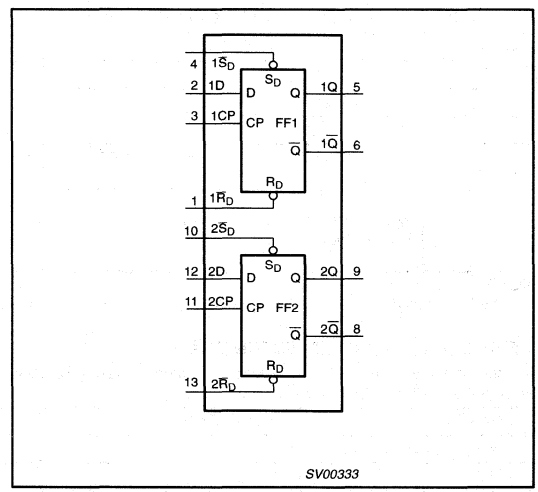
LOGIC SYMBOL



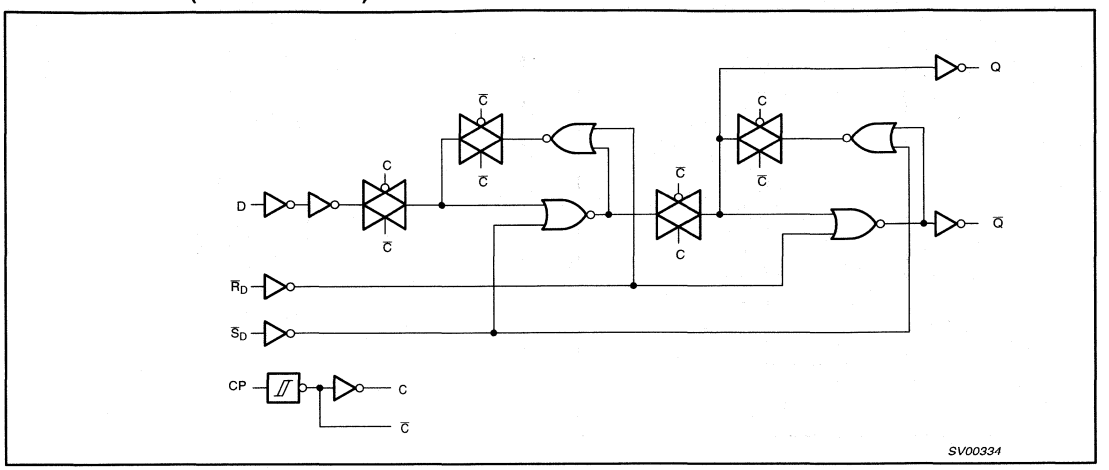
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM (ONE FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; flip-flops	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		80	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} −0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$	Figures, 1, 3	1.2	–	70	–	–	–	ns
			2.0	–	24	44	–	56	
			2.7	–	18	28	–	41	
			3.0 to 3.6	–	13[2]	26	–	33	
			4.5 to 5.5	–	9.5[3]	17	–	23	
t_{PHL}/t_{PLH}	Propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$	Figures 2, 3	1.2	–	90	–	–	–	ns
			2.0	–	31	46	–	58	
			2.7	–	23	34	–	43	
			3.0 to 3.6	–	17[2]	27	–	34	
			4.5 to 5.5	–	12[3]	19	–	24	
t_{PHL}/t_{PLH}	Propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$	Figures 2, 3	1.2	–	90	–	–	–	ns
			2.0	–	31	46	–	58	
			2.7	–	23	34	–	43	
			3.0 to 3.6	–	17[2]	27	–	34	
			4.5 to 5.5	–	12[3]	19	–	24	
t_W	Clock pulse width HIGH to LOW	Figure 1	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	7[2]	–	24	–	
			4.5 to 5.5	15	6[3]	–	18	–	
t_W	Set or reset pulse width LOW	Figure 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	7[2]	–	24	–	
			4.5 to 5.5	15	6[3]	–	18	–	
t_{rem}	Removal time set or reset	Figure 2	1.2	–	5	–	–	–	ns
			2.0	14	2	–	15	–	
			2.7	10	1	–	11	–	
			3.0 to 3.6	8	1[2]	–	9	–	
			4.5 to 5.5	6	1[3]	–	7	–	
t_{su}	Set-up time nD to nCP	Figure 1	1.2	–	10	–	–	–	ns
			2.0	22	4	–	26	–	
			2.7	12	3	–	15	–	
			3.0 to 3.6	8	2[2]	–	10	–	
			4.5 to 5.5	6	1[2]	–	8	–	
t_h	Hold time nD to nCP	Figure 1	1.2	–	–10	–	–	–	ns
			2.0	3	–2	–	3	–	
			2.7	3	–2	–	3	–	
			3.0 to 3.6	3	–2[2]	–	3	–	
			4.5 to 5.5	3	–2[3]	–	3	–	
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40	–	12	–	MHz
			2.7	50	90	–	40	–	
			3.0 to 3.6	60	100[2]	–	48	–	
			4.5 to 5.5	70	110[3]	–	56	–	

NOTE:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25°C$.
2. Typical value measured at $V_{CC} = 3.3$V.
3. Typical value measured at $V_{CC} = 5.0$V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V $\leq$ 3.6V
V_M = 0.5 * V_{CC} at V_{CC} < 2.7V and $\geq$ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

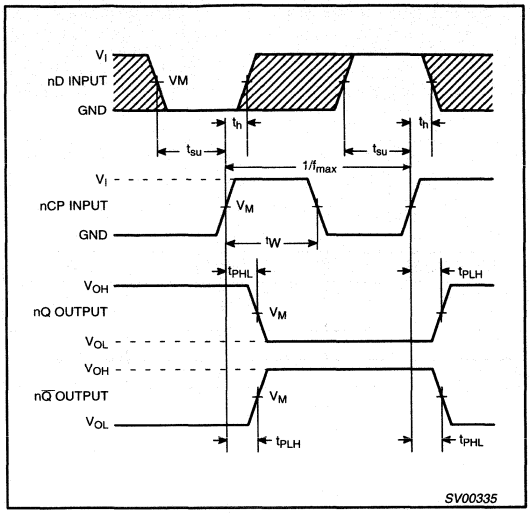


Figure 1.The clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP setup times, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance.

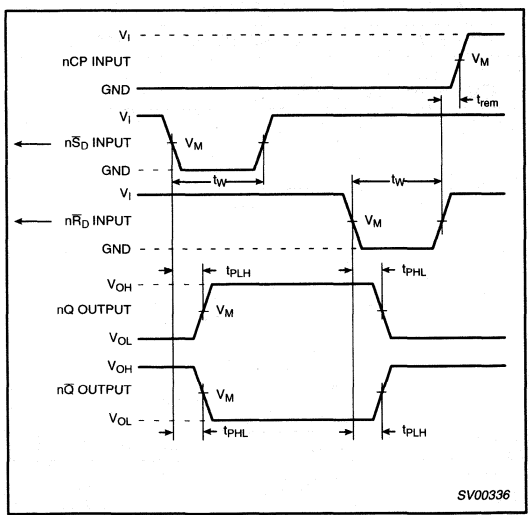


Figure 2.The set (nS̄D) and reset (nR̄D) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nR̄D to nCP removal time

TEST CIRCUIT

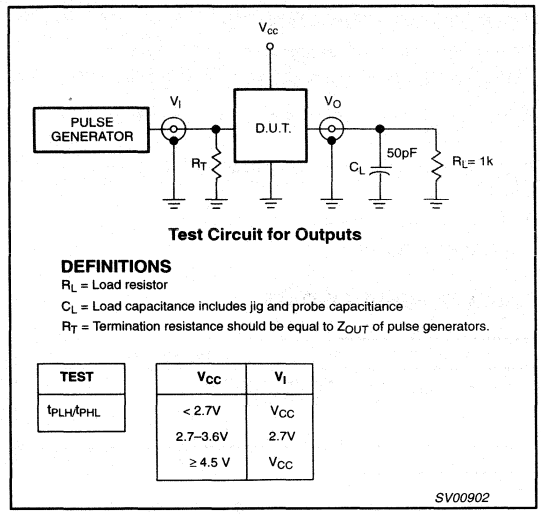


Figure 3. Load circuitry for switching times

Quad 2-input EXCLUSIVE-OR gate 74LV86

FEATURES

- Wide Operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV86 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT86.

The 74LV86 provides the 2-input EXCLUSIVE-OR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 3.3 V	11	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	30	pF

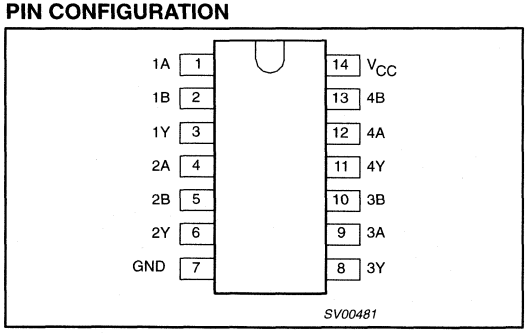
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

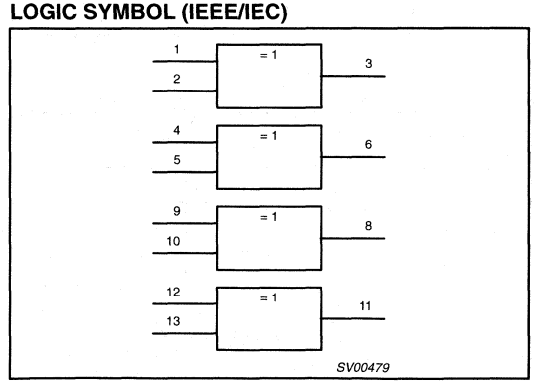
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV86 N	74LV86 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV86 D	74LV86 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV86 DB	74LV86 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV86 PW	74LV86PW DH	SOT402-1

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

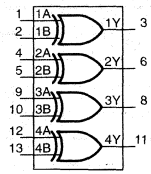
PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

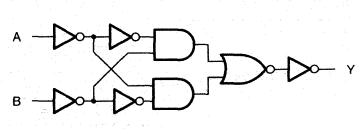
NOTES:
H = HIGH voltage level
L = LOW voltage level

LOGIC SYMBOL



SV00480

LOGIC DIAGRAM (ONE GATE)



SV00478

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0 V V_{CC} = 2.0V to 2.7 V V_{CC} = 2.7V to 3.6 V V_{CC} = 3.6V to 5.5 V			500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5 V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 to 5.5 V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} –0.6 V			500		850	μA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	Figure 1	1.2		70				ns
			2.0		24	32		41	
			2.7		18	24		30	
			3.0 to 3.6		13[2]	19		24	
			4.5 to 5.5			16		20	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C.
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V and $\geq$ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

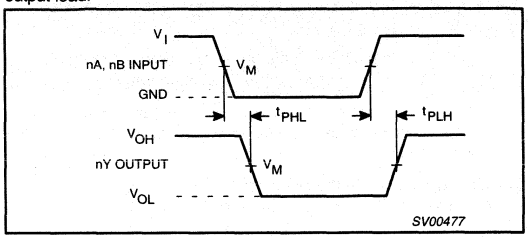


Figure 1. Input (nA, nB) to output (nY) propagation delays and the output transition times.

TEST CIRCUIT

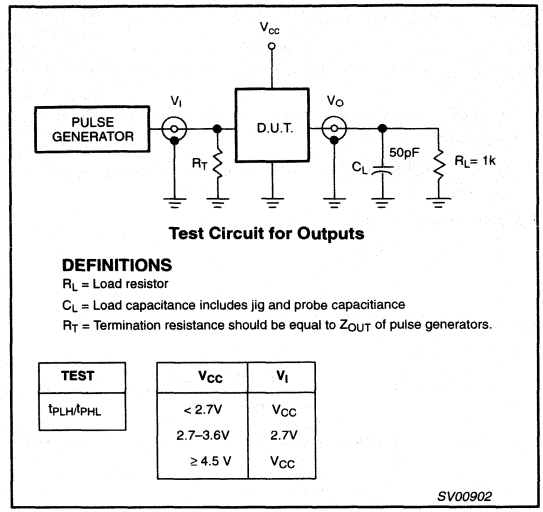


Figure 2. Load circuitry for switching times.

Dual JK flip-flop with reset; negative-edge trigger | 74LV107

FEATURES

- Wide operating: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: flip-flops

DESCRIPTION

The 74LV107 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT107.

The 74LV107 is a dual negative-edge triggered JK-type flip-flop featuring individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ($n\overline{R}$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $n\overline{CP}$ to nQ $n\overline{CP}$ to $n\overline{Q}$ $n\overline{R}$ to nQ, $n\overline{Q}$	C_L = 15 pF; V_{CC} = 3.3 V	 15 15 15	ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_I = GND to V_{CC}[1]	30	pF

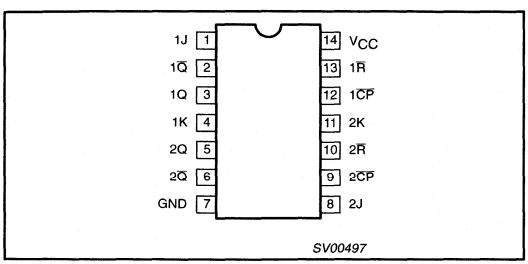
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV107 N	74LV107 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV107 D	74LV107 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV107 DB	74LV107 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV107 PW	74LV107PW DH	SOT402-1

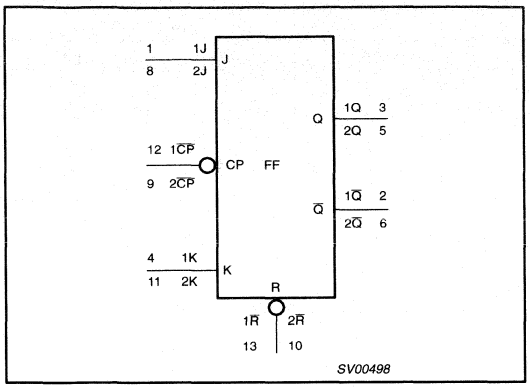
PIN CONFIGURATION



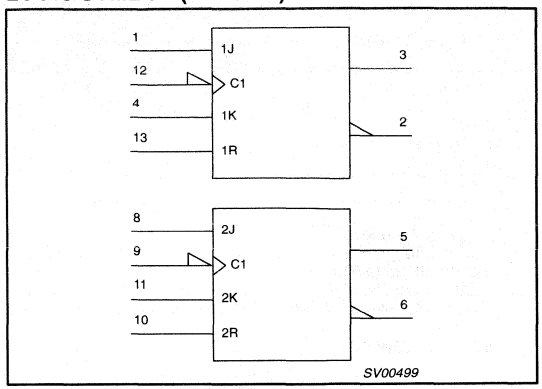
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 8, 4, 11	1J, 2J, 1K, 2K	Synchronous inputs; flip-flops 1 and 2
2, 6	$1\overline{Q}$, $2\overline{Q}$	Complement flip-flop outputs
3, 5	1Q, 2Q	True flip-flop outputs
7	GND	Ground (0 V)
12, 9	$1\overline{CP}$, $2\overline{CP}$	Clock input (HIGH-to-LOW, edge-triggered)
13, 10	$1\overline{R}$, $2\overline{R}$	Asynchronous reset inputs (active LOW)
14	V_{CC}	Positive supply voltage

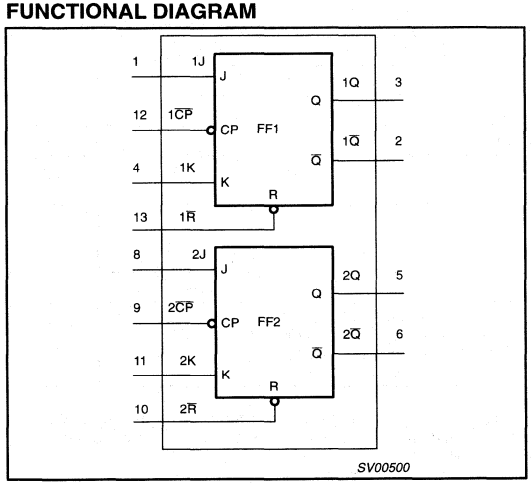
LOGIC SYMBOL



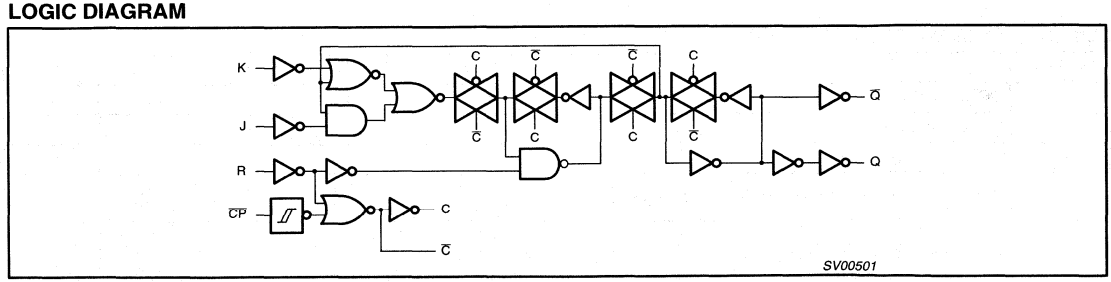
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	$n\overline{R}$	$n\overline{CP}$	nJ	nK	nQ	$n\overline{Q}$
Asynchronous reset	L	X	X	X	L	H
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (reset)	H	↓	l	h	L	H
Load "1" (set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

NOTES:
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition.
X = don't care
↓ = HIGH-to-LOW CP transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 to 5.5 V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; flip-flops	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		80	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} − 0.6 V			500		850	μA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $n\overline{CP}$ to nQ, $n\overline{Q}$	Figures 1, 2	1.2		95				ns
			2.0		32	44		56	
			2.7		24	33		41	
			3.0 to 3.6		18[2]	26		33	
			4.5 to 5.5			22		28	

AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	–40 to +85 °C			–40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $n\overline{R}$ to nQ, $n\overline{Q}$	Figures 1, 2	1.2		95				ns
			2.0		32	44		56	
			2.7		24	33		41	
			3.0 to 3.6		18[2]	26		33	
			4.5 to 5.5			22		28	
t_W	Clock pulse width HIGH or LOW	Figure 2	2.0	34	14		41		ns
			2.7	25	10		30		
			3.0 to 3.6	20	8[2]		24		
			4.5 to 5.5	15			18		
t_W	Reset pulse width LOW	Figure 2	2.0	34	14		41		ns
			2.7	25	10		30		
			3.0 to 3.6	20	8[2]		24		
			4.5 to 5.5	15					
t_{rem}	Removal time $n\overline{R}$ to $n\overline{CP}$	Figure 2	1.2		35				ns
			2.0	24	12		29		
			2.7	18	9		21		
			3.0 to 3.6	14	7[2]		17		
			4.5 to 5.5	11			14		
t_{su}	Set-up time nJ, nK to $\overline{CP}$	Figure 1	1.2		40				ns
			2.0	26	14		31		
			2.7	19	10		23		
			3.0 to 3.6	15	8[2]		18		
			4.5 to 5.5	12			15		
t_h	Hold time nJ, nK to $\overline{CP}$	Figure 1	1.2		-10				ns
			2.0	5	–3		5		
			2.7	5	–2		5		
			3.0 to 3.6	5	–2[2]		5		
			4.5 to 5.5	5			5		
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40		12		MHz
			2.7	19	58		16		
			3.0 to 3.6	24	70[2]		20		
			4.5 to 5.5	30			24		

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V and $\geq$ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

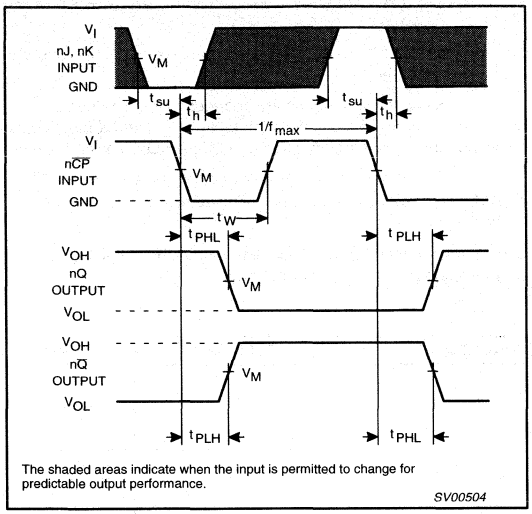


Figure 1. Clock (n$\overline{CP}$) to output (nQ, n$\overline{Q}$) propagation delays, the clock pulse width, the J and K to n$\overline{CP}$ set-up and hold times and the maximum clock pulse frequency.

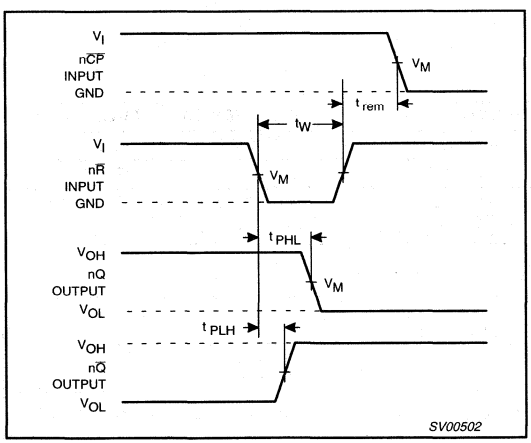


Figure 2. Reset (n$\overline{R}$) input to output (nQ, n$\overline{Q}$) propagation delays, the reset pulse width and the n$\overline{R}$ to n$\overline{CP}$ removal time.

TEST CIRCUIT

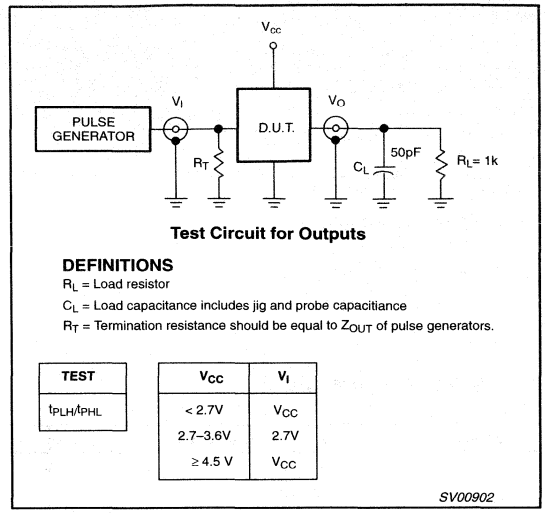


Figure 3. Load circuitry for switching times.

Dual J$\overline{K}$ flip-flop with set and reset; positive-edge trigger 74LV109

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: flip-flops

DESCRIPTION

The 74LV109 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT109.

The 74LV109 is a dual positive-edge triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table. The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The J$\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq$ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF; V_{CC} = 3.3 V	14 12 12	ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_I = GND to V_{CC}[1]	20	pF

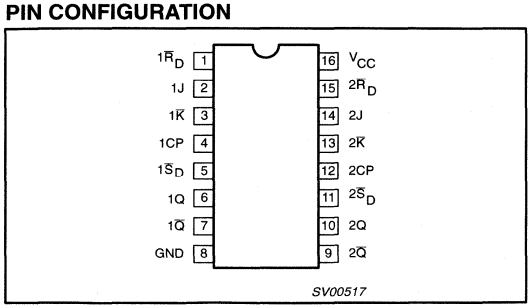
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	−40°C to +125°C	74LV109 N	74LV109 N	SOT38-4
16-Pin Plastic SO	−40°C to +125°C	74LV109 D	74LV109 D	SOT109-1
16-Pin Plastic SSOP Type II	−40°C to +125°C	74LV109 DB	74LV109 DB	SOT338-1
16-Pin Plastic TSSOP Type I	−40°C to +125°C	74LV109 PW	74LV109PW DH	SOT403-1

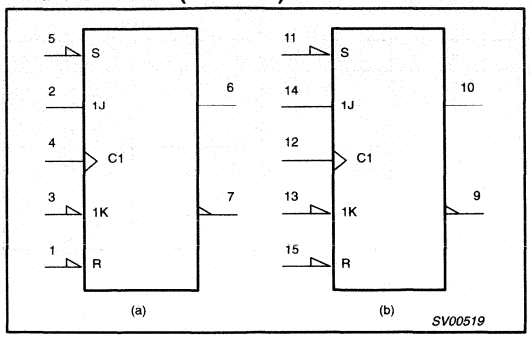
PIN CONFIGURATION



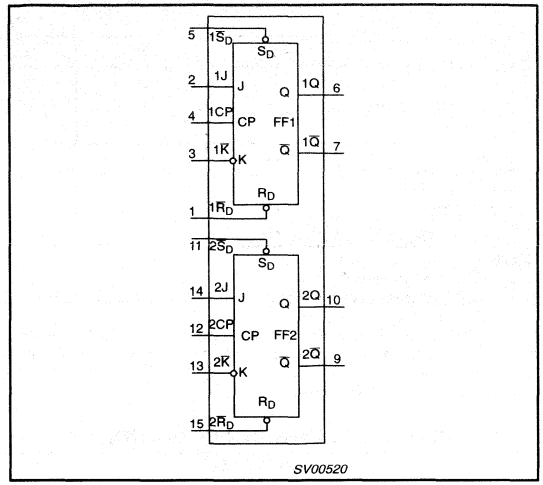
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	1$\overline{R}_D$, 2$\overline{R}_D$	Asynchronous reset input (active LOW)
2, 14, 3, 13	1J, 2J, 1$\overline{K}$, 2$\overline{K}$	Synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	Clock input (LOW-to-HIGH, edge-triggered)
5, 11	1$\overline{S}_D$, 2$\overline{S}_D$	Asynchronous set inputs (active LOW)
6, 10	1Q, 2Q	True flip-flop outputs
7, 9	1$\overline{Q}$, 2$\overline{Q}$	Complement flip-flop outputs
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

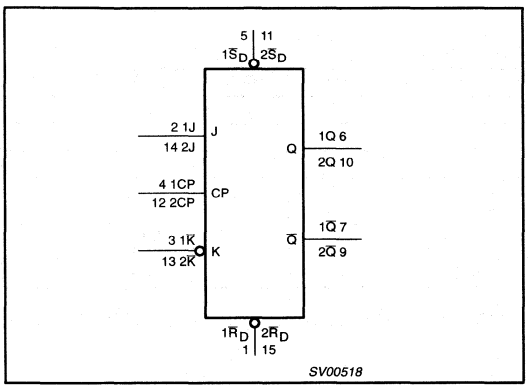
LOGIC SYMBOL (IEEE/IEC)



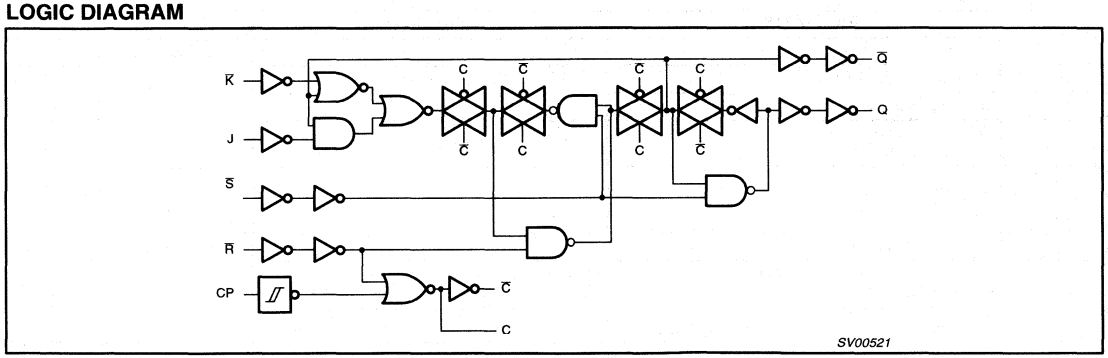
FUNCTIONAL DIAGRAM



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	nCP	nJ	$n\overline{K}$	nQ	$n\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

NOTES:
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.
X = don't care
↑ = LOW-to-HIGH CP transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	-40 -40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTE:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; flip-flops	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		80	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC}$ – 0.6 V			500		850	μA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$	Figure 1	1.2		90				ns
			2.0		31	58		70	
			2.7		23	43		51	
			3.0 to 3.6		18[2]	34		41	
t_{PLH}	Propagation delay n$\overline{S}_D$ to nQ	Figure 2	1.2		55				ns
			2.0		19	36		44	
			2.7		14	26		33	
			3.0 to 3.6		10[2]	21		26	

AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}	Propagation delay $n\overline{S}_D$ to $n\overline{Q}$	Figure 2	1.2		75				ns
			2.0		26	46		60	
			2.7		19	36		44	
			3.0 to 3.6		17[2]	29		35	
t_{PHL}	Propagation delay $n\overline{R}_D$ to nQ	Figure 2	1.2		75				ns
			2.0		26	46		60	
			2.7		19	36		44	
			3.0 to 3.6		15[2]	29		35	
t_{PLH}	Propagation delay $n\overline{R}_D$ to $n\overline{Q}$	Figure 2	1.2		70				ns
			2.0		24	44		54	
			2.7		18	33		40	
			3.0 to 3.6		13[2]	26		32	
t_W	Clock pulse width HIGH or LOW	Figure 1	2.0	34	12		41		ns
			2.7	25	9		30		
			3.0 to 3.6	20	7[2]		24		
t_W	Set or reset pulse width HIGH or LOW	Figure 2	2.0	34	9		41		ns
			2.7	25	6		30		
			3.0 to 3.6	20	5[2]		24		
t_{rem}	Removal time $n\overline{S}_D$, $n\overline{R}_D$ to nCP	Figure 2	1.2		35				ns
			2.0	24	12		29		
			2.7	18	9		21		
			3.0 to 3.6	14	7[2]		17		
t_{su}	Set-up time nJ, n$\overline{K}$ to CP	Figure 1	1.2		30				ns
			2.0	22	10		26		
			2.7	16	8		19		
			3.0 to 3.6	13	6[2]		15		
t_h	Hold time nJ, n$\overline{K}$ to nCP	Figure 1	1.2		–5				ns
			2.0	5	–2		5		
			2.7	5	–1		5		
			3.0 to 3.6	5	0[2]		5		
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40		12		MHz
			2.7	19	58		16		
			3.0 to 3.6	24	70[2]		20		

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

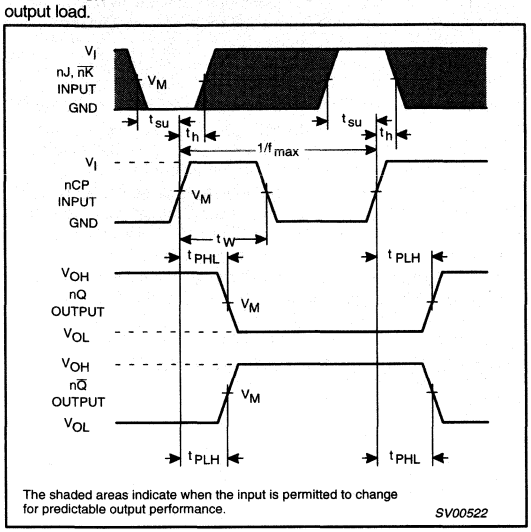


Figure 1. Clock (nCP) to output (nQ, n$\overline{Q}$) propagation delays, the clock pulse width, the nJ and n$\overline{K}$ to nCP set-up, the nCP to nJ, n$\overline{K}$ hold times and the maximum clock pulse frequency.

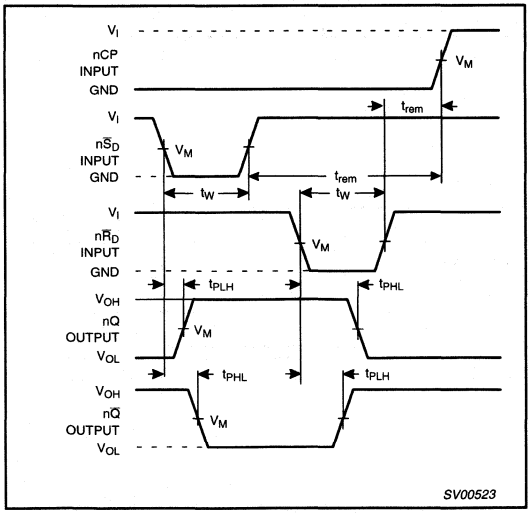
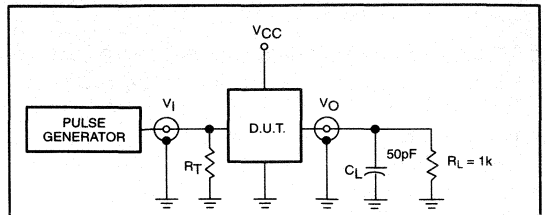


Figure 2. Set (n$\overline{S}_D$) and reset (n$\overline{R}_D$) input to output (nQ, n$\overline{Q}$) propagation delays, the set and reset pulse widths and the n$\overline{R}_D$, n$\overline{S}_D$ to nCP removal time.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00901

Figure 3. Load circuitry for switching times.

Dual retriggerable monostable multivibrator with reset

74LV123

FEATURES

- Optimized for Low Voltage applications: 1.0 to 5.5V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulses
- Schmitt-trigger action on all inputs except for the reset input
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- I_{CC} category: MSI

DESCRIPTION

The 74LV123 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT123.

The 74LV123 is a dual retriggerable monostable multivibrator with output pulse width control by three methods. The basic pulse time is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}). They are normally connected as shown in Figure 1. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ = HIGH, $n\overline{Q}$ = LOW) can be made as long as desired. Alternatively, an output delay can be terminated at any time by a LOW-going edge on input $n\overline{R}_D$, which also inhibits the triggering. Figures 1 and 2 illustrate pulse control by retriggering and early reset. The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}. For pulse width when C_{EXT} <10000pF, see Figure 5. When C_{EXT} > 10,000pF, the typical output pulse width is defined as: $t_W = 0.45 \times R_{EXT} \times C_{EXT}$ (typ.), where t_W = pulse width in ns; R_{EXT} = external resistor in KΩ; and C_{EXT} = external capacitor in pF. Schmitt-trigger action in the $n\overline{A}$ and nB inputs makes the circuit highly tolerant of slower input rise and fall times.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $n\overline{A}$, nB to nQ, $n\overline{Q}$ $n\overline{R}_D$ to nQ, $n\overline{Q}$	C_L = 15pF V_{CC} = 3.3V R_{EXT} = 5KΩ C_{EXT} = 0pF	 25 20	 ns ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per monostable	V_{CC} = 3.3V, V_I = GND to V_{CC}[1]	60	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

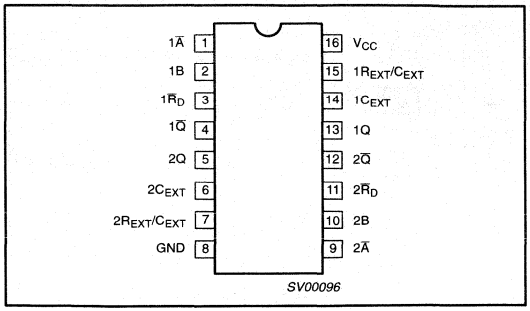
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV123 N	74LV123 N	SOT38-1
16-Pin Plastic SO	–40°C to +125°C	74LV123 D	74LV123 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV123 DB	74LV123 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV123 PW	74LV123PW DH	SOT403-1

Dual retriggerable monostable multivibrator with reset

74LV123

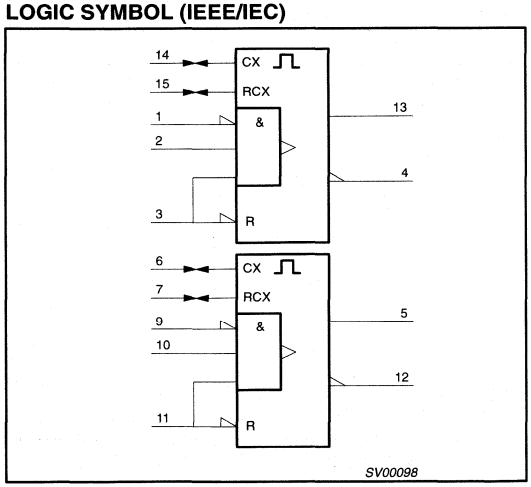
PIN CONFIGURATION



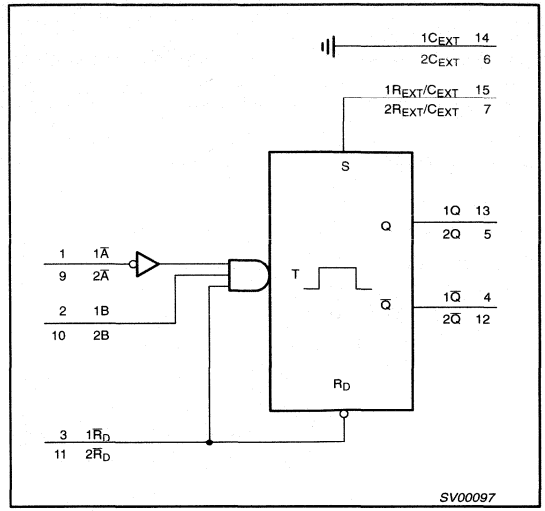
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1,9	1$\overline{A}$, 2$\overline{A}$	Trigger inputs (negative-edge triggered)
2,10	1B, 2B	Trigger inputs (positive-edge triggered)
3,11	1$\overline{R}_D$, 2$\overline{R}_D$	Direct reset LOW and trigger action at positive edge
4, 12	1$\overline{Q}$, 2$\overline{Q}$	Outputs (active LOW)
7	2R_{EXT}/C_{EXT}	External resistor/capacitor connection
8	GND	Ground (0V)
13, 5	1Q, 2Q	Outputs (active HIGH)
14, 6	1C_{EXT}, 2C_{EXT}	External capacitor connection
15	1R_{EXT}/C_{EXT}	External resistor/capacitor connection
16	V_{CC}	Positive supply voltage

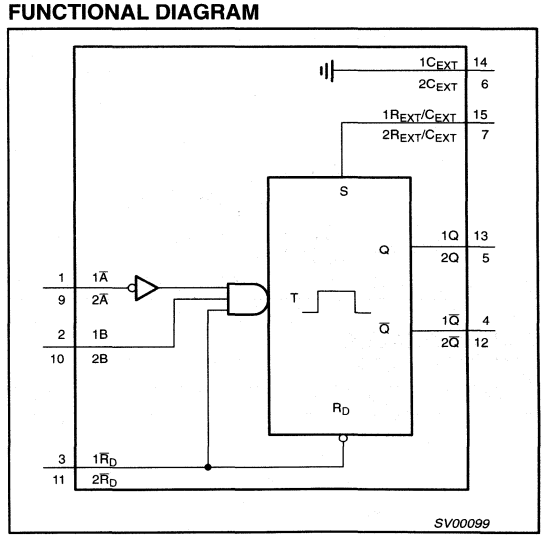
LOGIC SYMBOL (IEEE/IEC)



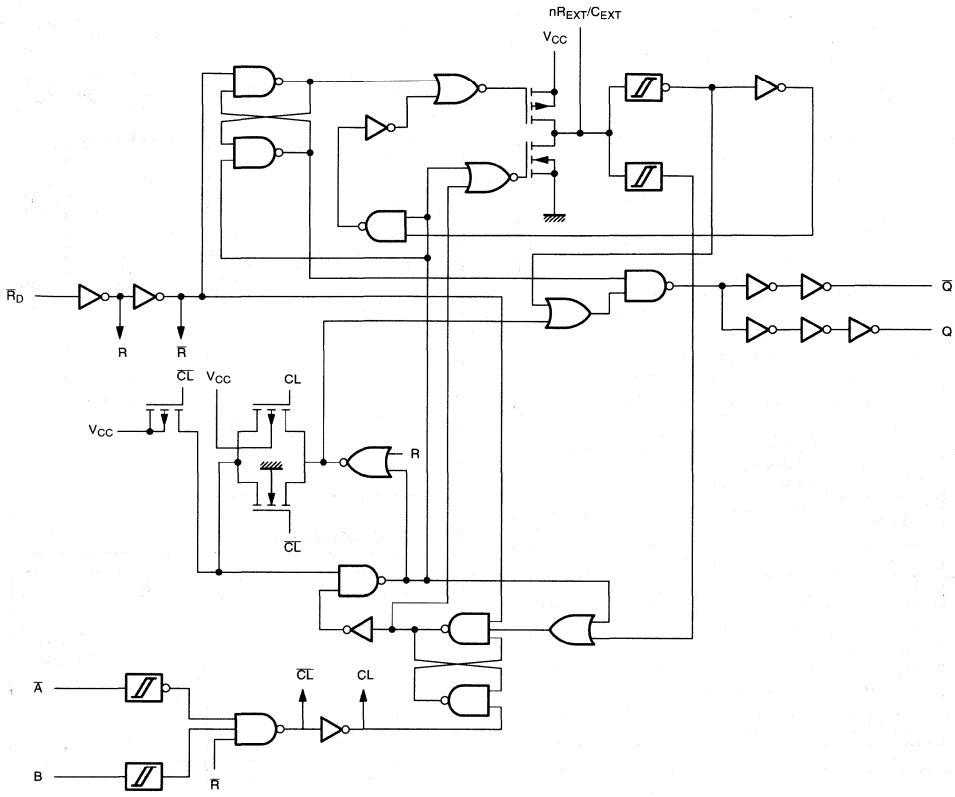
LOGIC SYMBOL



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



It is recommended that Pin 6 ($2C_{EXT}$) and Pin 14 ($1C_{EXT}$) by externally grounded to Pin 8 (GND)

FUNCTION TABLE

INPUTS			OUTPUTS	
$n\overline{R}_D$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L *	H *
X	X	L	L *	H *
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

NOTES:

* If the monostable was triggered before this condition was established, the pulse will continue as programmed.

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH level output pulse
⎍ = one LOW level output pulse

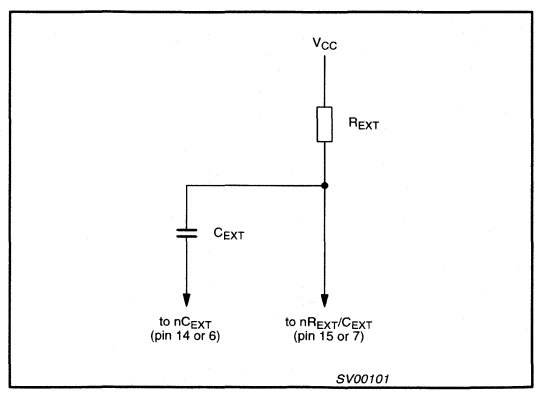


Figure 1.Timing component connection

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTES:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$ KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85°C			–40 to +125°C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}	Propagation delay $n\overline{R}_D$, $n\overline{A}$, nB, to $n\overline{Q}$	Figure 3 C_{EXT} = 0pF R_{EXT} = 5KΩ	1.2		120				ns
			2.0		40	76		92	
			2.7		30	56		68	
			3.0 to 3.6		25[2]	48		57	
			4.5 to 5.5		18[2]	40		46	
t_{PLH}	Propagation delay $n\overline{R}_D$, $n\overline{A}$, nB, to nQ	Figure 3 C_{EXT} = 0pF R_{EXT} = 5KΩ	1.2		120				ns
			2.0		40	76		92	
			2.7		30	56		68	
			3.0 to 3.6		25[2]	48		57	
			4.5 to 5.5		182	40		46	
t_{PHL}	Propagation delay nR_D to nQ (reset)	Figure 3 C_{EXT} = 0pF R_{EXT} = 5KΩ	1.2		100				ns
			2.0		30	57		68	
			2.7		23	43		51	
			3.0 to 3.6		20[2]	38		45	
			4.5 to 5.5		14[2]	31		36	
t_{PLH}	Propagation delay nR_D to nQ (reset)	Figure 3 C_{EXT} = 0pF R_{EXT} = 5KΩ	1.2		100				ns
			2.0		30	57		68	
			2.7		23	43		51	
			3.0 to 3.6		20[2]	38		45	
			4.5 to 5.5		14[2]	31		36	
t_W	Trigger pulse width nA = LOW	Figure 3	2.0	30	5		40		ns
			2.7	25	3.5		30		
			3.0 to 3.6	20	3.0[2]		25		
			4.5 to 5.5	15	2.5[2]		20		
t_W	Trigger pulse width nB = HIGH	Figure 3	2.0	30	13		40		ns
			2.7	25	8		30		
			3.0 to 3.6	20	7[2]		25		
			4.5 to 5.5	15	5[2]		20		
t_W	Reset pulse width nR_D = LOW	Figure 2	2.0	35	6		45		ns
			2.7	30	5		40		
			3.0 to 3.6	25	4[2]		30		
			4.5 to 5.5	20	3[2]		25		
t_W	Output pulse width $n\overline{Q}$ = HIGH nQ = LOW	Figures 1, 2 C_{EXT} = 100nF R_{EXT} = 10KΩ	2.0		470				µs
			2.7		460				
			3.0 to 3.6		450[2]				
			4.5 to 5.5		430[2]				
t_W	Output pulse width $n\overline{Q}$ = HIGH nQ = LOW	Figures 1, 2 C_{EXT} = 0pF R_{EXT} = 5KΩ	2.0		100				ns
			2.7		90				
			3.0 to 3.6		80[2]				
			4.5 to 5.5		70[2]				
t_{rt}	Retrigger time nA, nB	Figure 1 C_{EXT} = 0pF R_{EXT} = 5KΩ	2.0		70				ns
			2.7		55				
			3.0 to 3.6		45[2]				
			4.5 to 5.5		40[2]				

AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$ KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85°C			−40 to +125°C		
			V_{CC}(V)	MIN	TYP	MAX	MIN	MAX	
R_{EXT}	External timing resistor	Figure 5	1.2	10		1000			KΩ
			2.0	5		1000			
			2.7	3		1000			
			3.0 to 3.6	2		1000			
			4.5 to 5.5	2		1000			
C_{EXT}	External timing capacitor	Figure 5[3]	1.2	No limits					pF
			2.0						
			2.7						
			3.0 to 3.6						
			4.5 to 5.5						

NOTES:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25$°C.
2. Typical value measured at $V_{CC} = 3.3$V.
3. Typical value measured at $V_{CC} = 5.0$V.
4. For other R_{EXT} and C_{EXT} combinations see Figure 5.
   if $C_{EXT} > 10$ nF, the next formula is valid:
   $t_W = K \times R_{EXT} \times C_{EXT}$ (typ.)
   where, t_W = output pulse width in ns;
   R_{EXT} = external resistor in KΩ; C_{EXT} = external capacitor in pF;
   K = constant = 0.45 for $V_{CC} = 5.0$V and 0.48 for $V_{CC} = 2.0$V.
   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.
5. The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}.
   The output pulse width will only be extended when the time between the active-going edges of the trigger pulses meets the minimum retrigger time.
   If $C_{EXT} > 10$ pF, the next formula (at $V_{CC} = 5.0$V) for the set-up time of a retrigger pulse is valid:
   $t_{rt} = 30 + 0.19R \times C^{-9} + 13 \times R^{1.05}$ (typ.)
   where, t_{rt} = retrigger time in ns;
   C_{EXT} = external capacitor in pF;
   R_{EXT} = external resistor in KΩ.
   The inherent test jig and pin capacitance at pins 15 and 7 (nR_{EXT}/C_{EXT}) is approximately 7 pF.
6. When the device is powered up, initiate the device via a reset pulse, when $C_{EXT} < 50$pF.

AC WAVEFORMS

$V_M = 1.5$V at $V_{CC} \geq 2.7$V; $V_M = 0.5\ V_{CC}$ at $V_{CC} < 2.7$V; V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

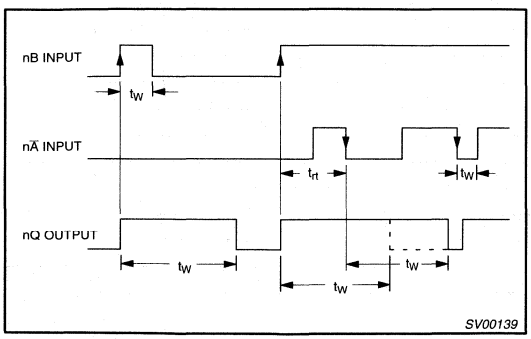


Figure 1.Output pulse control using retrigger pulse; $n\overline{R}_D$ = HIGH.

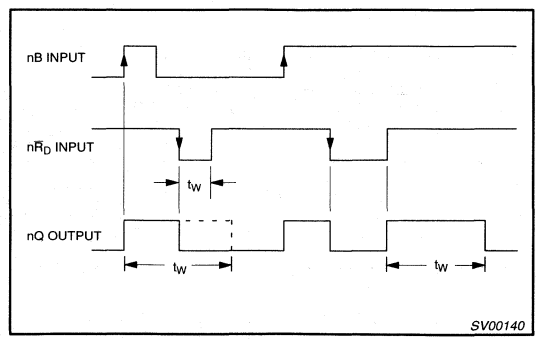


Figure 2.Output pulse control using reset input $n\overline{R}_D$; nĀ = LOW.

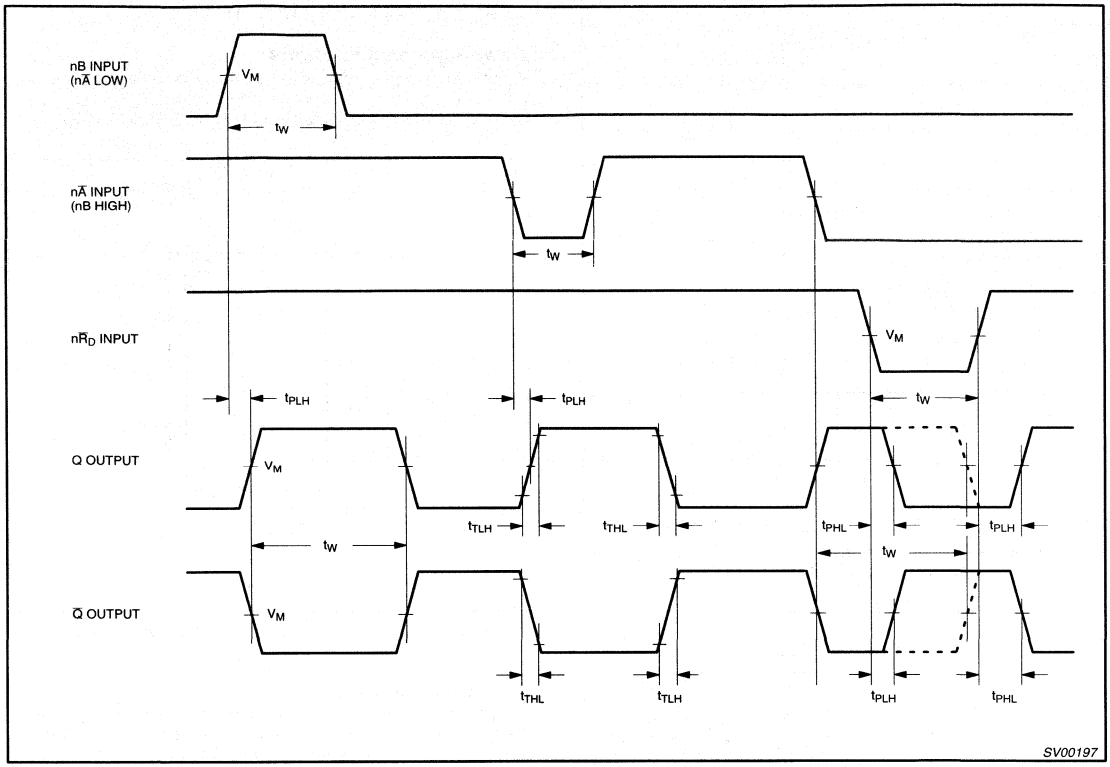


Figure 3. Input ($n\overline{A}$, nB, $n\overline{R}_D$) to output (nQ, $n\overline{Q}$) propagation delays, the output transition times, and the input and output pulse widths.

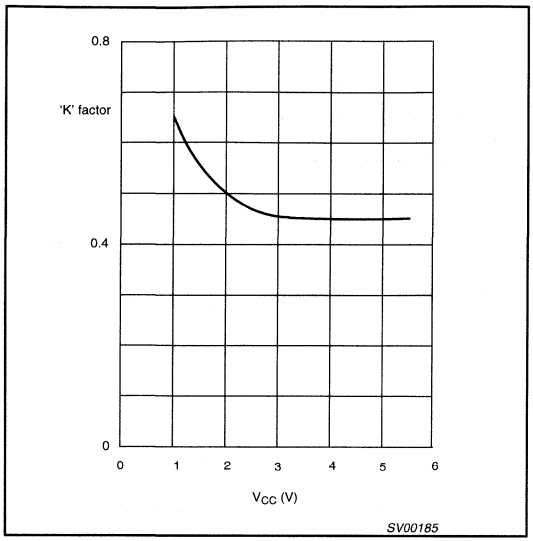


Figure 4. HCT typical "k" factor as a function of V_{CC}; C_X = 10 nF; R_X = 10 KΩ to 100 KΩ.

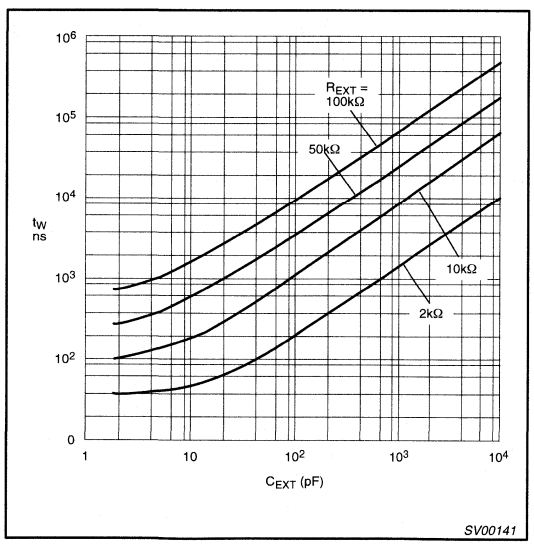


Figure 5.Typical output pulse width as a function of the external capacitor values at V_{CC} = 3.3V and T_{amb} = 25°C.

APPLICATION INFORMATION

Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_X and C_X. This output pulse can be eliminated using the circuit shown in Figure 6.

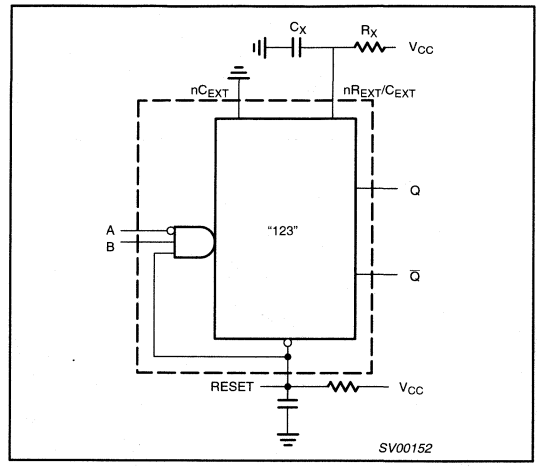


Figure 6. Power-up output pulse elimination circuit

Power-down considerations

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, connect a damping diode (D_X) preferably a germanium or Schottky type diode able to withstand large current surges as shown in Figure 7.

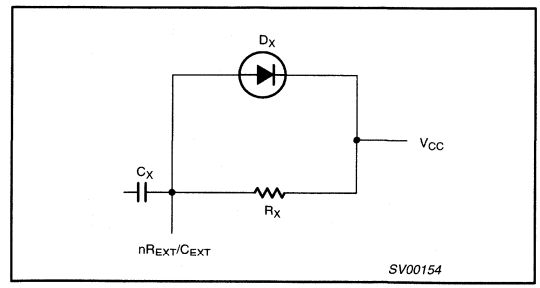
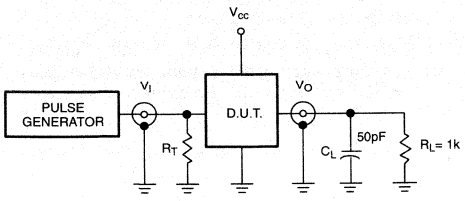


Figure 7. Power-down protection circuit

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitiance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5 V	V_{CC}

SV00902

Figure 8. Load circuitry for switching times

Quad buffer/line driver (3-State) 74LV125

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV125 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT125.

The 74LV125 consists of four non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 15 pF; V_{CC} = 3.3 V	9	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3 V; V_I = GND to V_{CC}[1]	22	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV125 N	74LV125 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV125 D	74LV125 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV125 DB	74LV125 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV125 PW	74LV125PW DH	SOT402-1

PIN DESCRIPTION

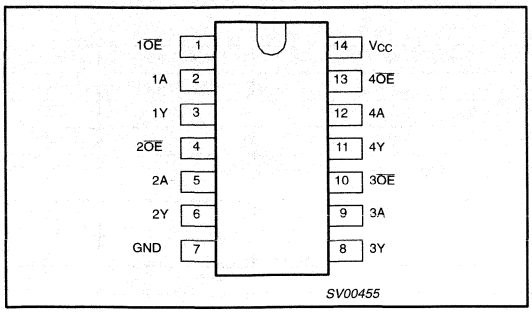
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$1\overline{OE} - 4\overline{OE}$	Data enable inputs (active LOW)
2, 5, 9, 12	1A – 4A	Data inputs
3, 6, 8, 11	1Y – 4Y	Data Outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

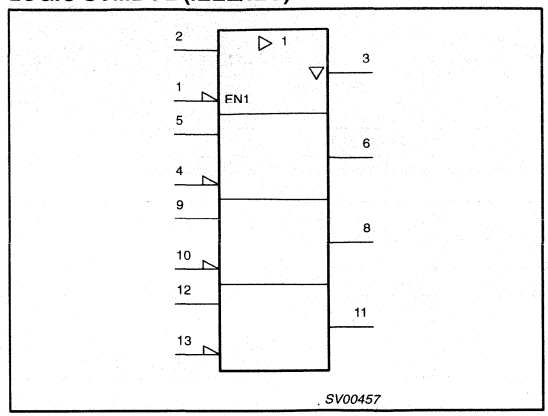
INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

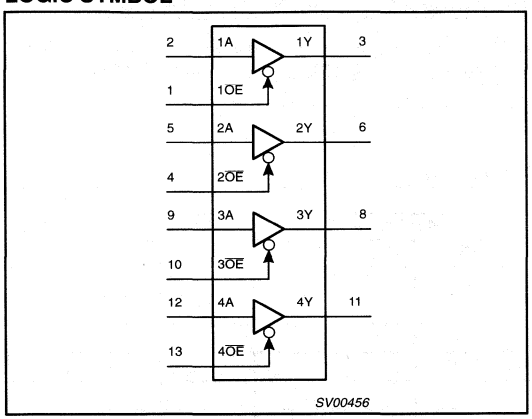
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – bus driver outputs		70	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 to 5.5 V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; I_O = 16mA		0.35	0.55		0.65	

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA to nY	Figures 1, 2	1.2		55				ns
			2.0		19	24		31	
			2.7		14	18		23	
			3.0 to 3.6		10[2]	14		18	
			4.5 to 5.5			12		15	
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nY	Figures 2, 3	1.2		75				ns
			2.0		26	31		39	
			2.7		19	23		29	
			3.0 to 3.6		14[2]	18		23	
			4.5 to 5.5			15		19	
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nY	Figures 2, 3	1.2		65				ns
			2.0		24	32		39	
			2.7		18	24		29	
			3.0 to 3.6		14[2]	20		24	
			4.5 to 5.5			17		21	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V and $\geq$ 4.5 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_X = V_{OL} + 0.1 \times V_{CC}$ at V_{CC} < 2.7 V and $\geq$ 4.5 V.
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V and $\geq$ 4.5 V.

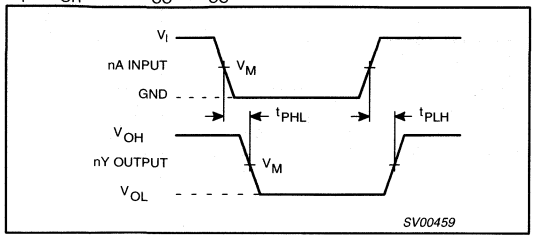


Figure 1. Input (nA) to output (nY) propagation delays and output transition times.

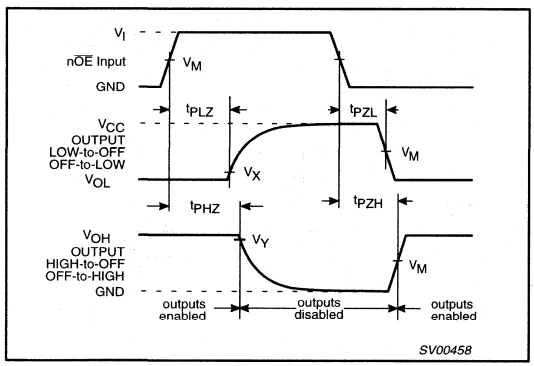
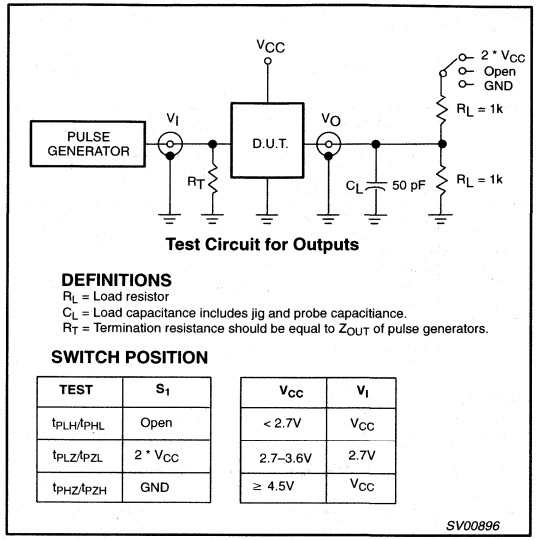


Figure 2. 3-state enable and disable times.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitiance.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
$\geq$ 4.5V	V_{CC}

Figure 3. Load circuitry for switching times.

Quad buffer/line driver (3-State) 74LV126

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV126 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT126.

The 74LV126 consists of four non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 15 pF; V_{CC} = 3.3 V	9	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3 V; V_I = GND to V_{CC}[1]	23	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV126 N	74LV126 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV126 D	74LV126 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV126 DB	74LV126 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV126 PW	74LV126PW DH	SOT402-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 10, 13	1OE – 4OE	Output enable inputs (active HIGH)
2, 5, 9, 12	1A – 4A	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

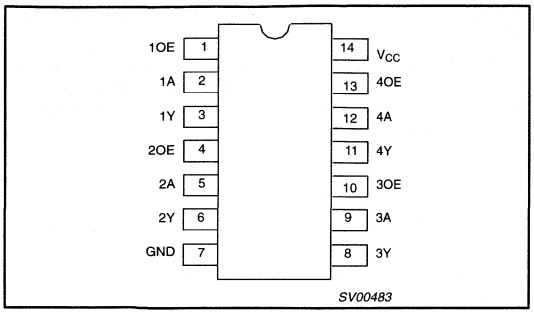
FUNCTION TABLE

INPUTS		OUTPUTS
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

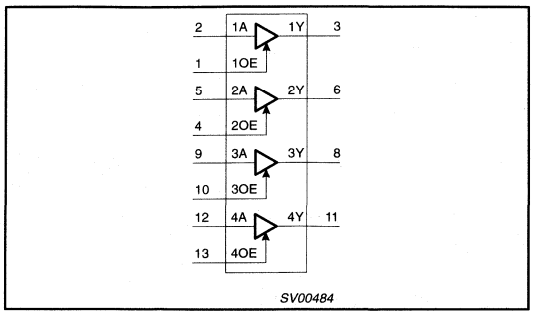
NOTES:

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

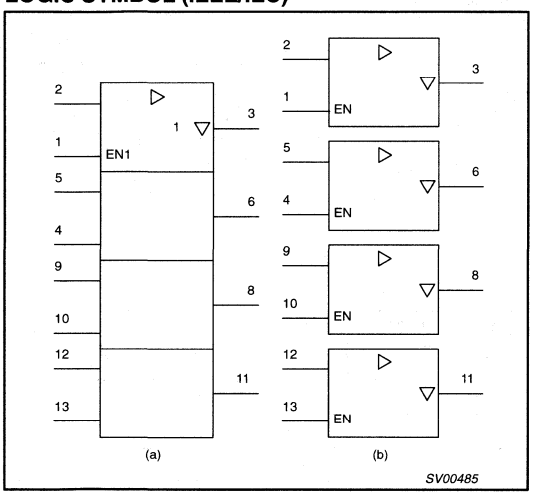
PIN CONFIGURATION



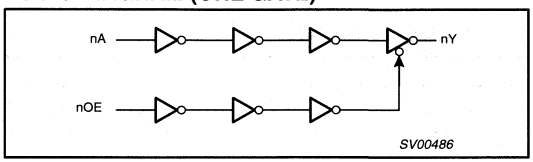
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 to 5.5 V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5 V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5 V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5 V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA to nY	Figures 1, 2	1.2		55				ns
			2.0		19	24		31	
			2.7		14	18		23	
			3.0 to 3.6		10[2]	14		18	
			4.5 to 5.5			12		15	
t_{PZH}/t_{PZL}	3-state output enable time nOE to nY	Figures 1, 2	1.2		75				ns
			2.0		26	31		39	
			2.7		19	23		29	
			3.0 to 3.6		14[2]	18		23	
			4.5 to 5.5			15		19	
t_{PHZ}/t_{PLZ}	3-state output disable time nOE to nY	Figures 1, 2	1.2		65				ns
			2.0		24	32		39	
			2.7		28	24		29	
			3.0 to 3.6		14[2]	20		24	
			4.5 to 5.5			17		21	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V and $\geq$ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_X = V_{OL} + 0.1 \times V_{CC}$ at V_{CC} < 2.7 V and $\geq$ 4.5 V.
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
$V_Y = V_{OH} - 0.1 \times V_{CC}$ at V_{CC} < 2.7 V and $\geq$ 4.5 V.

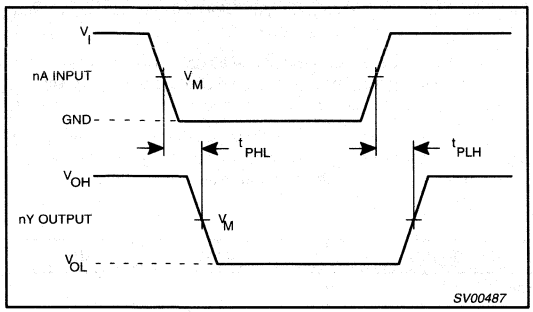


Figure 1. Input (nA, nB) to output (nY) propagation delays

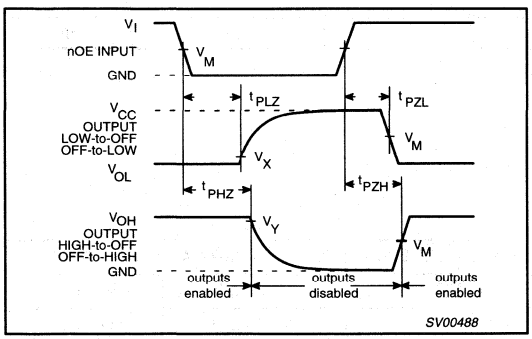


Figure 2. 3-state enable and disable times.

TEST CIRCUIT

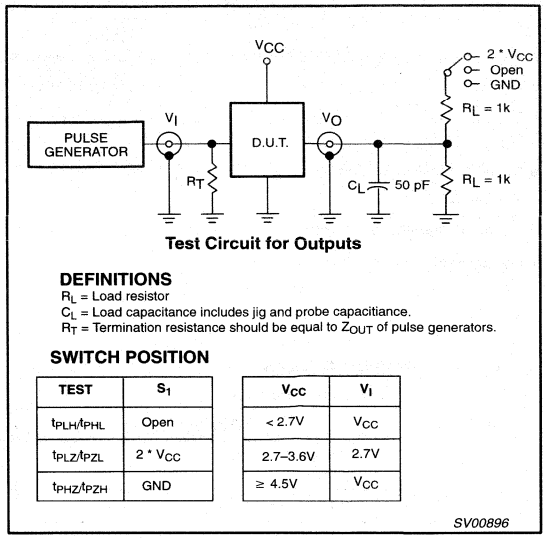


Figure 3. Load circuitry for switching times.

Quad 2-input NAND Schmitt-trigger | 74LV132

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: SSI

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

DESCRIPTION

The 74LV132 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT132.

The 74LV132 contains four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 15pF V_{CC} = 3.3V	10	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	24	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV132 N	74LV132 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV132 D	74LV132 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV132 DB	74LV132 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV132 PW	74LV132PW DH	SOT402-1

PIN DESCRIPTION

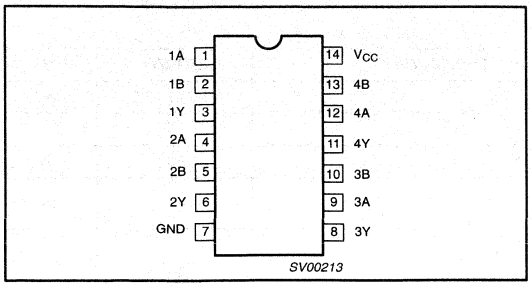
PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

FUNCTION TABLE

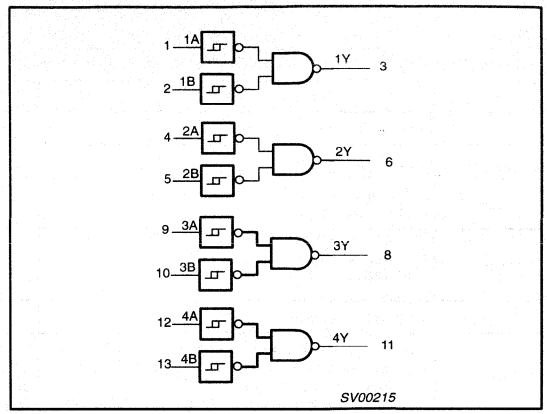
INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level

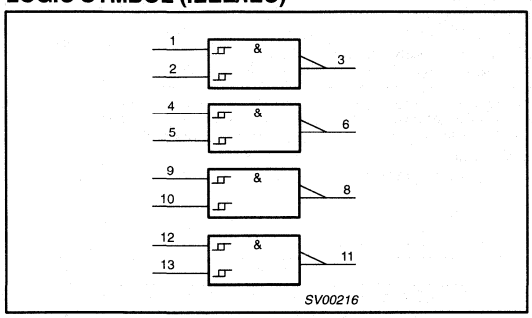
PIN CONFIGURATION



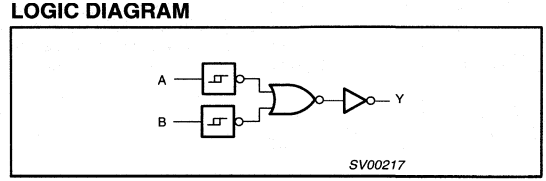
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	

DC CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		40	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ – 0.6V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

TRANSFER CHARACTERISTICS

Voltages are referenced to GND = 0V.

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85°C			–40 to +125°C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
V_{T+}	Positive going threshold	Figures 1 and 2	1.2	–	0.70	–	–		V
			2.0	0.8	1.10	1.4	0.8	1.4	
			2.7	1.0	1.45	2.0	1.0	2.0	
			3.0	1.2	1.60	2.2	1.2	2.2	
			3.6	1.5	1.95	2.4	1.5	2.4	
			4.5	1.7	2.50	3.2	1.7	3.2	
			5.5	2.1	3.00	3.9	2.1	3.9	
V_{T-}	Negative going threshold	Figures 1 and 2	1.2	–	0.34	–	–	–	V
			2.0	0.3	0.65	0.9	0.3	0.9	
			2.7	0.4	0.90	1.4	0.4	1.4	
			3.0	0.6	1.05	1.5	0.6	1.5	
			3.6	0.8	1.30	1.8	0.8	1.8	
			4.5	0.9	1.60	2.0	0.9	2.0	
			5.5	1.2	2.00	2.6	1.2	2.6	
V_H	Hysteresis ($V_{T+} - V_{T-}$)	Figures 1 and 2	1.2	–	0.30	–	–	–	V
			2.0	0.2	0.55	0.8	0.2	0.8	
			2.7	0.3	0.60	1.1	0.3	1.1	
			3.0	0.4	0.65	1.2	0.4	1.2	
			3.6	0.4	0.70	1.2	0.4	1.2	
			4.5	0.4	0.80	1.4	0.4	1.4	
			5.5	0.6	1.00	1.5	0.6	1.5	

NOTE:
1. Unless otherwise stated, all typical values are at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85°C			−40 to +125°C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA, nB, to nY	Figure 6	1.2	–	65	–	–	–	ns
			2.0	–	18	34	–	43	
			2.7	–	15	24	–	30	
			3.0 to 3.6	–	12[2]	20	–	25	
			4.5 to 5.5	–	9.0[2]	14	–	17	

NOTES:
1. Unless otherwise stated, all typical values are at T_{amb} = 25°C.
2. Typical value measured at V_{CC} = 3.3V.
3. Typical value measured at V_{CC} = 5.0V.

TRANSFER CHARACTERISTIC WAVEFORMS

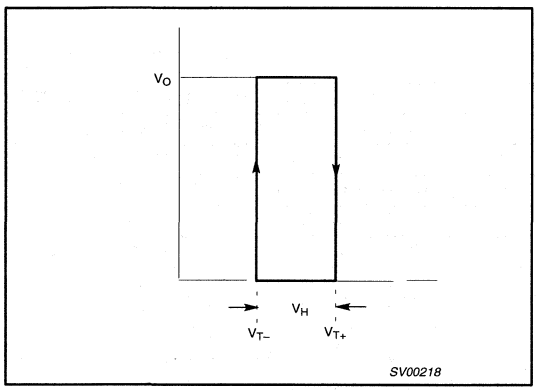


Figure 1. Transfer characteristic.

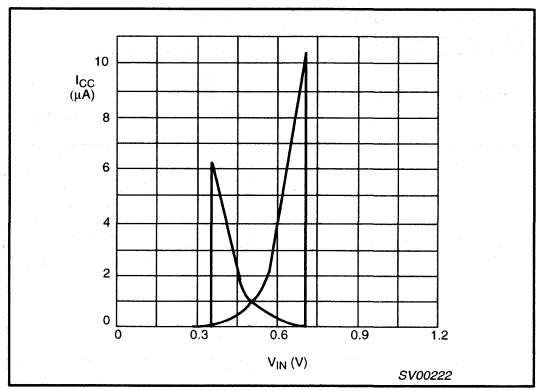


Figure 3. Typical LV132 transfer characteristics; V_{CC} = 1.2V.

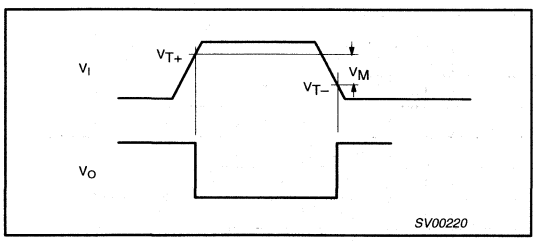


Figure 2. Definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%.

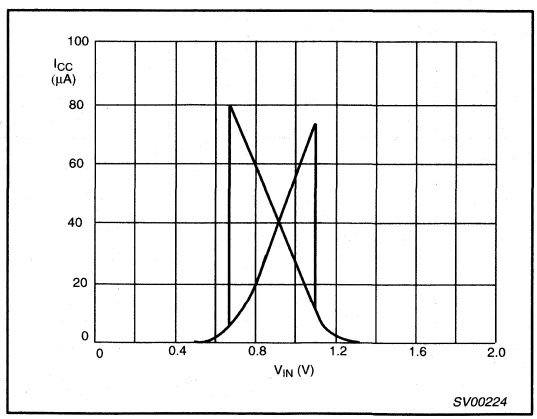


Figure 4. Typical LV132 transfer characteristics; V_{CC} = 2.0V.

TRANSFER CHARACTERISTIC WAVEFORMS (Continued)

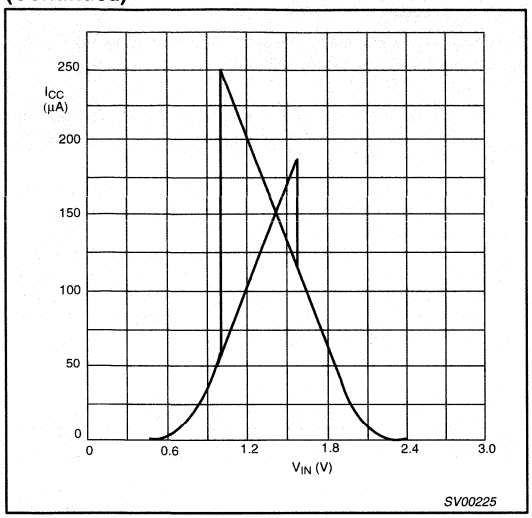


Figure 5. Typical LV132 transfer characteristics; V_{CC} = 3.0V.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V ≤ 3.6V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

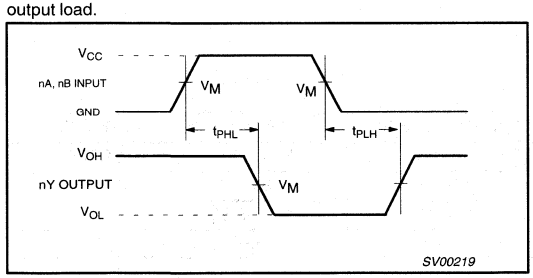


Figure 6. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT

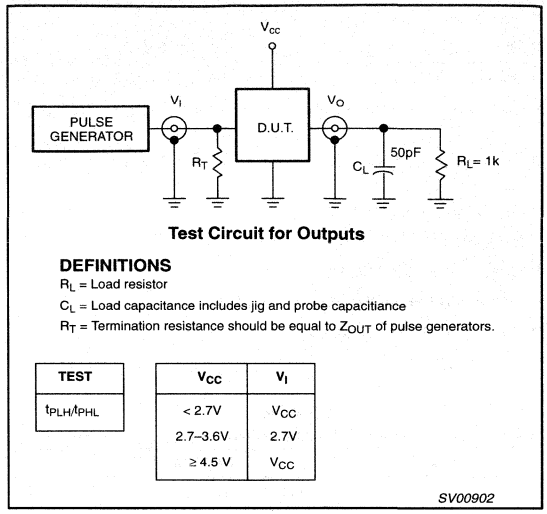


Figure 7.Load circuitry for switching times.

3-to-8 line decoder/demultiplexer; inverting | 74LV138

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV138 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT138.

The 74LV138 accepts three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).

The 74LV138 features three enable inputs: two active LOW ($\overline{E}_1$, and $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74LV138 to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LV138 ICs and one inverter. The 74LV138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state. The 74LV138 is identical to the 74LV238 but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to $\overline{Y}n$, E3 to $\overline{Y}n$, $\overline{E}n$ to $\overline{Y}n$	C_L = 15 pF; V_{CC} = 3.3 V	 12 14	 ns ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per package	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	45	pF

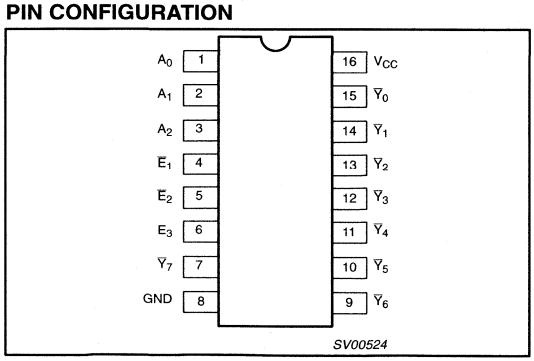
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	−40°C to +125°C	74LV138 N	74LV138 N	SOT38-4
16-Pin Plastic SO	−40°C to +125°C	74LV138 D	74LV138 D	SOT109-1
16-Pin Plastic SSOP Type II	−40°C to +125°C	74LV138 DB	74LV138 DB	SOT338-1
16-Pin Plastic TSSOP Type I	−40°C to +125°C	74LV138 PW	74LV138PW DH	SOT403-1

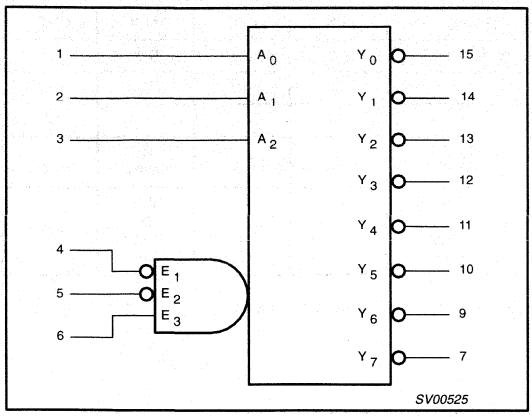
PIN CONFIGURATION



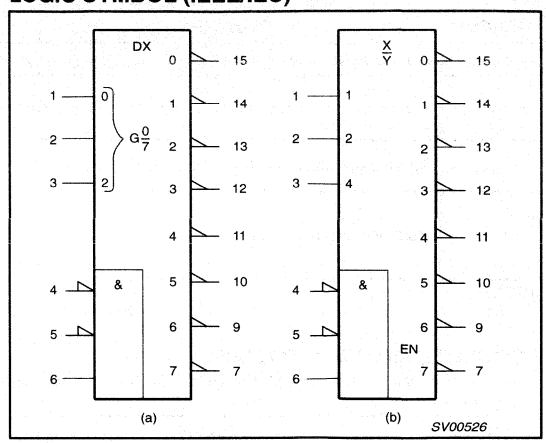
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3	A_0 to A_2	Address inputs
4, 5	$\overline{E}_1$ to $\overline{E}_2$	Enable inputs (active LOW)
6	E_3	Enable inputs (active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	Outputs
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

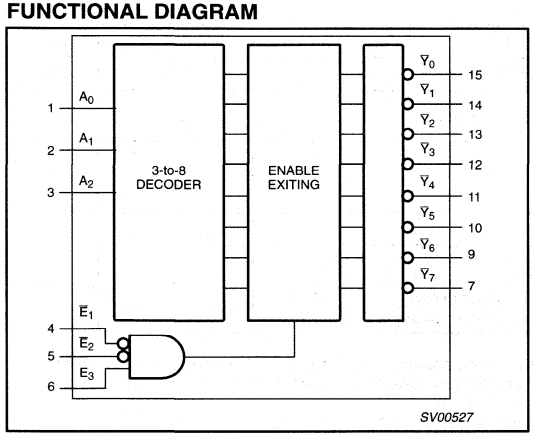
LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 to 5.5 V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay A_n to $\overline{Y}_n$	Figures 1, 3	1.2		75				ns
			2.0		26	44		55	
			2.7		19	31		39	
			3.0 to 3.6		15[2]	26		32	
			4.5 to 5.5		–[3]	17		22	
t_{PHL}/t_{PLH}	Propagation delay E_3 to $\overline{Y}_n$	Figures 1, 3	1.2		75				ns
			2.0		26	43		53	
			2.7		19	30		38	
			3.0 to 3.6		15[2]	25		31	
			4.5 to 5.5			19		24	
t_{PHL}/t_{PLH}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	Figures 2, 3	1.2		75				ns
			2.0		26	43		53	
			2.7		19	30		38	
			3.0 to 3.6		15[2]	25		31	
			4.5 to 5.5			19		24	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.
3. Typical values are measured at V_{CC} = 5.0 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6 V;
V_M = 0.5 V × V_{CC} at V_{CC} < 2.7 V and ≥ 4.5 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

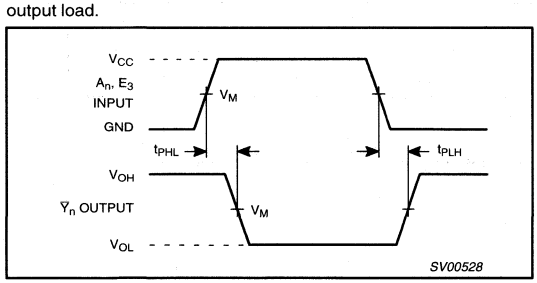


Figure 1. Input (An) and enable input (E_3) to output ($\overline{Y}$n) propagation delays.

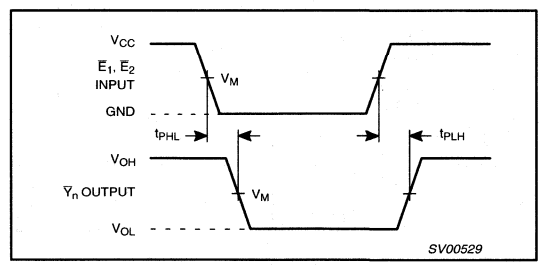
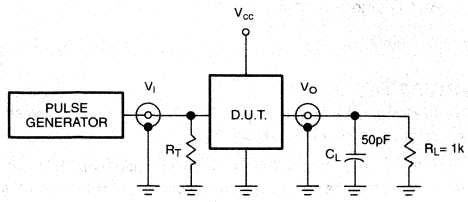


Figure 2. Enable input ($\overline{E}_n$) to output ($\overline{Y}$n) propagation delays.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitiance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5 V	V_{CC}

SV00902

Figure 3. Load circuitry for switching times.

Dual 2-to-4 line decoder/demultiplexer | 74LV139

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

APPLICATIONS

- Memory decoding or data-routing
- Code conversion

DESCRIPTION

The 74LV139 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT139.

The 74LV139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW enable input ($n\overline{E}$).

When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA_n to $n\overline{Y}_n$, $n\overline{E}$ to $n\overline{Y}_n$	C_L = 15 pF; V_{CC} = 3.3 V	11 10	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per multiplexer	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	42	pF

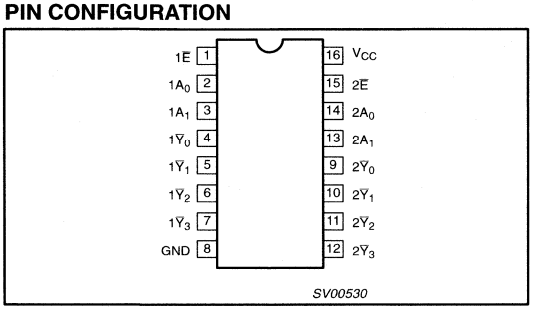
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV139 N	74LV139 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV139 D	74LV139 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV139 DB	74LV139 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV139 PW	74LV139PW DH	SOT403-1

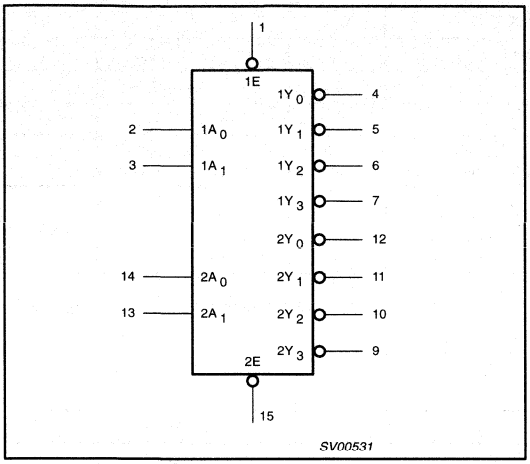
PIN CONFIGURATION



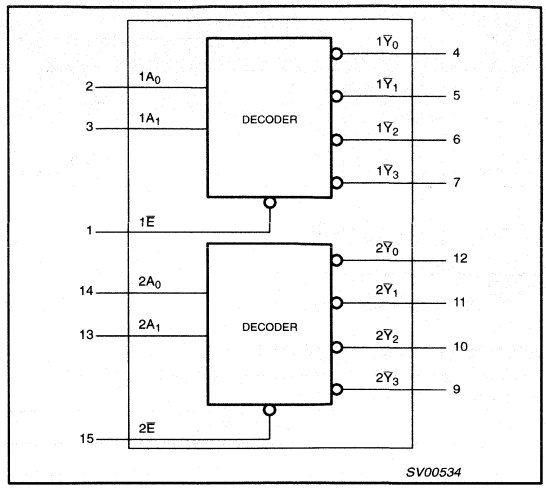
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	Enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	Address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	Outputs (active LOW)
8	GND	Ground (0 V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	Outputs (active LOW)
14, 13	$2A_0$, $2A_1$	Address inputs
16	V_{CC}	Positive supply voltage

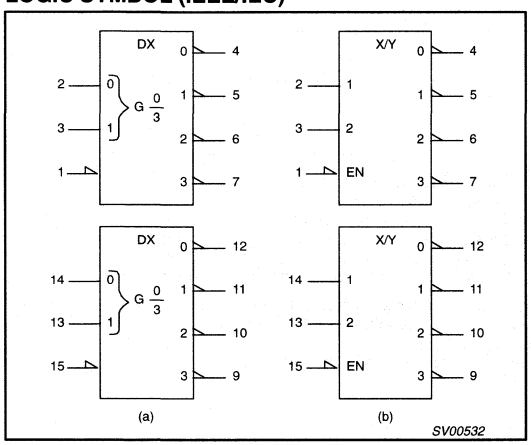
LOGIC DIAGRAM



FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS			OUTPUTS			
$n\bar{E}$	nA_0	nA_1	$n\bar{Y}_0$	$n\bar{Y}_1$	$n\bar{Y}_2$	$n\bar{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 to 5.5 V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA_n to $\overline{Y}_n$	Figures 1, 2	1.2		70				ns
			2.0		24	31		39	
			2.7		18	23		29	
			3.0 to 3.6		13[2]	18		23	
			4.5 to 5.5			15		19	
t_{PHL}/t_{PLH}	Propagation delay $n\overline{E}$ to $\overline{Y}_n$	Figures 1, 2	1.2		60				ns
			2.0		20	27		34	
			2.7		15	20		25	
			3.0 to 3.6		11[2]	16		20	
			4.5 to 5.5			13		16	

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V and ≤ 3.6 V;
$V_M = 0.5$ V $\times V_{CC}$ at $V_{CC} < 2.7$ V and ≥ 4.5 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

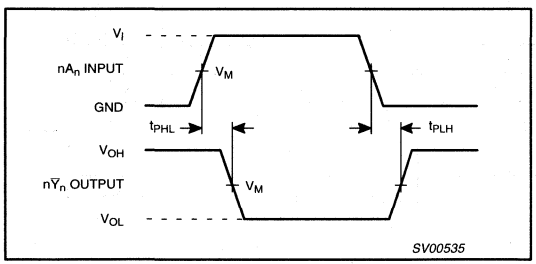


Figure 1. Address input (nA_n) to output ($n\overline{Y}n$) propagation delays.

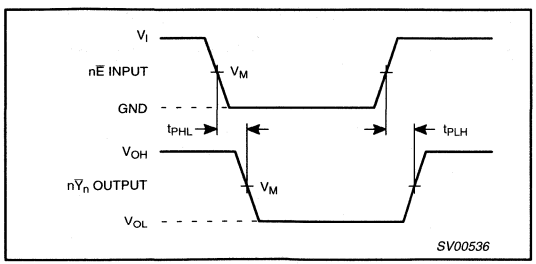
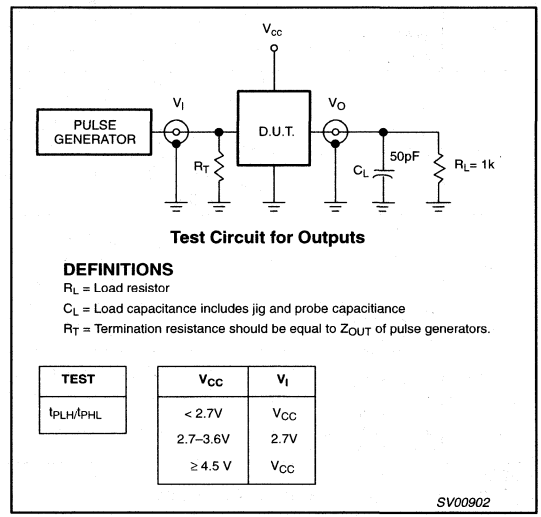


Figure 2. Enable input ($n\overline{E}$) to output ($n\overline{Y}_n$) propagation delays.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5 V	V_{CC}

Figure 3. Load circuitry for switching times.

Dual 4-input multiplexer 74LV153

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Non-inverting outputs
- Separate enable for each output
- Common select inputs
- Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV153 is a low-voltage CMOS device that is pin and function compatible with 74HC/HCT153.

The 74LV153 is a dual 4-input multiplexer which selects 2 bits of data from up to four sources selected by common data select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW output enable inputs ($1\overline{E}$, $2\overline{E}$) which can be used to strobe the outputs independently. The outputs (1Y, 2Y) are forced LOW when the corresponding output enable inputs are HIGH. The 74LV153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch, is determined by the logic levels applied to S_0 and S_1. The logic equations for the outputs are:

$1Y=1\overline{E}.(1I_0.\overline{S}_1.\overline{S}_0+1I_1.\overline{S}_1.S_0+1I_2.S_1.\overline{S}_0+1I_3.S_1.S_0)$

$2Y=2\overline{E}.(2I_0.\overline{S}_1.\overline{S}_0+2I_1.\overline{S}_1.S_0+2I_2.S_1.\overline{S}_0+2I_3.S_1.S_0)$

The 74LV153 can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $1I_n$, $2I_n$ to nY Sn to nY $n\overline{E}$ to nY	C_L = 15 pF; V_{CC} = 3.3 V	 14 14 10	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	30	pF

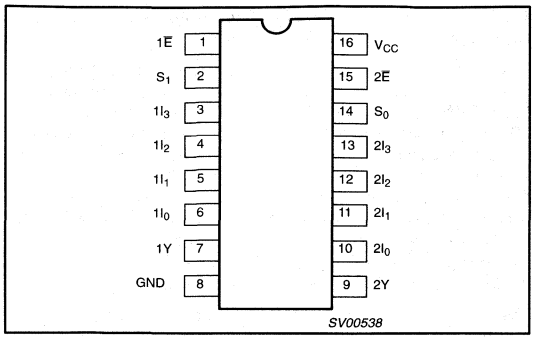
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV153 N	74LV153 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV153 D	74LV153 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV153 DB	74LV153 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV153 PW	74LV153PW DH	SOT403-1

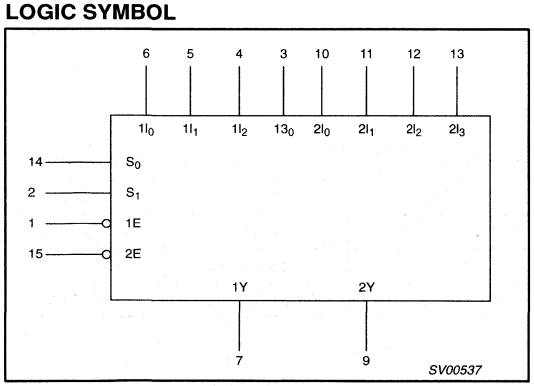
PIN CONFIGURATION



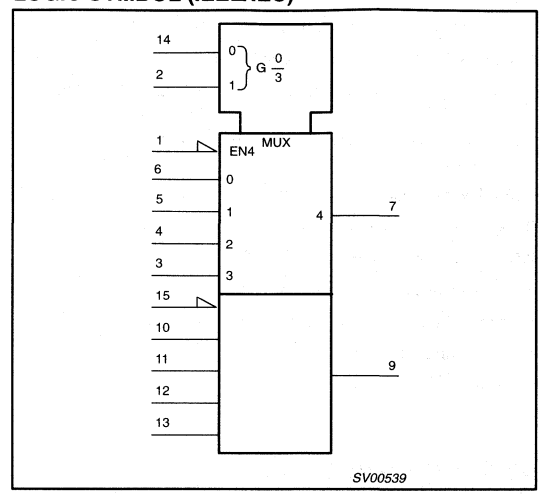
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	1$\overline{E}$, 2$\overline{E}$	Output enable inputs (active LOW)
14, 2	S_0, S_1	Common data select inputs
6, 5, 4, 3	$1I_0$ to $1I_3$	Data inputs from source 1
7	1Y	Multiplexer output from source 1
8	GND	Ground (0 V)
9	2Y	Multiplexer output from source 2
10, 11, 12, 13	$2I_0$ to $2I_3$	Data inputs from source 2
16	V_{CC}	Positive supply voltage

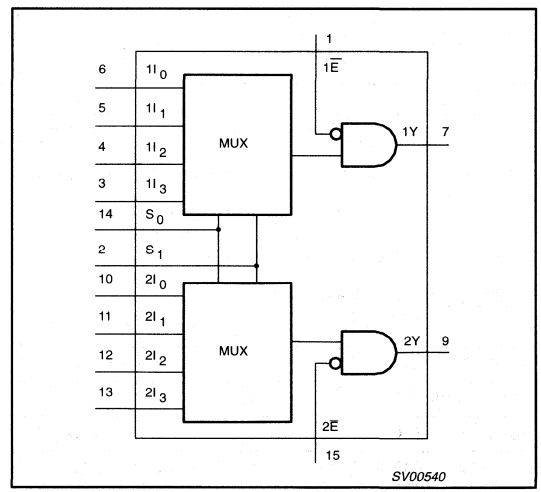
LOGIC SYMBOL



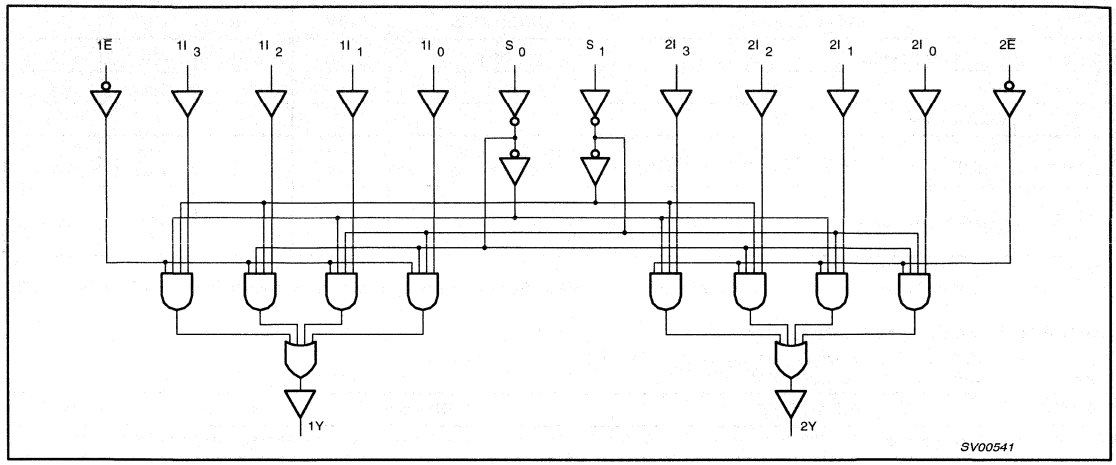
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	nI_0	nI_1	nI_2	nI_3	$n\bar{E}$	nY
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V			500		850	μA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L =KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $1I_n$ to nY; $2I_n$ to nY	Figures 1, 2	1.2		85				ns
			2.0		29	56		66	
			2.7		21	41		49	
			3.0 to 3.6		16[2]	33		39	
t_{PHL}/t_{PLH}	Propagation delay S_n to nY	Figures 1, 2	1.2		90				ns
			2.0		31	58		70	
			2.7		23	43		51	
			3.0 to 3.6		17[2]	34		41	
t_{PHL}/t_{PLH}	Propagation delay $n\overline{E}$ to nY	Figures 1, 2	1.2		60				ns
			2.0		20	39		46	
			2.7		15	29		34	
			3.0 to 3.6		11[2]	23		27	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
V_M = 0.5 V × V_{CC} at V_{CC} < 2.7 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

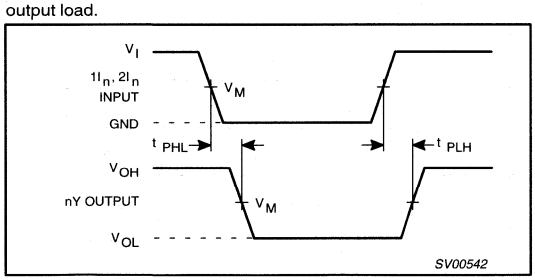


Figure 1. Input ($1I_n$, $2I_n$) to output (1Y, 2Y) propagation delays.

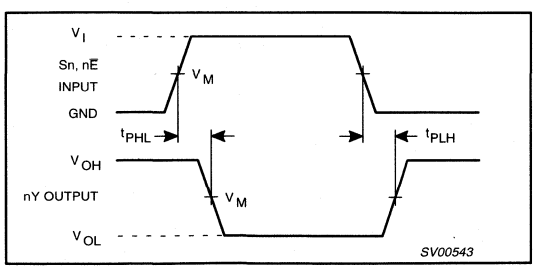
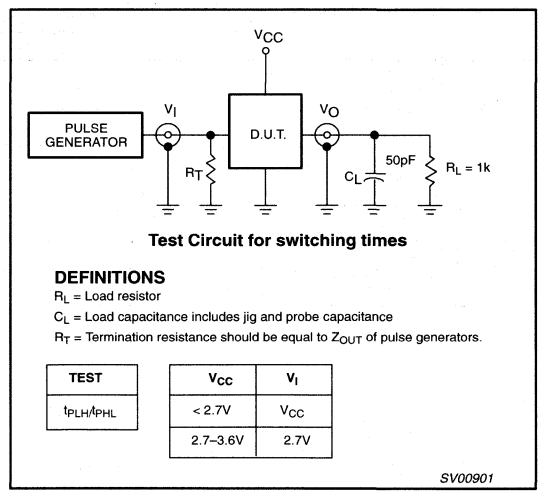


Figure 2. Select input (S_0, S_1) and the output enable input ($\overline{E}$) to output ($n\overline{Y}_n$) propagation delays.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V

Figure 3. Load circuitry for switching times.

4-to-16 line decoder/demultiplexer 74LV154

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- 2-input enable gate for strobing or expansion
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV154 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT154.

The 74LV154 decoders accept four active HIGH binary address inputs (A_0 to A_3) and provide 16 mutually exclusive active LOW outputs($\overline{Y}_0$ to $\overline{Y}_{15}$).

The 2-input enable inputs ($\overline{E}_0$, $\overline{E}_1$) can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder.

The enable input has two AND'ed inputs which must be LOW to enable the outputs.

The 74LV154 can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable is LOW, the addressed output will follow the state of the applied data.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n, $\overline{E}_n$ to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 3.3 V	11	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	60	pF

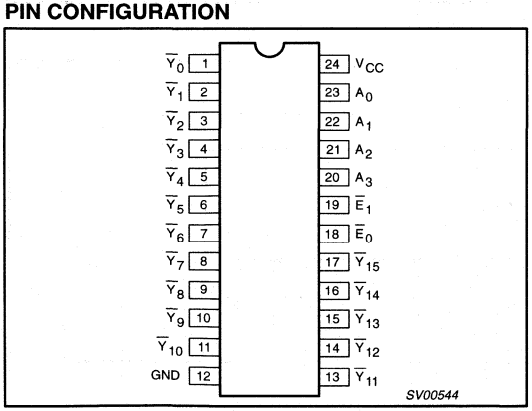
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic DIL	–40°C to +125°C	74LV154 N	74LV154 N	SOT101-1
24-Pin Plastic SO	–40°C to +125°C	74LV154 D	74LV154 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +125°C	74LV154 DB	74LV154 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV154 PW	74LV154PW DH	SOT355-1

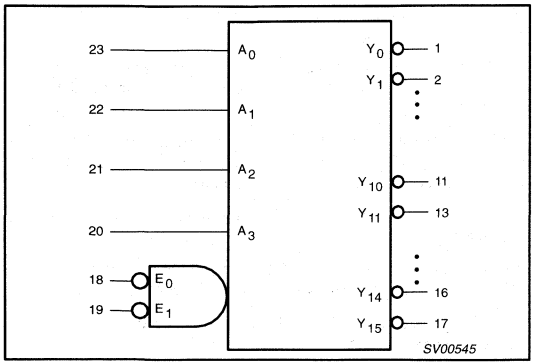
PIN CONFIGURATION



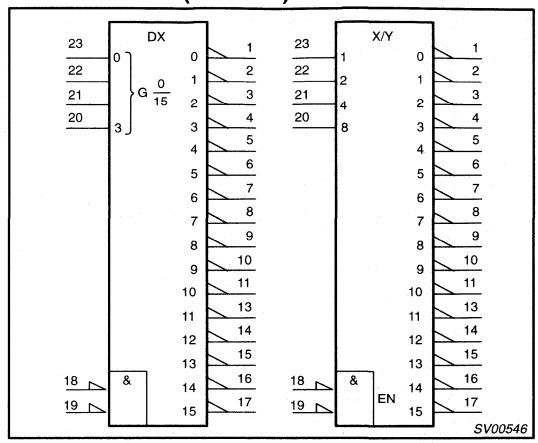
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17	$\overline{Y}_0$ to $\overline{Y}_{15}$	Outputs (active LOW)
18, 19	$\overline{E}_0$, $\overline{E}_1$	Enable inputs (active LOW)
12	GND	Ground (0 V)
23, 22, 21, 20	A_0 to A_3	Address inputs
16	V_{CC}	Positive supply voltage

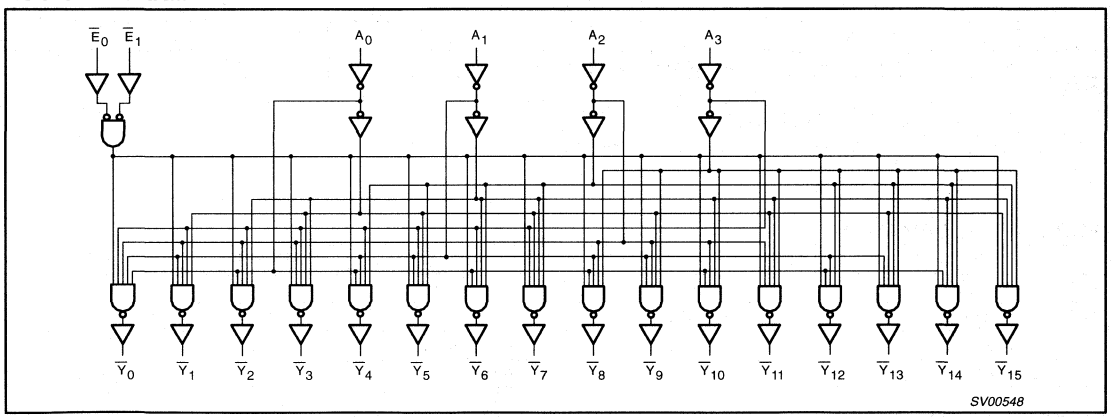
LOGIC SYMBOL



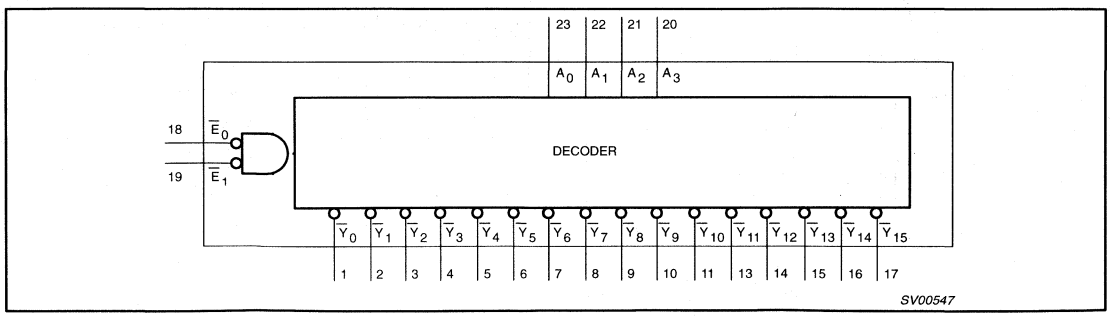
LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTIONAL DIAGRAM



FUNCTION TABLE

		INPUTS				OUTPUTS														
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$	$\overline{Y}_8$	$\overline{Y}_9$	$\overline{Y}_{10}$	$\overline{Y}_{11}$	$\overline{Y}_{12}$	$\overline{Y}_{13}$	$\overline{Y}_{14}$	$\overline{Y}_{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND			1.0		1.0	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V			500		850	μA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay A_n to $\overline{Y}_n$	Figures 1, 2	1.2		65				ns
			2.0		22	43		51	
			2.7		16	31		38	
			3.0 to 3.6		12[2]	25		30	
t_{PHL}/t_{PLH}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	Figures 1, 2	1.2		70				ns
			2.0		24	44		54	
			2.7		18	33		40	
			3.0 to 3.6		13[2]	26		32	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C.
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

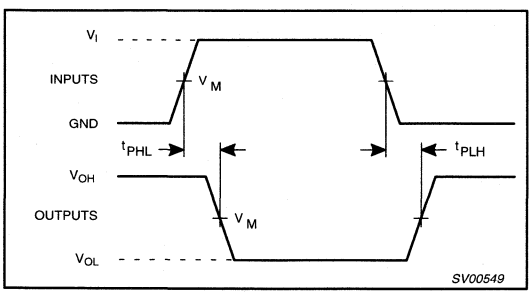


Figure 1. Address input (A_n) to output ($\overline{Y}_n$) propagation delays.

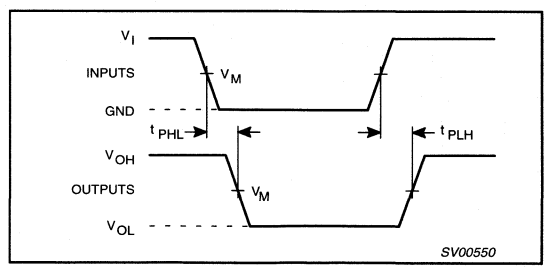
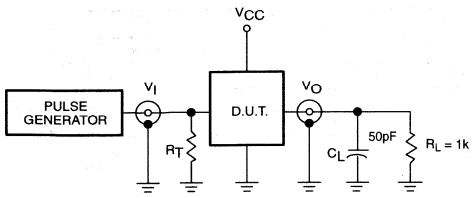


Figure 2. Enable input ($\overline{E}_n$) to output ($\overline{Y}_n$) propagation delays.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00901

Figure 3. Load circuitry for switching times.

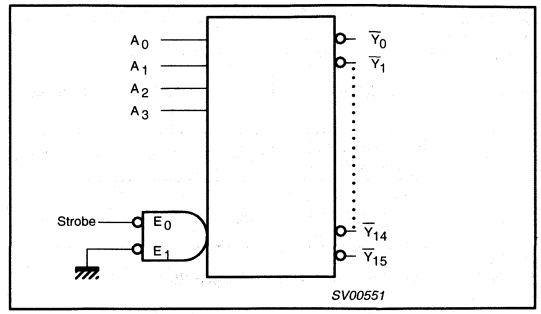


Figure 4. 1-of-16 decoder; LOW level output is selected.

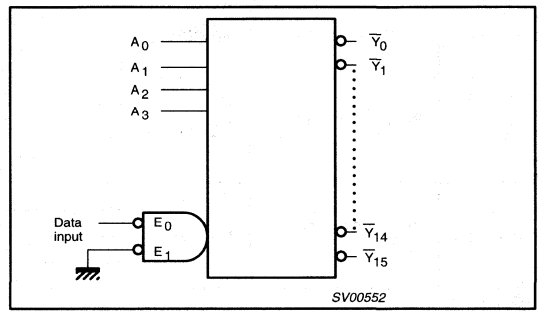


Figure 5. 1-of-16 demultiplexer; logic level on selected outputs follow the logic level on the data input.

Quad 2-input multiplexer 74LV157

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV157 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT157.

The 74LV157 is a quad 2-input multiplexer which selects 4 bits of data from two sources under the control of a common data select input (S).

The four outputs present the selected data in the true (non-inverted) form. The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the 74LV157. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The 74LV157 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nI_0, nI_1, to nY $\overline{E}$ to nY S to nY	C_L = 15 pF; V_{CC} = 3.3 V	10 11 12	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	70	pF

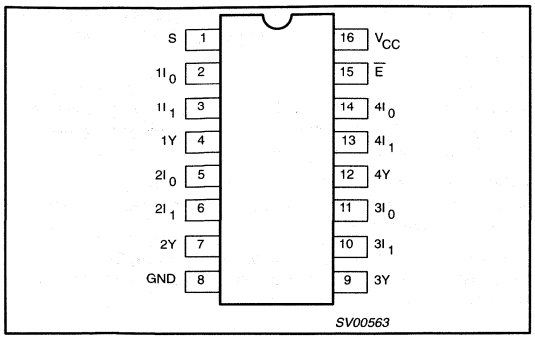
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

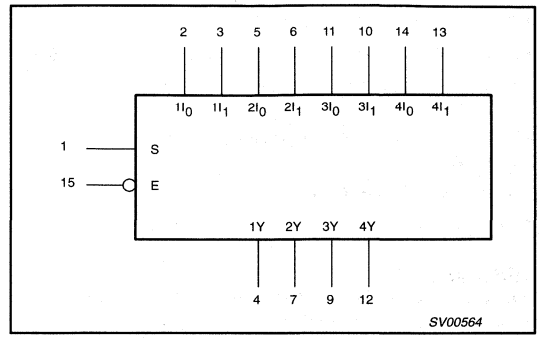
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV157 N	74LV157 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV157 D	74LV157 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV157 DB	74LV157 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV157 PW	74LV157PW DH	SOT403-1

PIN CONFIGURATION



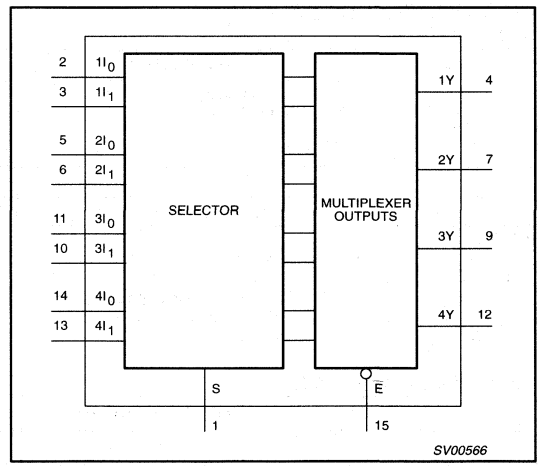
LOGIC SYMBOL



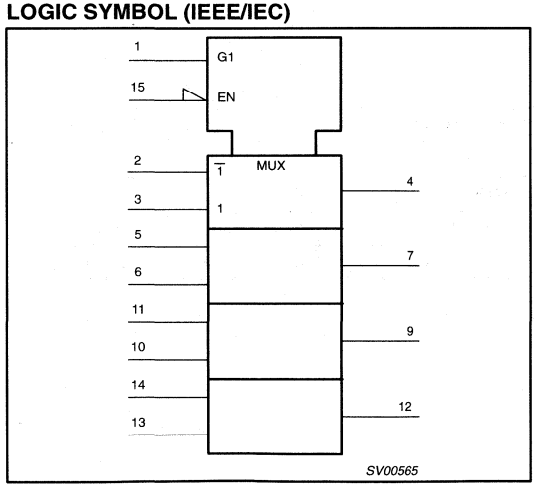
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	S	Common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	Data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	Data inputs from source 1
4, 7, 9, 12	1Y to 4Y	Multiplexer outputs
8	GND	Ground (0 V)
15	$\overline{E}$	Enable inputs (active LOW)
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nI_0 to nY; nI_1 to nY	Figures 1, 2	1.2		65				ns
			2.0		22	43		51	
			2.7		16	31		38	
			3.0 to 3.6		12[2]	25		30	
t_{PHL}/t_{PLH}	Propagation delay $\overline{E}$ to nY	Figures 1, 2	1.2		70				ns
			2.0		24	44		54	
			2.7		18	33		40	
			3.0 to 3.6		13[2]	26		32	
t_{PHL}/t_{PLH}	Propagation delay S to nY	Figures 1, 2	1.2		75				ns
			2.0		26	49		60	
			2.7		19	36		44	
			3.0 to 3.6		14[2]	29		35	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
V_M = 0.5 V × V_{CC} at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

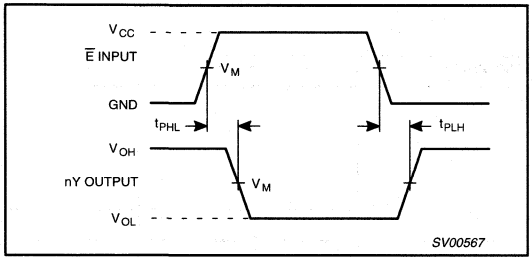


Figure 1. Enable input ($\overline{E}$) to output (nY) propagation delays and output transition times.

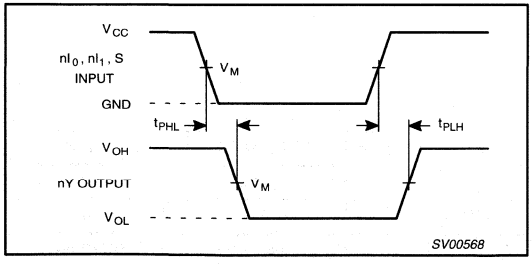
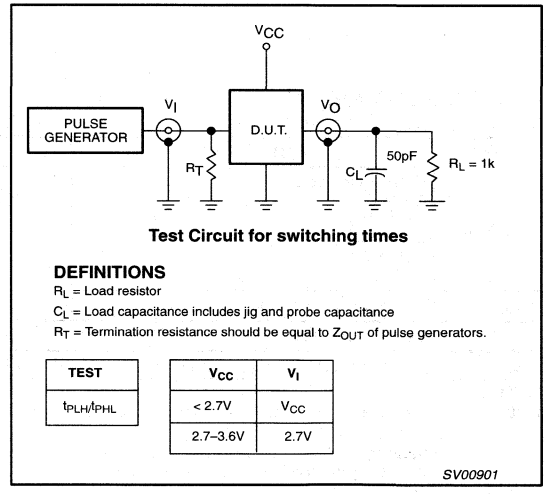


Figure 2. Data inputs (nI_n) and common data select input (S) to output (nY) propagation delays.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V

Figure 3. Load circuitry for switching times.

Presettable synchronous 4-bit binary counter; asynchronous reset

74LV161

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Asynchronous reset
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV161 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT161.

The 74LV161 is a synchronous presettable binary counter which features an internal look-head carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascading stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{tp_{(max)}\ (CP\ to\ TC) + t_{su}(CEP\ to\ CP)}$$

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n CP to TC $\overline{MR}$ to Q_n $\overline{MR}$ to TC CET to TC	C_L = 15 pF; V_{CC} = 3.3 V	 15 18 15 17 9	ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

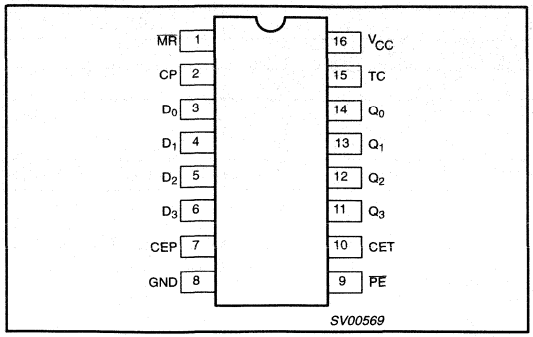
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV161 N	74LV161 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV161 D	74LV161 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV161 DB	74LV161 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV161 PW	74LV161PW DH	SOT403-1

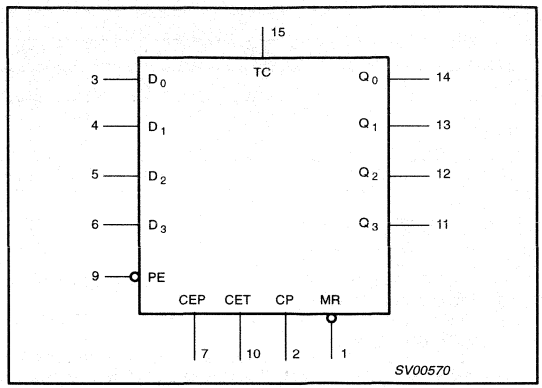
Presettable synchronous 4-bit binary counter; asynchronous reset

74LV161

PIN CONFIGURATION



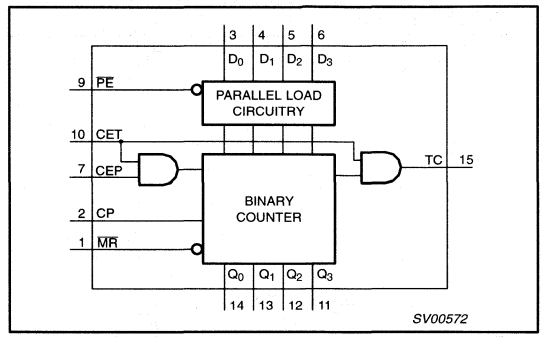
LOGIC SYMBOL



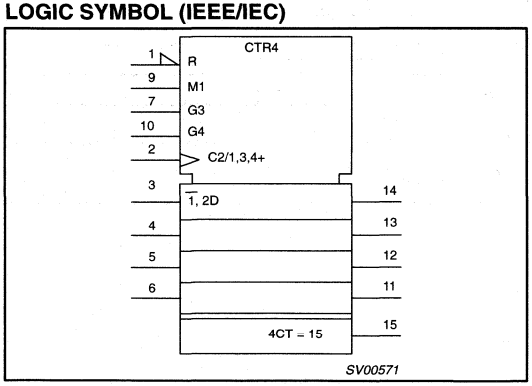
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	Asynchronous master reset (active LOW)
2	CP	Clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	Data inputs
7	CEP	Count enable inputs
8	GND	Ground (0 V)
9	$\overline{PE}$	Parallel enable input (active LOW)
10	CET	Count enable carry input
14, 13, 12, 11	Q_0 to Q_3	Flip-flop outputs
15	TC	Terminal count output
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



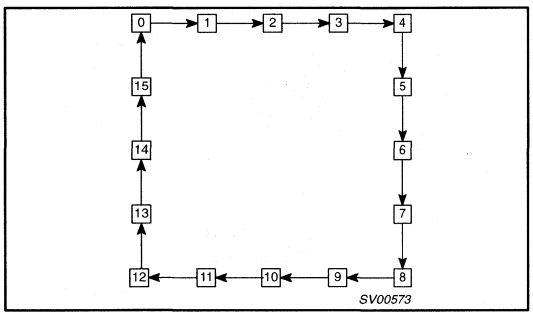
FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
Count	H	↑	h	h	h	X	Count	*
Hold (do nothing)	H	X	l	X	h	X	q_n	*
	H	X	X	l	h	X	q_n	L

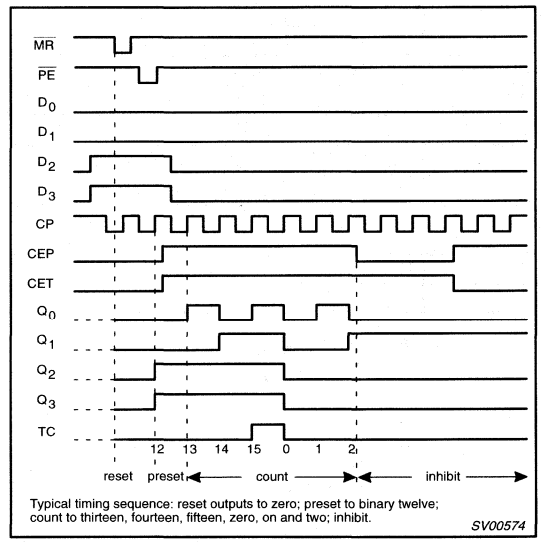
NOTES:

* = The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH)
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

STATE DIAGRAM

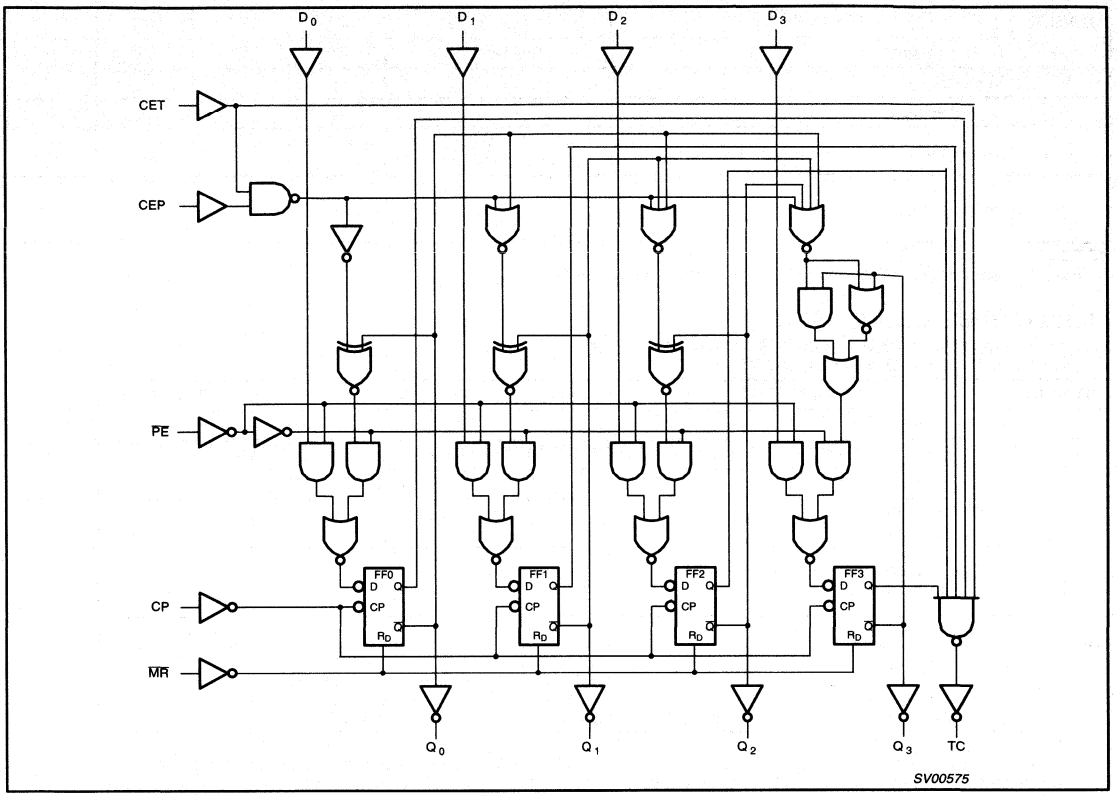


TYPICAL TIMING SEQUENCE



Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, on and two; inhibit.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V			500		850	μA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	Figures 1, 6	1.2		95				ns
			2.0		32	61		75	
			2.7		24	45		55	
			3.0 to 3.6		18[2]	36		44	
t_{PHL}/t_{PLH}	Propagation delay CP to TC	Figures 1, 6	1.2		115				ns
			2.0		39	75		90	
			2.7		29	55		66	
			3.0 to 3.6		22[2]	44		53	
t_{PHL}/t_{PLH}	Propagation delay $\overline{MR}$ to Q_n	Figures 2, 6	1.2		95				ns
			2.0		32	61		75	
			2.7		24	45		55	
			3.0 to 3.6		18[2]	36		44	
t_{PHL}/t_{PLH}	Propagation delay $\overline{MR}$ to TC	Figures 2, 6	1.2		105				ns
			2.0		36	68		82	
			2.7		26	50		60	
			3.0 to 3.6		20[2]	40		48	
t_{PHL}/t_{PLH}	Propagation delay CET to TC	Figures 3, 6	1.2		55				ns
			2.0		19	36		44	
			2.7		14	26		33	
			3.0 to 3.6		10[2]	21		26	
t_w	Clock pulse width HIGH or LOW	Figures 1, 6	2.0	34	10		41		ns
			2.7	25	8		30		
			3.0 to 3.6	20	6[2]		24		
t_w	Master reset width; LOW	Figures 2, 6	2.0	34	14		41		ns
			2.7	25	10		30		
			3.0 to 3.6	20	8[2]		24		
t_{rem}	Removal time $\overline{MR}$ to CP	Figures 2, 6	1.2		25				ns
			2.0	22	9		26		
			2.7	16	6		19		
			3.0 to 3.6	13	5[2]		15		
t_{su}	Set-up time D_n to CP	Figures 4, 6	1.2		25				ns
			2.0	22	9		26		
			2.7	16	6		19		
			3.0 to 3.6	13	5[2]		15		
t_{su}	Set-up time $\overline{PE}$ to CP	Figures 4, 6	1.2		30				ns
			2.0	22	10		26		
			2.7	16	8		19		
			3.0 to 3.6	13	6[2]		15		
t_{su}	Set-up time CEP, CET to CP	Figures 5, 6	1.2		30				ns
			2.0	22	10		26		
			2.7	16	8		19		
			3.0 to 3.6	13	6[2]		15		

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_h	Hold time D_n, $\overline{PE}$, CEP, CET to CP	Figures 4 – 6	1.2		–35				ns
			2.0	0	–12		0		
			2.7	0	–9		0		
			3.0 to 3.6	0	–7[2]		0		
f_{max}	Maximum clock pulse frequency	Figures 1, 6	2.0	14	40		12		MHz
			2.7	19	58		16		
			3.0 to 3.6	24	70		20		

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

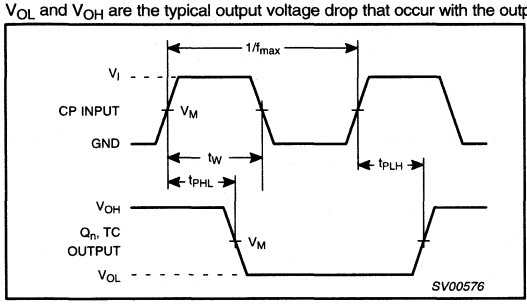


Figure 1. Clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width and the maximum clock frequency.

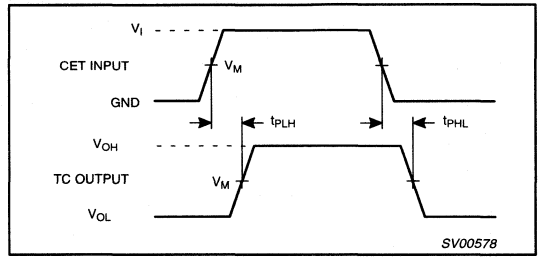


Figure 3. Input (CET) to output (TC) propagation delays.

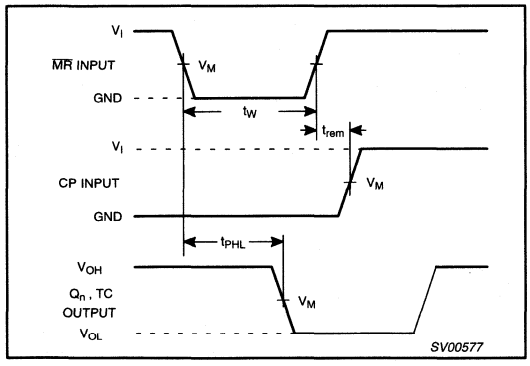


Figure 2. Master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n, TC) propagation delays and the master reset to clock (CP) removal times.

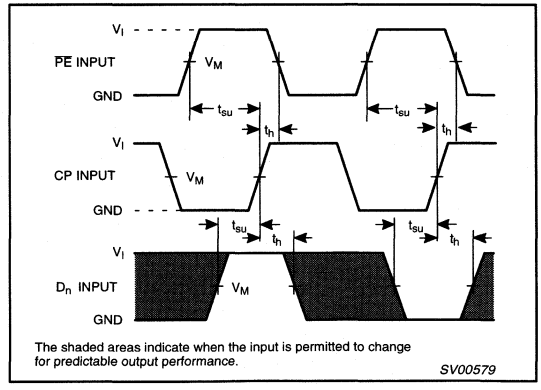


Figure 4. Set-up and hold times for input (D_n) and parallel enable input ($\overline{PE}$).

AC WAVEFORMS (Continued)

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

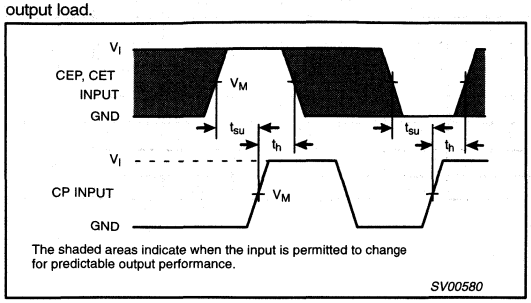


Figure 5. CEP and CET set-up and hold times.

TEST CIRCUIT

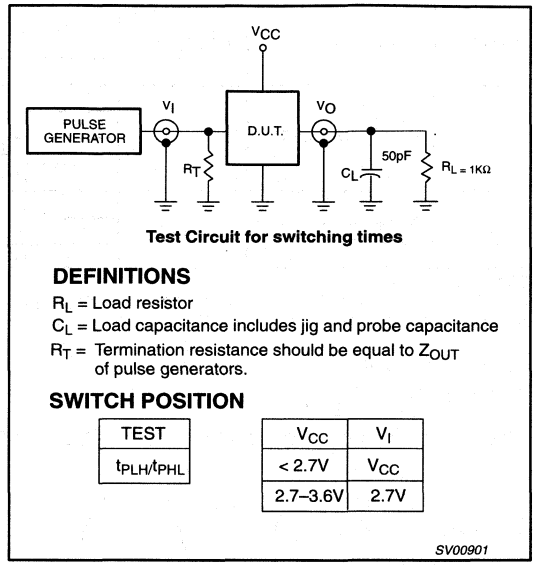


Figure 6. Load circuitry for switching times.

Presettable synchronous 4-bit binary counter; synchronous reset

74LV163

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive-edge triggered clock
- Synchronous reset
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV163 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT163.

The 74LV163 is a synchronous presettable binary counter which features an internal look-head carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input ($\overline{PE}$) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold time requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input ($\overline{MR}$) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for $\overline{MR}$ are met).

This action occurs regardless of the levels at $\overline{PE}$, CET and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate. The look ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascading stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{tp_{(max)}\ (CP\ to\ TC) + t_{su}(CEP\ to\ CP)}$$

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n CP to TC CET to TC	C_L = 15 pF; V_{CC} = 3.3 V	 15 18 9	ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

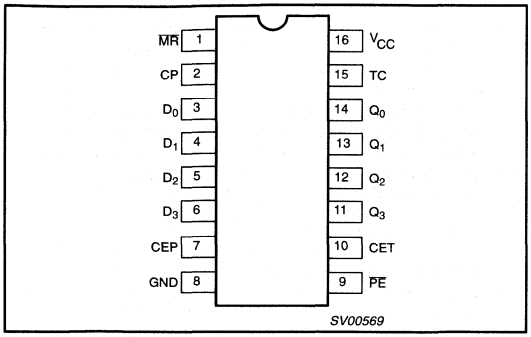
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV163 N	74LV163 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV163 D	74LV163 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV163 DB	74LV163 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV163 PW	74LV163PW DH	SOT403-1

Presettable synchronous 4-bit binary counter; synchronous reset

74LV163

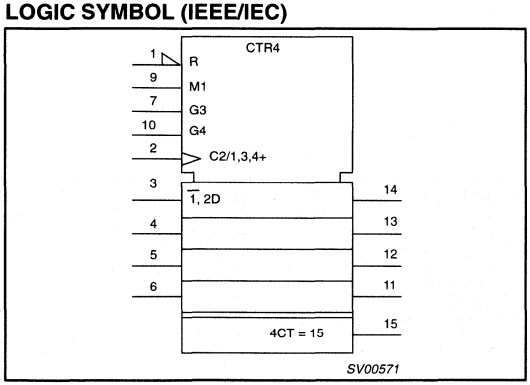
PIN CONFIGURATION



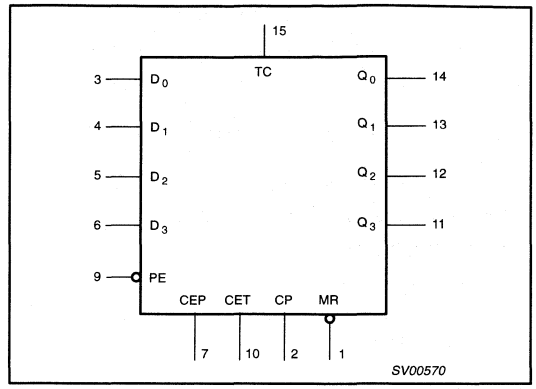
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	Asynchronous master reset (active LOW)
2	CP	Clock input (LOW-to-HIGH, edge-triggered)
3, 4, 5, 6	D_0 to D_3	Data inputs
7	CEP	Count enable inputs
8	GND	Ground (0 V)
9	$\overline{PE}$	Parallel enable input (active LOW)
10	CET	Count enable carry input
14, 13, 12, 11	Q_0 to Q_3	Flip-flop outputs
15	TC	Terminal count output
16	V_{CC}	Positive supply voltage

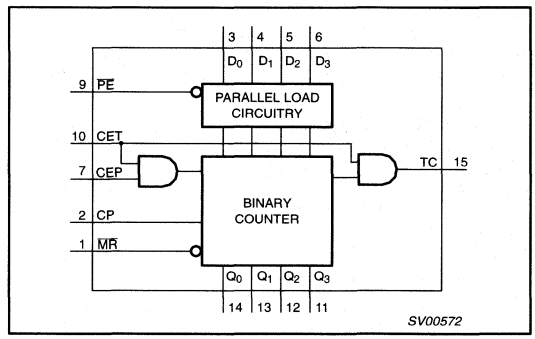
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTIONAL DIAGRAM



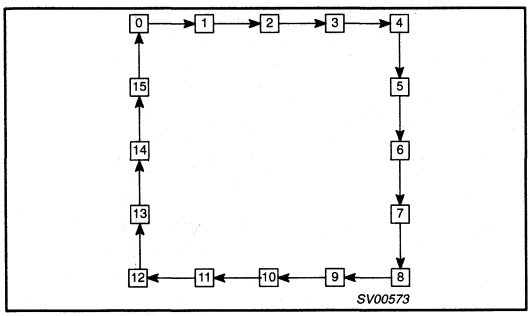
FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
Count	h	↑	h	h	h	X	Count	*
Hold (do nothing)	h	X	l	X	h	X	q_n	*
	h	X	X	l	h	X	q_n	L

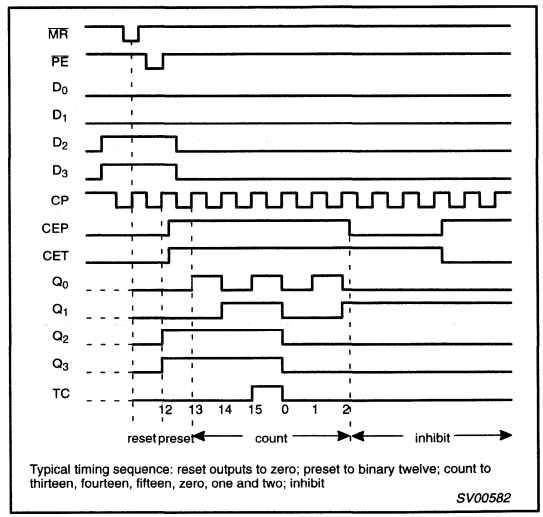
NOTES:

* = The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH)
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

STATE DIAGRAM

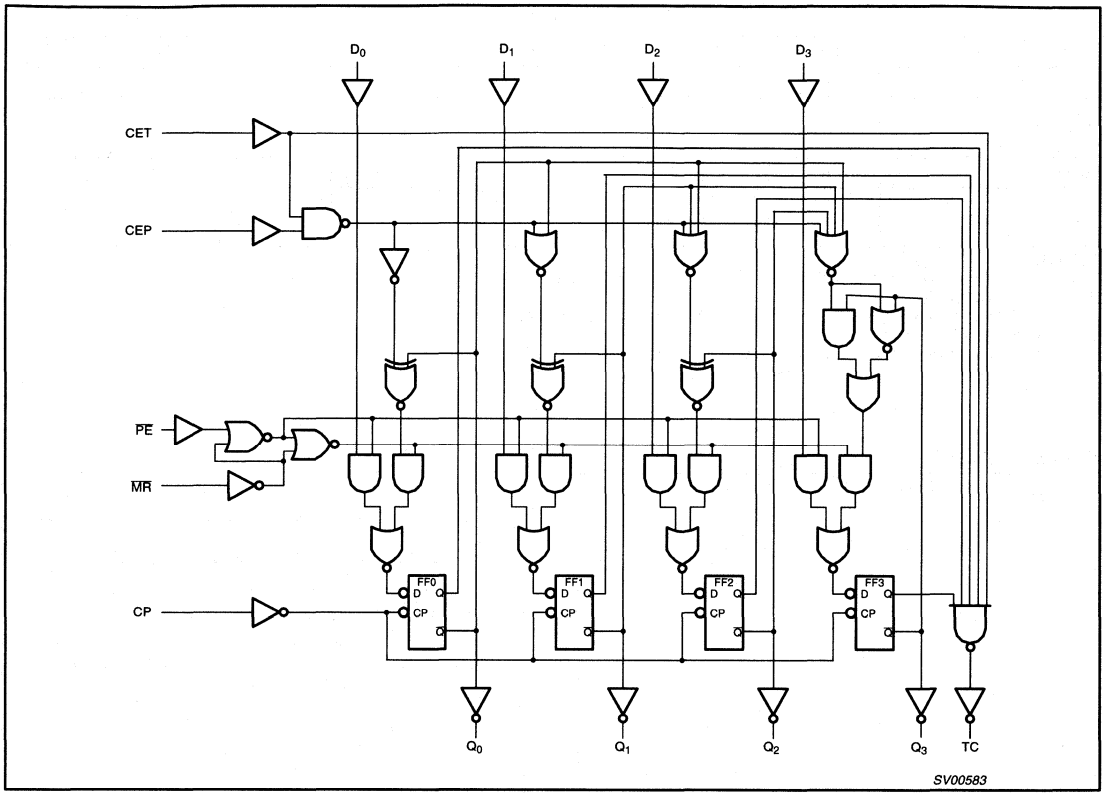


TYPICAL TIMING SEQUENCE



Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V			500		850	μA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	Figures 1	1.2		95				ns
			2.0		32	61		75	
			2.7		24	45		55	
			3.0 to 3.6		18[2]	36		44	
t_{PHL}/t_{PLH}	Propagation delay CP to TC	Figures 1	1.2		115				ns
			2.0		39	75		90	
			2.7		29	55		66	
			3.0 to 3.6		22[2]	44		53	
t_{PHL}/t_{PLH}	Propagation delay CET to TC	Figures 2	1.2		55				ns
			2.0		19	36		44	
			2.7		14	26		33	
			3.0 to 3.6		10[2]	21		26	
t_w	Clock pulse width HIGH or LOW	Figures 1	2.0	34	10		41		ns
			2.7	25	8		30		
			3.0 to 3.6	20	6[2]		24		
t_{su}	Set-up time MR, D_n to CP	Figures 3, 4	1.2		25				ns
			2.0	22	9		26		
			2.7	16	6		19		
			3.0 to 3.6	13	5[2]		15		
t_{su}	Set-up time $\overline{PE}$ to CP	Figures 3	1.2		30				ns
			2.0	22	10		26		
			2.7	16	8		19		
			3.0 to 3.6	13	6[2]		15		
t_{su}	Set-up time CEP, CET to CP	Figures 5	1.2		30				ns
			2.0	22	10		26		
			2.7	16	8		19		
			3.0 to 3.6	13	6[2]		15		
t_h	Hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	Figures 3, 4, 5	1.2		−35				ns
			2.0	0	−12		0		
			2.7	0	−9		0		
			3.0 to 3.6	0	−7		0		
f_{max}	Maximum clock pulse frequency	Figures 1	2.0	14	40		12		MHz
			2.7	19	58		16		
			3.0 to 3.6	24	70		20		

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

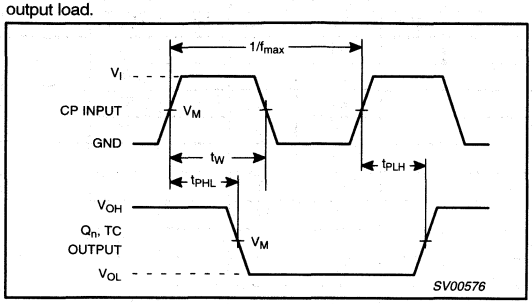


Figure 1. Clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width and the maximum clock frequency.

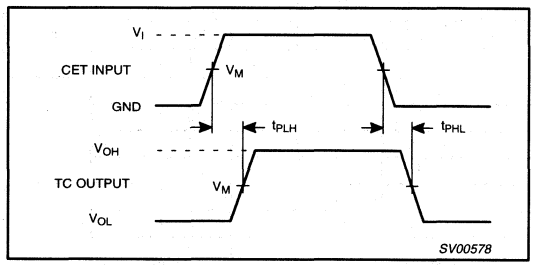


Figure 2. Input (CET) to output (TC) propagation delays and output transition times.

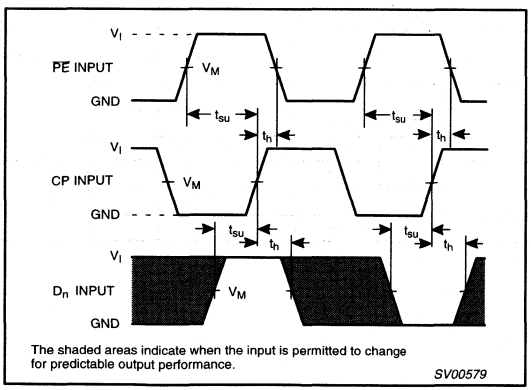


Figure 3. Set-up and hold times for input (D_n) and parallel enable input ($\overline{PE}$).

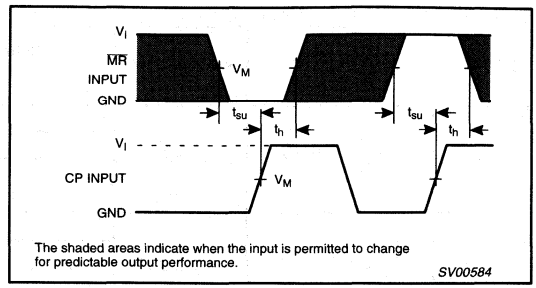


Figure 4. $\overline{MR}$ set-up and hold times.

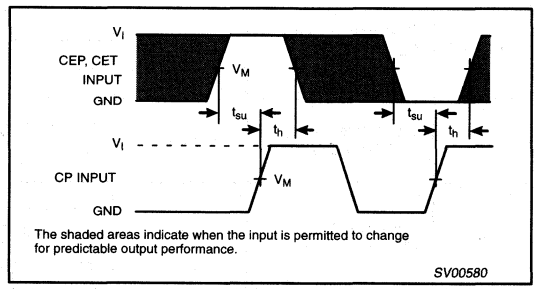
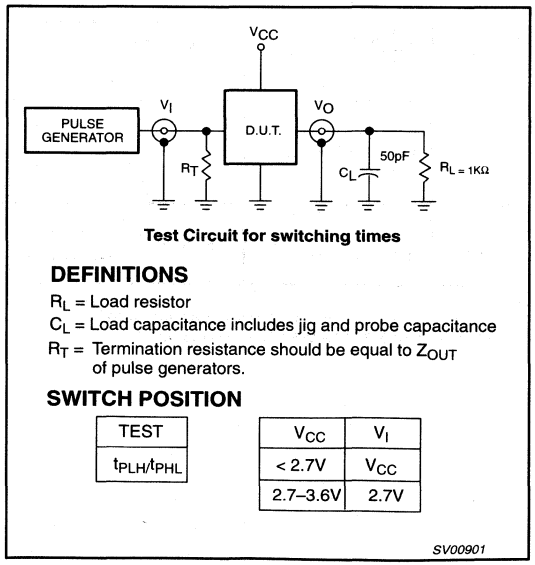


Figure 5. CEP and CET set-up and hold times.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Figure 6. Load circuitry for switching times.

8-bit serial-in/parallel-out shift register 74LV164

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Gated serial data inputs
- Asynchronous master reset
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV164 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT164.

The 74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q_0, which is the logical AND of the two data inputs (D_{sa}, D_{sb}) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n $\overline{MR}$ to Q_n	C_L = 15pF V_{CC} = 3.3V	12 12	ns
f_{max}	Maximum clock frequency		78	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_{CC} = 3.3V Notes 1 and 2	40	pF

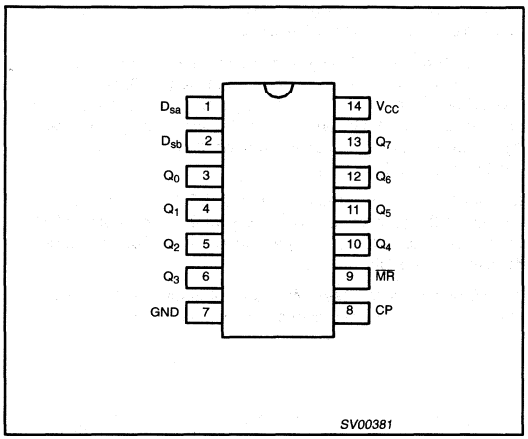
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV164 N	74LV164 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV164 D	74LV164 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV164 DB	74LV164 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV164 PW	74LV164PW DH	SOT402-1

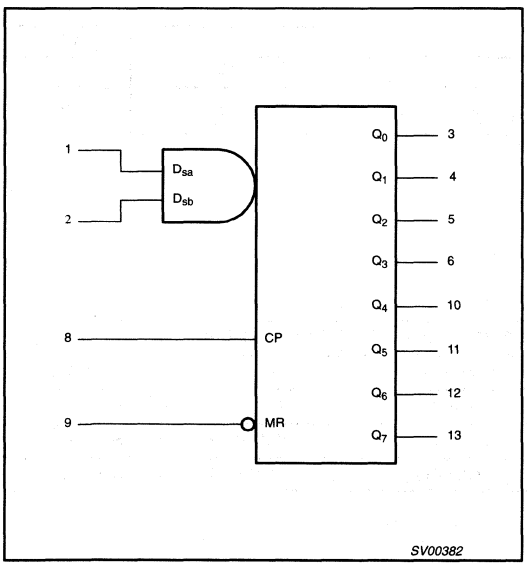
PIN CONFIGURATION



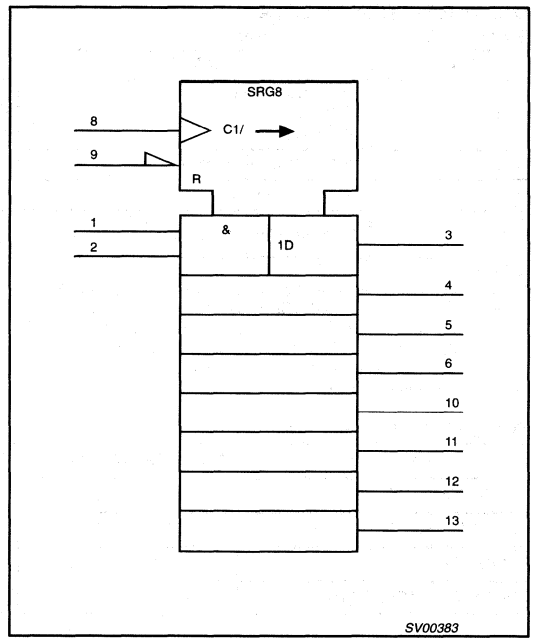
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1,2	D_{sa}, D_{sb}	Data inputs
3, 4, 5, 6, 10, 11, 12, 13	Q_0 to Q_7	Outputs
7	GND	Ground (0V)
8	CP	Clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	Master reset input (active LOW)
14	V_{CC}	Positive supply voltage

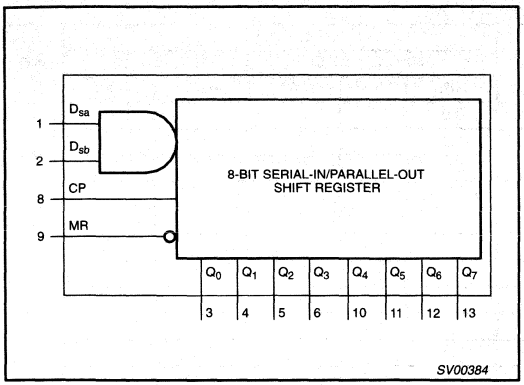
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	$Q_1 - Q_7$
Reset (clear)	L	X	x	x	L	L – L
Shift	H	↑	l	l	L	$q_0 - q_6$
	H	↑	l	h	L	$q_0 - q_6$
	H	↑	h	l	L	$q_0 - q_6$
	H	↑	h	h	H	$q_0 - q_6$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = Lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTES:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} −0.6V			500		850	µA

NOTES:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	Figure 1	1.2	–	75	–	–	–	ns
			2.0	–	26	39	–	49	
			2.7	–	19	29	–	36	
			3.0 to 3.6	–	14[2]	23	–	29	
			4.5 to 5.5	–	12[2]	19	–	24	
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Figure 2	1.2	–	75	–	–	–	ns
			2.0	–	26	39	–	49	
			2.7	–	19	29	–	36	
			3.0 to 3.6	–	14[2]	23	–	29	
			4.5 to 5.5	–	12[2]	19	–	24	
t_W	Clock pulse width HIGH to LOW	Figure 1	2.0	34	9	–	41	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5[2]	–	24	–	
			4.5 to 5.5	13	4[2]		16		
t_W	Master reset pulse width; LOW	Figure 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6[2]	–	24	–	
			4.5 to 5.5	13	5[2]		16		
t_{rem}	Removal time $\overline{MR}$ to CP	Figure 2	1.2	–	30	–	–	–	ns
			2.0	19	10	–	24	–	
			2.7	14	8	–	18	–	
			3.0 to 3.6	11	6[2]	–	14	–	
			4.5 to 5.5	8	5[2]		10		
t_{su}	Set-up time D_{sa}, D_{sb} to CP	Figure 3	1.2	–	15	–	–	–	ns
			2.0	22	5	–	26	–	
			2.7	16	4	–	19	–	
			3.0 to 3.6	13	3[2]	–	15	–	
			4.5 to 5.5	9	2[2]		10		
t_h	Hold time D_{sa}, D_{sb} to CP	Figure 3	1.2	–	–10	–	–	–	ns
			2.0	5	–3	–	5	–	
			2.7	5	–2	–	5	–	
			3.0 to 3.6	5	–2[2]	–	5	–	
			4.5 to 5.5	5	–1[2]		5		
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40	–	12	–	MHz
			2.7	19	58	–	16	–	
			3.0 to 3.6	24	70[2]	–	20	–	
			4.5 to 5.5	36	100[2]		30		

NOTE:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25°C$.
2. Typical value measured at $V_{CC} = 3.3$V.
3. Typical value measured at $V_{CC} = 5.0$V.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V ≤ 3.6V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

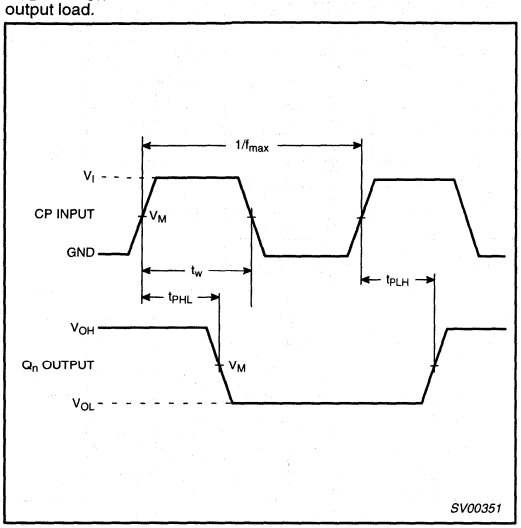


Figure 1. The clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency

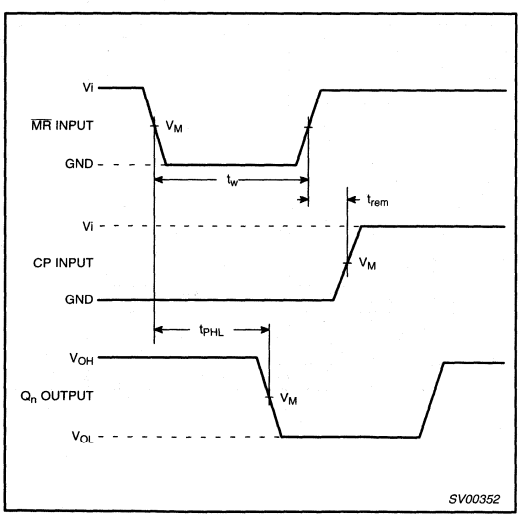


Figure 2. The master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delay and the master reset to clock (CP) removal time

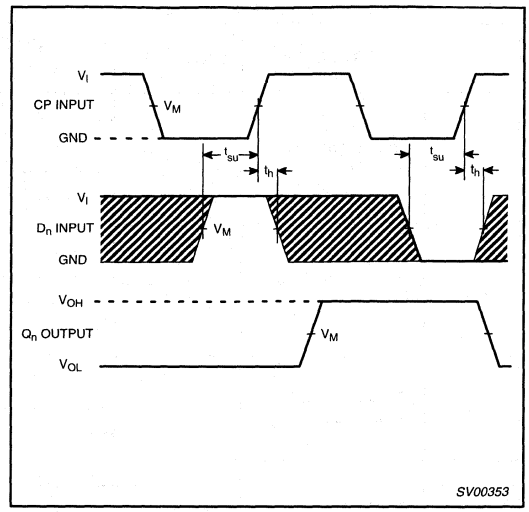
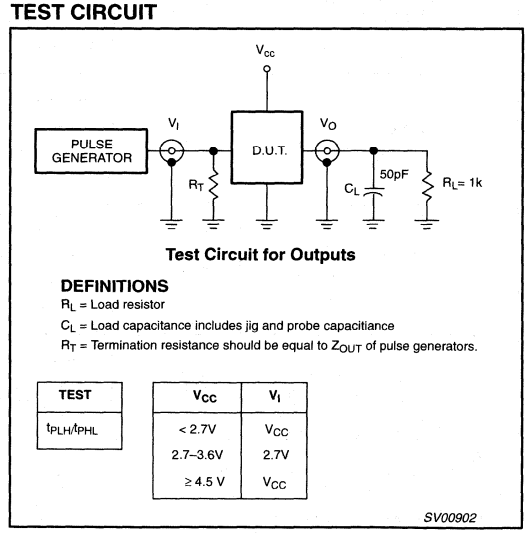


Figure 3. Data set-up and hold times for the D_n inputs

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitiance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V
	≥ 4.5 V	V_{CC}

Figure 4. Load circuitry for switching times

8-bit parallel-in/serial-out shift register | 74LV165

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Asynchronous 8-bit parallel load
- Synchronous serial input
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV165 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT165.

The 74LV165 is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q_7 and $\overline{Q}_7$) available from the last stage. When the parallel load ($\overline{PL}$) input is LOW, parallel data from the D_0 to D_7 inputs are loaded into the register asynchronously. When $\overline{PL}$ is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input $\overline{CE}$ should only take place while CP HIGH for predictable operation. Either the CP or the $\overline{CE}$ should be HIGH before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when $\overline{PL}$ is activated.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$ $\overline{PL}$ to Q_7, $\overline{Q}_7$ D_7 to Q_7, $\overline{Q}_7$	C_L = 15 pF; V_{CC} = 3.3 V	 18 18 14	ns
f_{max}	Maximum clock frequency		78	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	35	pF

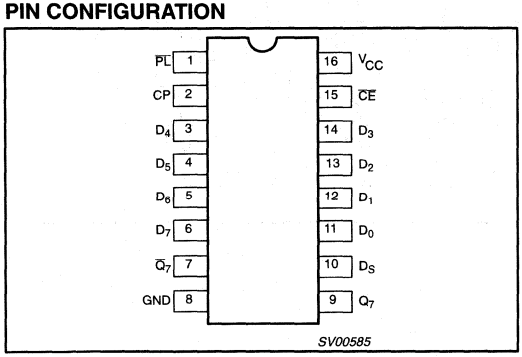
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	−40°C to +125°C	74LV165 N	74LV165 N	SOT38-4
16-Pin Plastic SO	−40°C to +125°C	74LV165 D	74LV165 D	SOT109-1
16-Pin Plastic SSOP Type II	−40°C to +125°C	74LV165 DB	74LV165 DB	SOT338-1
16-Pin Plastic TSSOP Type I	−40°C to +125°C	74LV165 PW	74LV165PW DH	SOT403-1

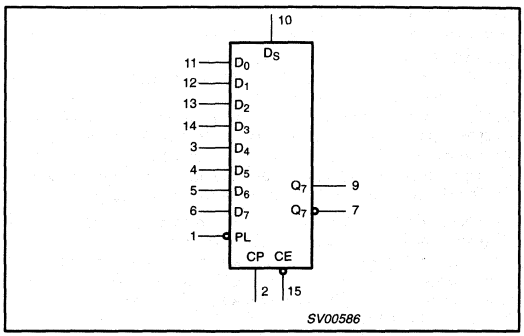
PIN CONFIGURATION



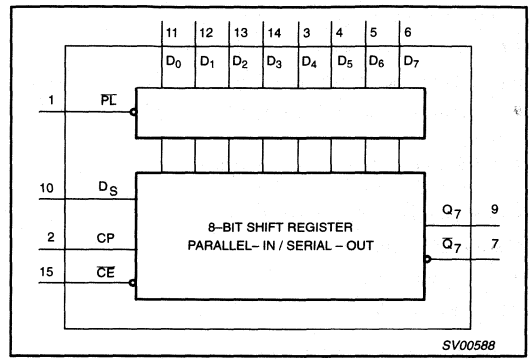
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{PL}$	Asynchronous parallel load input (active LOW)
2	CP	Clock input (LOW to HIGH, edge-triggered)
7	$\overline{Q}_7$	Complementary output from the last stage
8	GND	Ground (0 V)
9	Q_7	Serial output from last stage
10	D_S	Serial data input
11, 12, 13, 14, 3, 4, 5, 6	D_0 to D_7	Parallel data inputs
15	$\overline{CE}$	Clock enable input (active LOW)
16	V_{CC}	Positive supply voltage

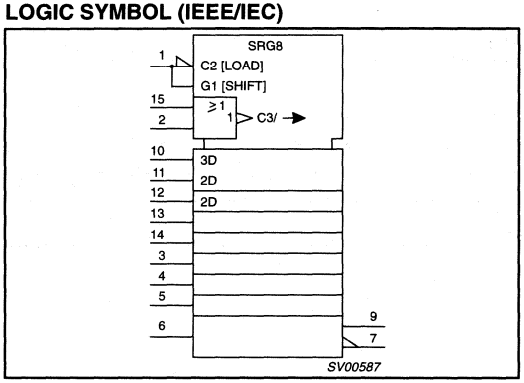
LOGIC SYMBOL



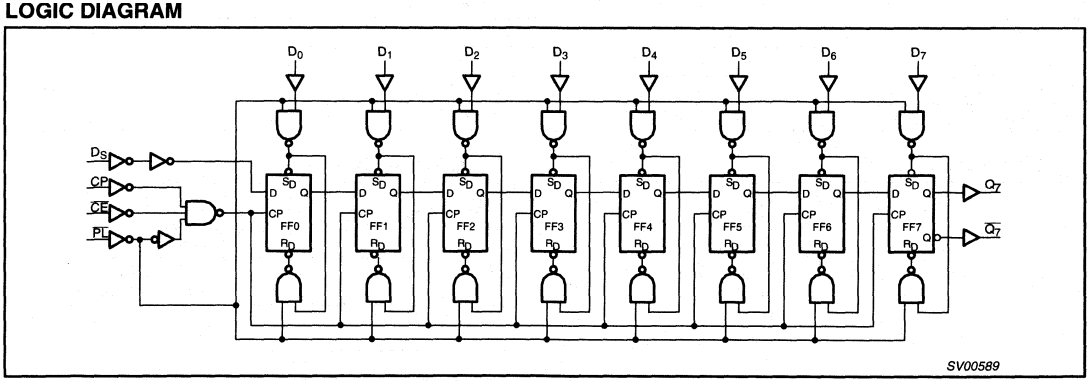
FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS					Qn REGISTERS		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	D_S	D_0–D_7	Q_0	Q_1–Q_6	Q_7	$\overline{Q}_7$
Parallel load	L	X	X	X	L	L	L–L	L	H
	L	X	X	X	H	H	H–H	H	L
Serial Shift	H	L	↑	l	X	L	q_0–q_5	q_6	$\overline{q}_6$
	H	L	↑	h	X	H	q_0–q_5	q_6	$\overline{q}_6$
Hold "do nothing"	H	H	X	X	X	q_0	q_1–q_6	q_7	q_7

NOTES:
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 to 5.5 V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PLH}/t_{PHL}	Propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$	Figures 1, 2	1.2	–	115		–		ns
			2.0	–	38	61	–	76	
			2.7	–	27	43	–	54	
			3.0 to 3.6	–	22[2]	36	–	45	
			4.5 to 5.5	–	15	24	–	30	
t_{PLH}/t_{PHL}	Propagation delay $\overline{PL}$ to Q_7, $\overline{Q}_7$	Figures 1, 2	1.2	–	110		–		ns
			2.0	–	35	56	–	70	
			2.7	–	24	39	–	49	
			3.0 to 3.6	–	20[2]	33	–	41	
			4.5 to 5.5	–	14	22	–	27	
t_{PLH}/t_{PHL}	Propagation delay D_7 to Q_7, $\overline{Q}_7$	Figures 1, 2	1.2	–	90		–		ns
			2.0	–	28	45	–	56	
			2.7	–	20	32	–	40	
			3.0 to 3.6	–	17[2]	27	–	33	
			4.5 to 5.5	–	11	18	–	22	
t_w	Clock Pulse width HIGH or LOW	Figures 1, 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	7[2]	–	24	–	
			4.5 to 5.5	15	5	–	18	–	
t_w	Parallel load pulse width LOW	Figures 1, 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	7[2]	–	24	–	
			4.5 to 5.5	15	5	–	18	–	
t_{rem}	Removal time $\overline{PL}$ to CP, $\overline{CE}$	Figures 1, 2	1.2	–	40	–	–	–	ns
			2.0	24	15	–	30	–	
			2.7	18	11	–	23	–	
			3.0 to 3.6	17	10[2]	–	21	–	
			4.5 to 5.5	12	7	–	15	–	
t_{su}	Set-up time D_S to CP, $\overline{CE}$	Figures 1, 2	1.2	–	−8	–	–	–	ns
			2.0	22	−2	–	26	–	
			2.7	16	−1	–	19	–	
			3.0 to 3.6	13	−1[2]	–	15	–	
			4.5 to 5.5	9	0	–	10	–	
t_{su}	Set-up time $\overline{CE}$ to CP; CP to $\overline{CE}$	Figures 1, 2	1.2	–	20	–	–	–	ns
			2.0	22	7	–	26	–	
			2.7	16	5	–	19	–	
			3.0 to 3.6	13	4[2]	–	15	–	
			4.5 to 5.5	9	3	–	10	–	

AC CHARACTERISTICS (*Continued*)

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	–40 to +85 °C			–40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{su}	Set-up time D_n to $\overline{PL}$	Figures 1, 2	1.2	–	25	–	–	–	ns
			2.0	22	8	–	26	–	
			2.7	16	6	–	19	–	
			3.0 to 3.6	13	5[2]	–	15	–	
			4.5 to 5.5	9	4	–	10	–	
t_h	Hold time D_s to CP, $\overline{CE}$ D_n to $\overline{PL}$	Figures 1, 2	1.2	–	20	–	–	–	ns
			2.0	22	7	–	26	–	
			2.7	16	5	–	19	–	
			3.0 to 3.6	13	4	–	15	–	
			4.5 to 5.5	9	3	–	10	–	
t_h	Hold time $\overline{CE}$ to CP, CP to $\overline{CE}$	Figures 1, 2	1.2	–	–30	–	–	–	ns
			2.0	5	–8	–	5	–	
			2.7	5	–6	–	5	–	
			3.0 to 3.6	5	–5[2]	–	5	–	
			4.5 to 5.5	5	–4	–	5	–	
f_{max}	Maximum clock pulse frequency	Figures 1, 2	2.0	14	40	–	12	–	MHz
			2.7	19	60	–	16	–	
			3.0 to 3.6	24	65[2]	–	20	–	
			4.5 to 5.5	36	75	–	30	–	

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V.
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

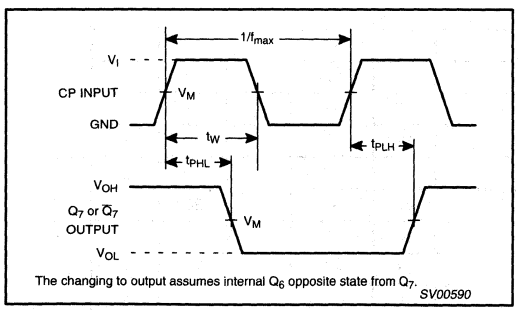


Figure 1. Clock (CP) to output (Q_7 or $\overline{Q}_7$) propagation delays, the clock pulse width and the maximum clock frequency.

Note to Figures 1 and 2

The changing to output assumes internal Q_6 opposite state from Q_7.

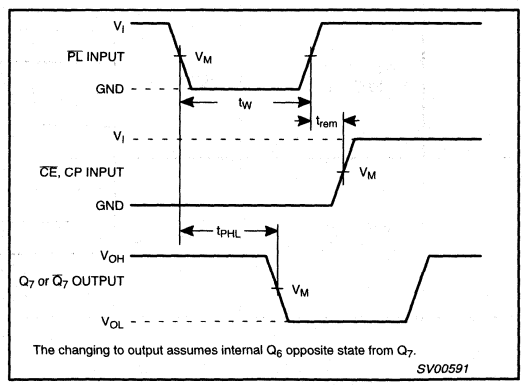


Figure 2. Parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q_7 or $\overline{Q}_7$) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{CE}$) removal time.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

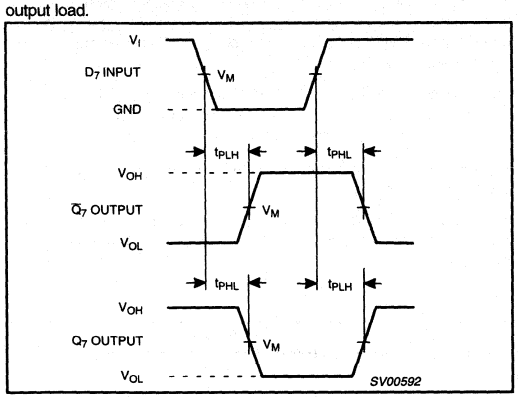
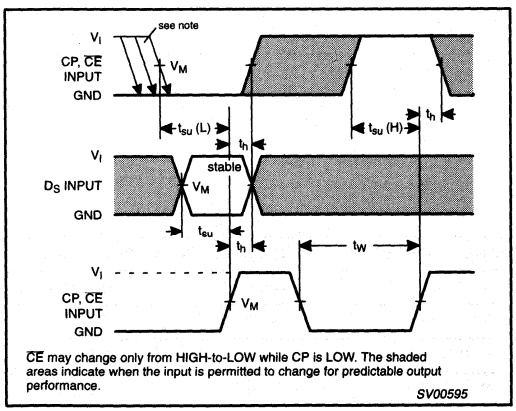


Figure 3. Data input (D_n) to output (Q_7 or $\overline{Q_7}$) propagation delays when $\overline{PL}$ is LOW.



$\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 4. Set-up and hold times from the serial data input (D_S) to the clock (CP) and the clock enable ($\overline{CE}$) inputs, from the clock enable input ($\overline{CE}$) to the clock input (CP) and from the clock input (CP) to the clock enable input ($\overline{CE}$).

Note to Figure 4

$\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

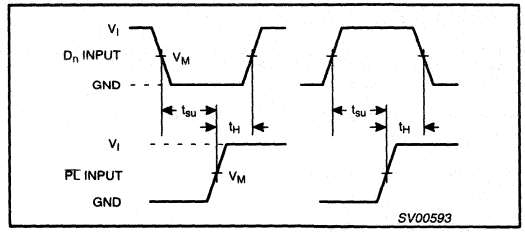
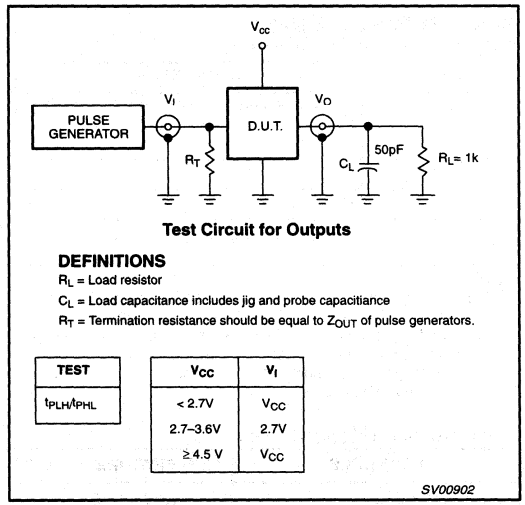


Figure 5. Set-up and hold times from the data inputs (D_n) to the parallel load input ($\overline{PL}$).

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitiance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V
	≥ 4.5 V	V_{CC}

Figure 6. Load circuitry for switching times.

Hex D-type flip-flop with reset; positive edge-trigger 74LV174

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV174 is a low–voltage Si–gate CMOS device and is pin and function compatible with the 74HC/HCT174.

The 74LV174 has six edge–triggered D–type flip–flops with individual D inputs and Q outputs. The common clock (CP) and master reset (MR) inputs load and reset (clear) all flip–flops simultaneously.

The register is fully edge–triggered. The state of each D input, one set–up time prior to the LOW–to–HIGH clock transition, is transferred to the corresponding output of the flip–flop.

A LOW level on the MR input forces all outputs LOW, independently of clock or data inputs.

The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n $\overline{MR}$ to Q_n	C_L = 15pF V_{CC} = 3.3V	16 13	ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_{CC} = 3.3V Notes 1 and 2	17	pF

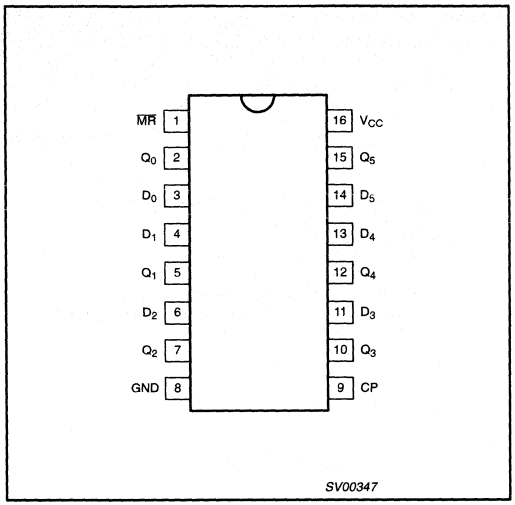
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

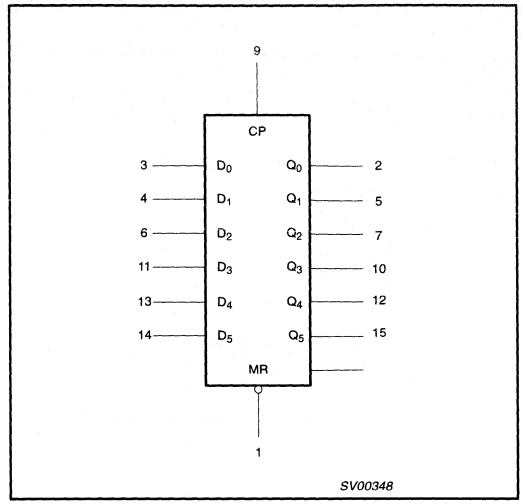
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV174 N	74LV174 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV174 D	74LV174 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV174 DB	74LV174 DB	SOT338-1
16-Pin Plastic TSSOP	–40°C to +125°C	74LV174 PW	74LV174PW DH	SOT403-1

PIN CONFIGURATION



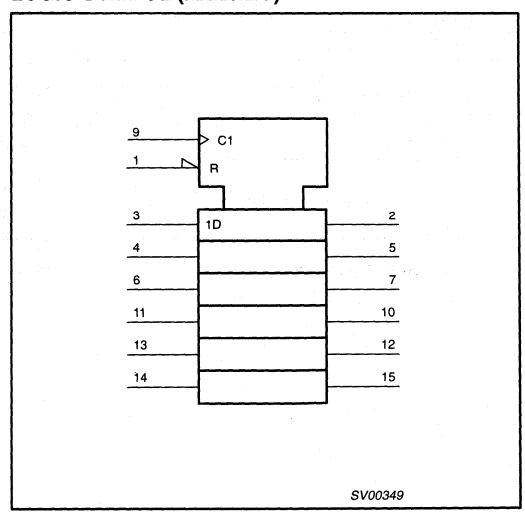
LOGIC SYMBOL



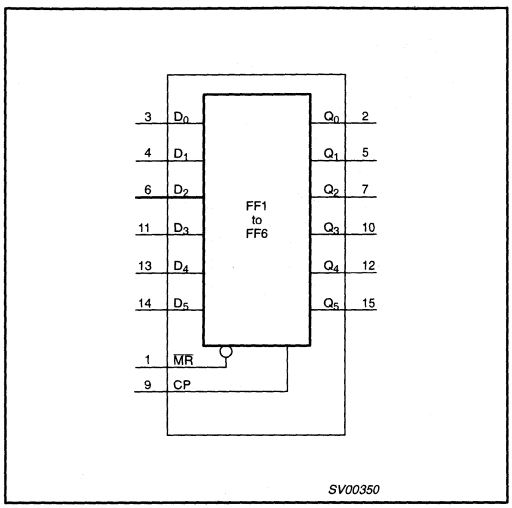
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	Asynchronous master reset (active LOW)
2, 5, 7, 10, 12, 15	Q_0 to Q_5	Flip-flop outputs
3, 4, 6, 11, 13, 14	D_0 to D_5	Data inputs
8	GND	Ground (0V)
9	CP	Clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_0
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = Lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW–to–HIGH clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTES:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	$0.7*V_{CC}$			$0.7*V_{CC}$		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			$0.3*V_{CC}$		$0.3*V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	

DC CHARACTERISTICS FOR THE LV FAMILY (Continued)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f = 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	Figure 1	1.2	–	100	–	–	–	ns
			2.0	–	34	43	–	53	
			2.7	–	25	31	–	39	
			3.0 to 3.6	–	19[2]	25	–	31	
			4.5 to 5.5	–	13[3]	21	–	26	
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Figure 2	1.2	–	80	–	–	–	ns
			2.0	–	27	43	–	53	
			2.7	–	20	31	–	39	
			3.0 to 3.6	–	15[2]	25	–	31	
			4.5 to 5.5	–	11[3]	21	–	26	
t_W	Clock pulse width HIGH to LOW	Figure 1	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6[2]	–	24	–	
			4.5 to 5.5	13	4[3]		16		
t_W	Master reset pulse width LOW	Figure 2	2.0	34	9	–	41	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5	–	24	–	
			4.5 to 5.5	13	4[2]		16		
t_{rem}	Removal time $\overline{MR}$ to CP	Figure 2	1.2	–	–20	–	–	–	ns
			2.0	5	–7	–	5	–	
			2.7	5	–5	–	5	–	
			3.0 to 3.6	5	–4[2]	–	5	–	
			4.5 to 5.5	5	–3[3]		5		
t_{su}	Set-up time D_n to CP	Figure 3	1.2	–	10	–	–	–	ns
			2.0	22	4	–	26	–	
			2.7	16	3	–	19	–	
			3.0 to 3.6	13	2[2]	–	15	–	
			4.5 to 5.5	9	1[3]		10		

AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_h	Hold time D_n to CP	Figure 3	1.2	–	–10	–	–	–	ns
			2.0	5	–4	–	5	–	
			2.7	5	–2	–	5	–	
			3.0 to 3.6	5	–2[2]	–	5	–	
			4.5 to 5.5	5	–1[3]		5		
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40	–	12	–	MHz
			2.7	19	58	–	16	–	
			3.0 to 3.6	24	70[2]	–	20	–	
			4.5 to 5.5	36	100[3]		30		

NOTES:
1. Unless otherwise stated, all typical values are at T_{amb} = 25°C.
2. Typical value measured at V_{CC} = 3.3V.
3. Typical value measured at V_{CC} = 5.0V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V $\leq$ 3.6V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V and $\geq$ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

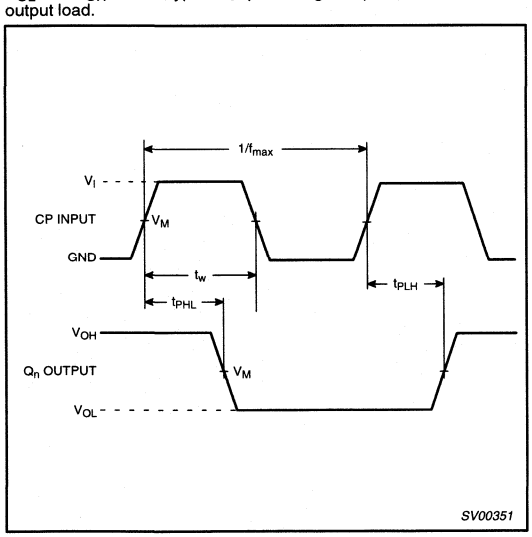


Figure 1. The clock (CP) to output (Q_n) propagation delays, the clock pulse width, and the maximum clock pulse frequency.

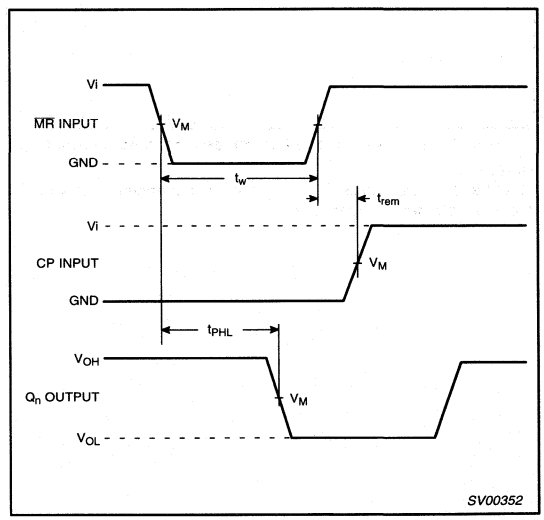


Figure 2. The master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delay and the master reset to clock removal time.

AC WAVEFORMS (Continued)

V_M = 1.5V at $V_{CC} \geq 2.7V \leq 3.6V$
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

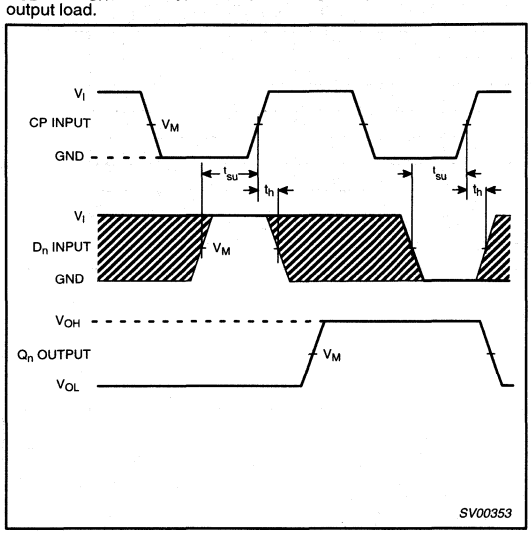


Figure 3. Data set-up and hold times for the data input (D_n).

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT

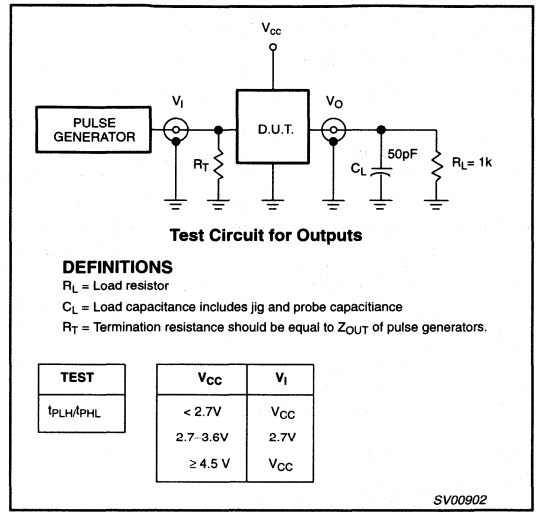


Figure 4. Load circuitry for switching times

Quad D-type flip-flop with reset; positive-edge trigger 74LV175

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Four edge-triggered D flip-flops
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV175 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT175.

The 74LV175 has four edge-triggered, D-type flip-flops with individual D inputs and both Q and $\overline{Q}$ outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time prior to the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All Q_n outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n, $\overline{Q}_n$ $\overline{MR}$ to Q_n, $\overline{Q}_n$	C_L = 15 pF; V_{CC} = 3.3 V	 16 14	 ns ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	32	pF

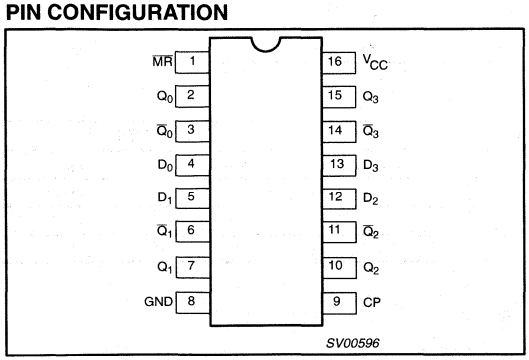
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV175 N	74LV175 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV175 D	74LV175 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV175 DB	74LV175 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV175 PW	74LV175PW DH	SOT403-1

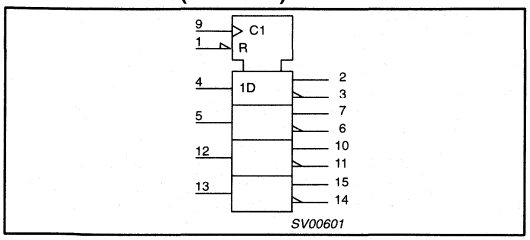
PIN CONFIGURATION



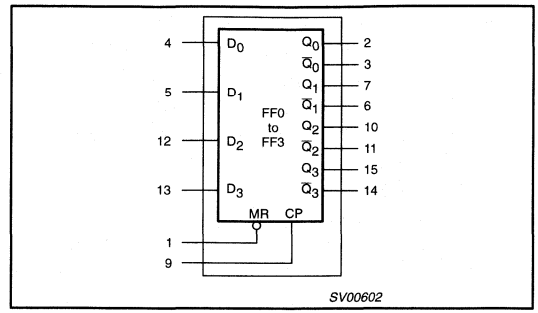
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	Master reset input (active LOW)
2, 7, 10, 15	Q_0 to Q_3	Flip-flop outputs
3, 6, 11, 14	$\overline{Q}_0$ to $\overline{Q}_3$	Complementary flip-flop outputs
4, 5, 12, 13	D_0 to D_3	Data inputs
8	GND	Ground (0 V)
9	CP	Clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	Positive supply voltage

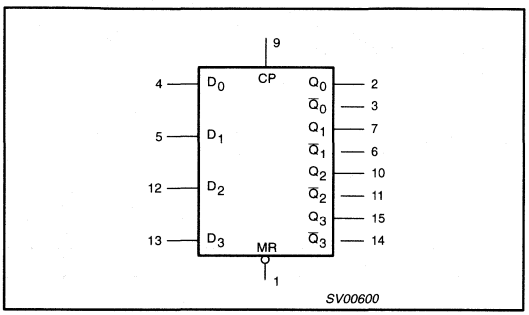
LOGIC SYMBOL (IEEE/IEC)



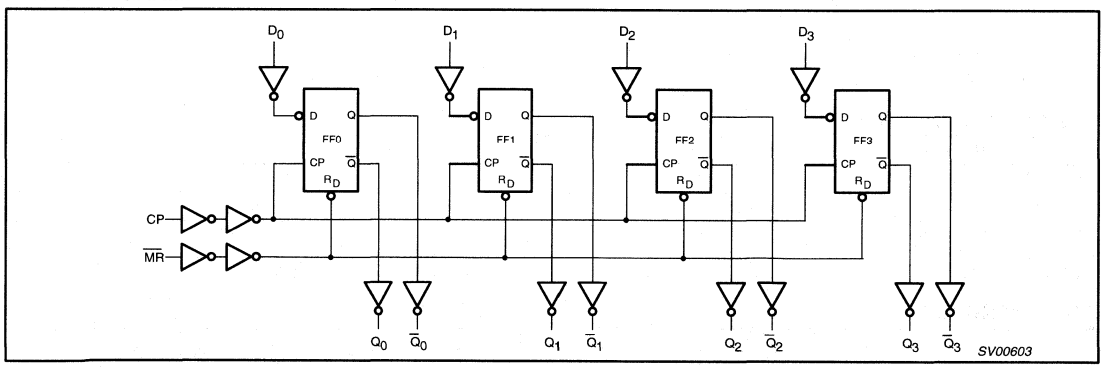
FUNCTIONAL DIAGRAM



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load '1'	H	↑	h	H	L
Load '0'	H	↑	l	L	H

NOTES:

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level level one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition
X = don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC} - 0.6V$			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n, $\overline{Q}_n$	Figures 1	1.2		100				ns
			2.0		34	65		77	
			2.7		25	48		56	
			3.0 to 3.6		19[2]	38		45	
t_{PHL}/t_{PLH}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	Figures 2	1.2		90				ns
			2.0		31	58		70	
			2.7		23	43		51	
			3.0 to 3.6		17[2]	34		41	
t_w	Clock pulse width HIGH or LOW	Figures 1	2.0	34	14		41		ns
			2.7	25	10		30		
			3.0 to 3.6	20	8[2]		24		
t_w	Master reset pulse width LOW	Figures 2	2.0	34	14		41		ns
			2.7	25	9		30		
			3.0 to 3.6	20	7[2]		24		
t_{rem}	Removal time $\overline{MR}$ to CP	Figures 2	1.2		–60				ns
			2.0	5	–20		5		
			2.7	5	–15		5		
			3.0 to 3.6	5	–12[2]		5		
t_{su}	Set-up time D_n to CP	Figures 3	1.2		5				ns
			2.0	22	2		26		
			2.7	16	2		19		
			3.0 to 3.6	13	1[2]		15		
t_h	Hold time D_n to CP	Figures 3	1.2		–5				ns
			2.0	5	–1		5		
			2.7	5	0		5		
			3.0 to 3.6	5	0[2]		5		
f_{max}	Maximum clock pulse frequency	Figures 1	2.0	14	40		12		MHz
			2.7	19	58		16		
			3.0 to 3.6	24	70[2]		20		

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$.
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq 2.7$ V;
$V_M = 0.5\ V \times V_{CC}$ at $V_{CC} < 2.7$ V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

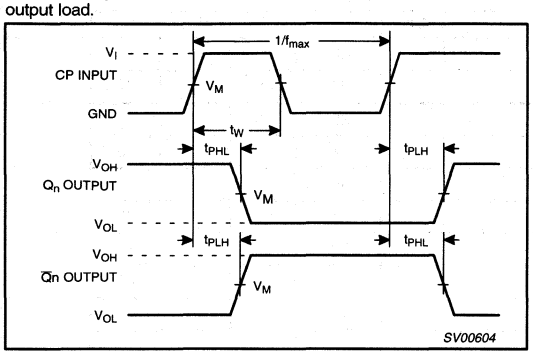


Figure 1. Clock (CP) to outputs (Q_n, $\overline{Q}_n$) propagation delays, the clock pulse width and the maximum clock pulse frequency.

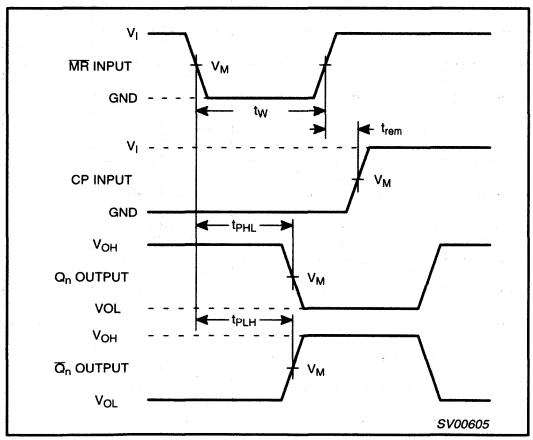


Figure 2. Master reset ($\overline{MR}$) pulse width, the master reset to outputs (Q_n, $\overline{Q}_n$) propagation delay and master reset to clock (CP) removal time.

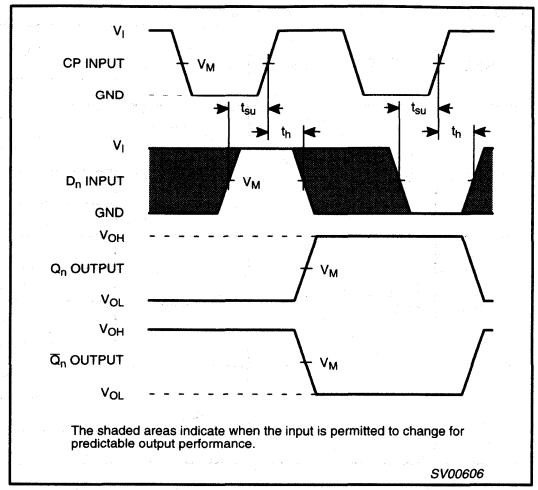


Figure 3. Data set-up and hold times for data input (D_n).

TEST CIRCUIT

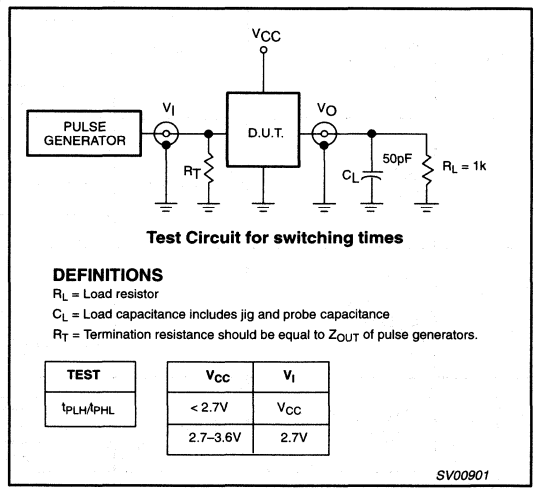


Figure 4. Load circuitry for switching times.

Octal buffer/line driver; inverting (3-State) 74LV240

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV240 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT240.

The 74LV240 is an octal inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The 74LV240 is identical to the 74LV244 but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 3.3 V	9.0	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3 V; V_I = GND to V_{CC}[1]	30	pF

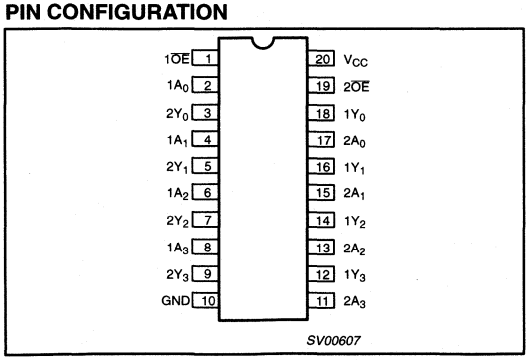
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

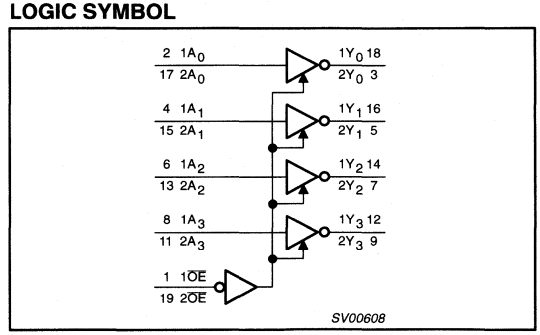
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV240 N	74LV240 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV240 D	74LV240 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV240 DB	74LV240 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV240 PW	74LV240PW DH	SOT360-1

PIN CONFIGURATION



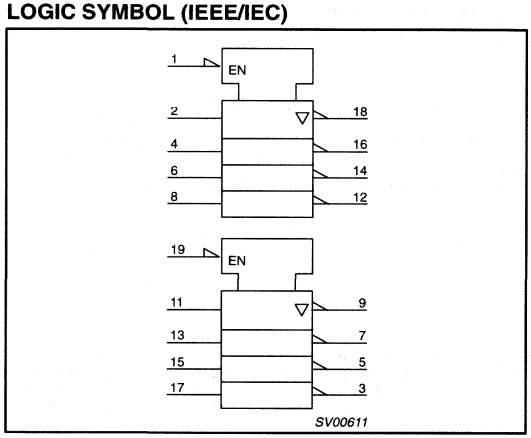
LOGIC SYMBOL



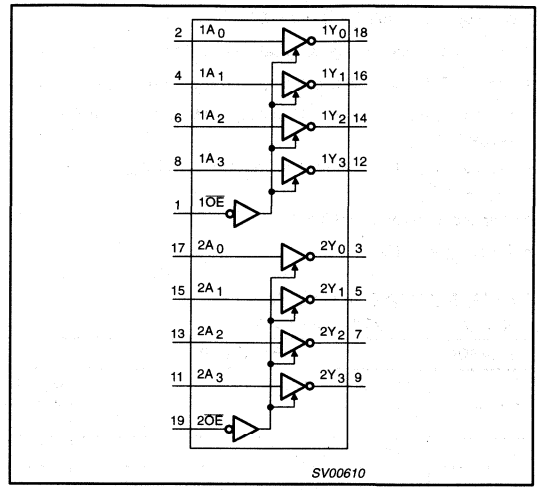
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	Data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	Bus outputs
10	GND	Ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	Data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	Bus outputs
19	$2\overline{OE}$	Output enable input (active LOW)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	Figures 1	1.2		55				ns
			2.0		19	24		31	
			2.7		14	18		23	
			3.0 to 3.6		10[2]	14		18	
			4.5 to 5.5			12		15	
t_{PZH}/t_{PZL}	3-State output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	Figures 2	1.2		70				ns
			2.0		24	32		41	
			2.7		18	24		30	
			3.0 to 3.6		13[2]	19		24	
			4.5 to 5.5			16		20	
t_{PHZ}/t_{PLZ}	3-State output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	Figures 2	1.2		65				ns
			2.0		24	29		36	
			2.7		18	22		27	
			3.0 to 3.6		14[2]	18		22	
			4.5 to 5.5			15		18	

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$V at $V_{CC} \geq 2.7$V and ≤ 3.6V;
$V_M = 0.5V \times V_{CC}$ at $V_{CC} < 2.7$V and ≥ 4.5V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$V at $V_{CC} \geq 2.7$V and ≤ 3.6V
$V_X = V_{OL} + 0.1V \times V_{CC}$ at $V_{CC} < 2.7$V and 4.5V
$V_Y = V_{OH} - 0.3$V at $V_{CC} \geq 2.7$V and ≤ 3.6V
$V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7$V and ≥ 4.5V

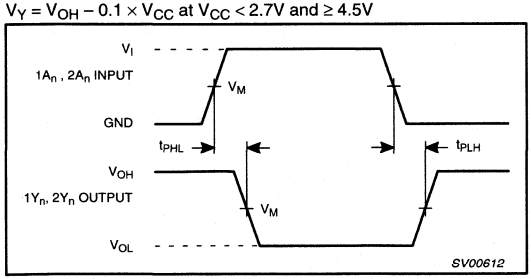


Figure 1. Input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

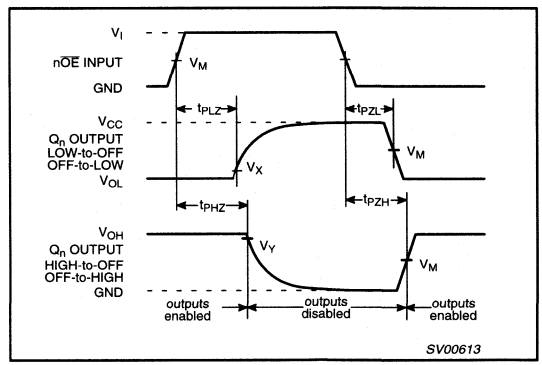
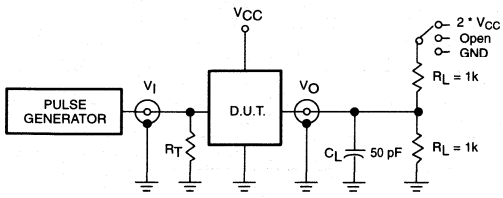


Figure 2. 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitiance.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5V	V_{CC}

SV00896

Figure 3. Load circuitry for switching times.

Octal buffer/line driver (3-State) 74LV241

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV241 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT241.

The 74LV241 is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 3.3 V	8.0	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	30	pF

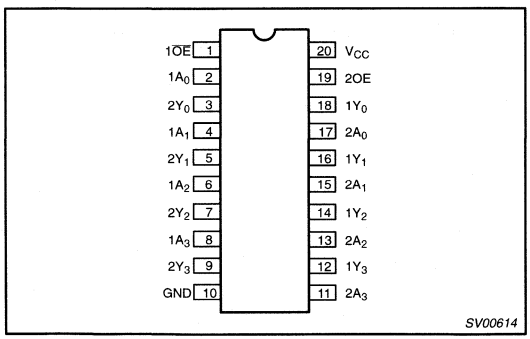
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

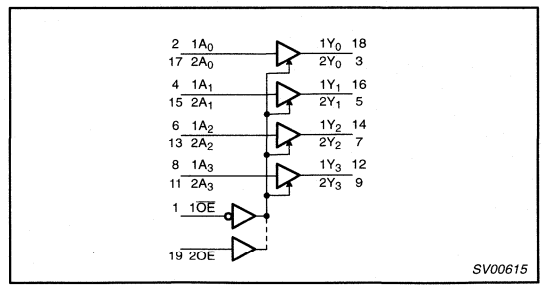
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV241 N	74LV241 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV241 D	74LV241 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV241 DB	74LV241 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV241 PW	74LV241PW DH	SOT360-1

PIN CONFIGURATION



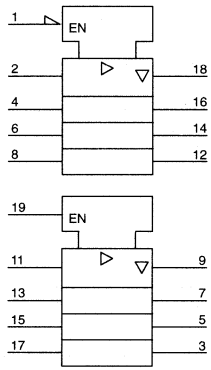
LOGIC SYMBOL



PIN DESCRIPTION

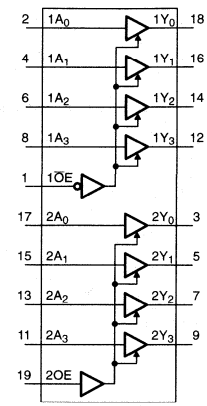
PIN NUMBER	SYMBOL	FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	Data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	Bus outputs
10	GND	Ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	Data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	Bus outputs
19	2OE	Output enable input (active HIGH)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



SV00609

FUNCTIONAL DIAGRAM



SV00616

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	2OE	$2A_n$	$1Y_n$	$2Y_n$
L	L	H	L	H	L
L	H	H	H	L	H
H	X	L	X	Z	Z

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC} - 0.6V$			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	Figures 1	1.2		45				ns
			2.0		15	31		36	
			2.7		11	23		26	
			3.0 to 3.6		9[2]	18		21	
t_{PZH}/t_{PZL}	3-State output enable time $1\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$	Figures 2, 3	1.2		55				ns
			2.0		19	36		44	
			2.7		14	26		33	
			3.0 to 3.6		10[2]	21		26	
t_{PHZ}/t_{PLZ}	3-State output disable time $1\overline{OE}$ to $1Y_n$; 2OE to $2Y_n$	Figures 2, 3	1.2		60				ns
			2.0		22	39		48	
			2.7		17	29		36	
			3.0 to 3.6		13[2]	24		29	

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$.
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V; $V_M = 0.5$ V × V_{CC} at $V_{CC} < 2.7$ V
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V; $V_X = V_{OL} + 0.1$ V × V_{CC} at $V_{CC} < 2.7$ V
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$V; $V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

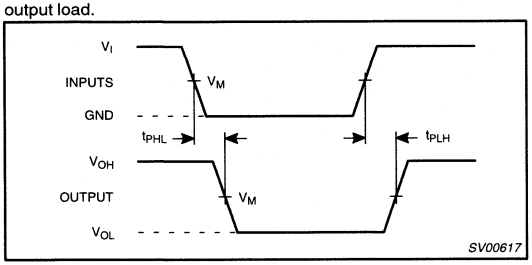


Figure 1. Input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

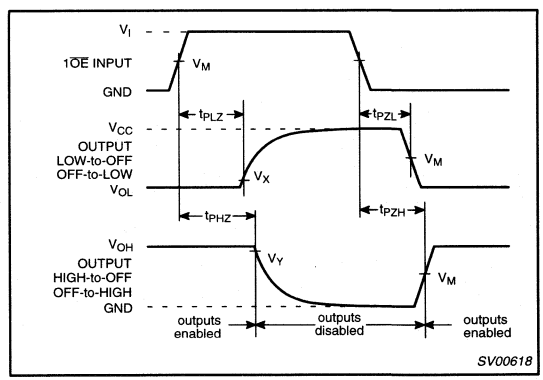


Figure 2. 3-State enable and disable times.

AC WAVEFORMS (Continued)

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V; V_M = 0.5 V × V_{CC} at V_{CC} < 2.7 V
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V; $V_X = V_{OL}$ + 0.1 V × V_{CC} at V_{CC} < 2.7 V
$V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ − 0.1 × V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

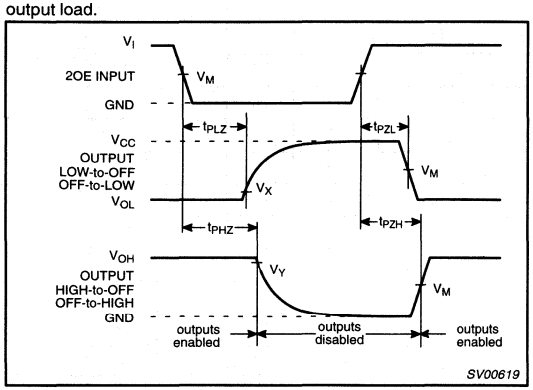


Figure 3. 3-State enable and disable times for input 2OE.

TEST CIRCUIT

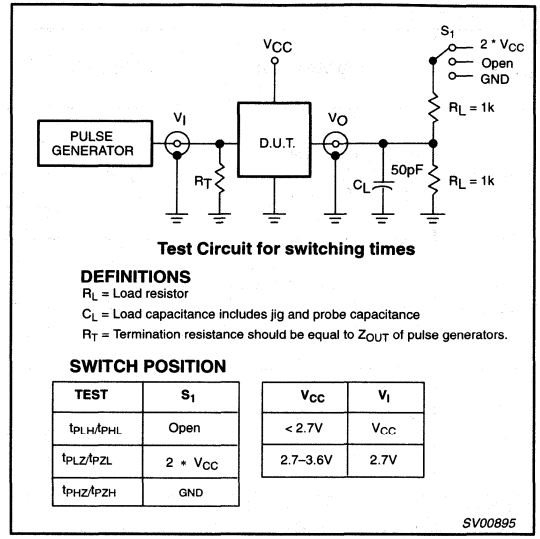


Figure 4. Load circuitry for switching times.

Octal buffer/line driver (3-State) 74LV244

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV244 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT244.

The 74LV244 is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The 74LV244 is identical to the 74LV240 but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 3.3 V	8.0	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3 V; V_I = GND to V_{CC}[1]	35	pF

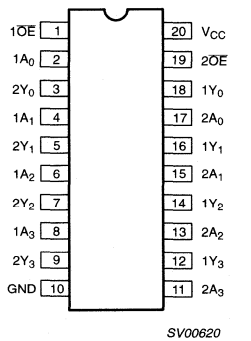
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

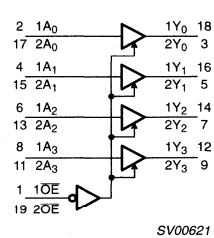
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV244 N	74LV244 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV244 D	74LV244 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV244 DB	74LV244 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV244 PW	74LV244PW DH	SOT360-1

PIN CONFIGURATION



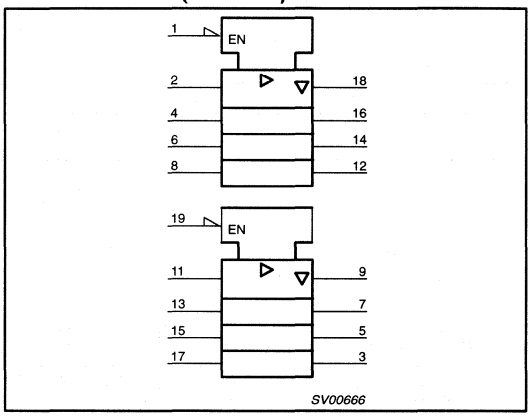
LOGIC SYMBOL



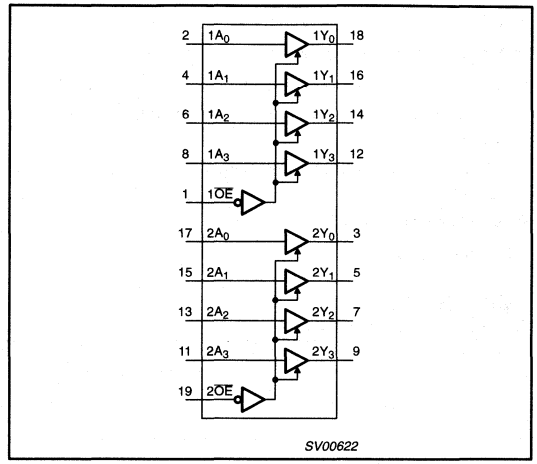
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	Data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	Bus outputs
10	GND	Ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	Data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	Bus outputs
19	$2\overline{OE}$	Output enable input (active LOW)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 8mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	Figures 1, 2	1.2		50				ns
			2.0		17	24		31	
			2.7		13	17		23	
			3.0 to 3.6		9[2]	14		18	
			4.5 to 5.5			12		15	
t_{PZH}/t_{PZL}	3-State output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	Figures 2, 3	1.2		65				ns
			2.0		22	39		49	
			2.7		16	29		36	
			3.0 to 3.6		12[2]	23		29	
			4.5 to 5.5			19		24	
t_{PHZ}/t_{PLZ}	3-State output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	Figures 2, 3	1.2		60				ns
			2.0		22	34		43	
			2.7		17	24		32	
			3.0 to 3.6		13[2]	21		26	
			4.5 to 5.5			16		19	

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$.
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V and ≤ 3.6 V
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V and ≥ 4.5 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V and ≤ 3.6 V
$V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V and ≥ 4.5 V
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$V and ≤ 3.6 V
$V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V and ≥ 4.5 V

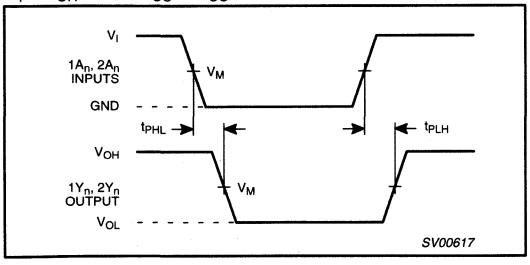


Figure 1. Input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

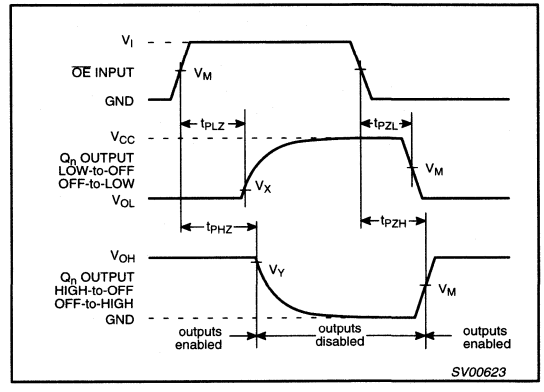
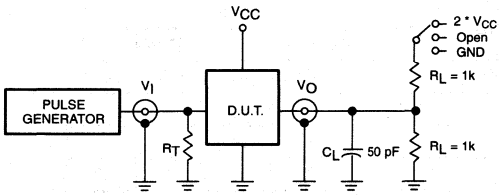


Figure 2. 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitiance.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5V	V_{CC}

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Figure 3. Load circuitry for switching times.

Octal bus transceiver (3-State) 74LV245

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV245 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT245.

The 74LV245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74LV245 features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n; B_n to A_n	C_L = 15 pF; V_{CC} = 3.3 V	7.0	ns
C_I	Input capacitance		3.5	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3 V; V_I = GND to V_{CC}, note 1	40	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV245 N	74LV245 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV245 D	74LV245 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV245 DB	74LV245 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV245 PW	74LV245PW DH	SOT360-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	DIR	Direction
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	Data inputs/outputs
10	GND	Ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	Data inputs/outputs
19	$\overline{OE}$	Output enable input (active LOW)
20	V_{CC}	Positive supply voltage

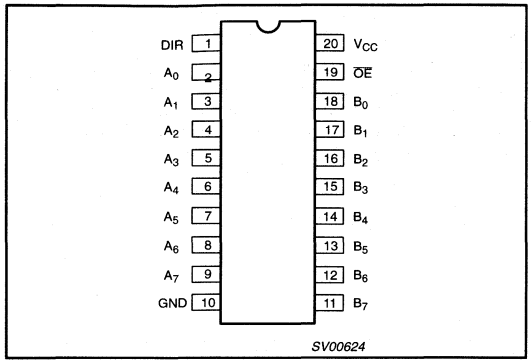
FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

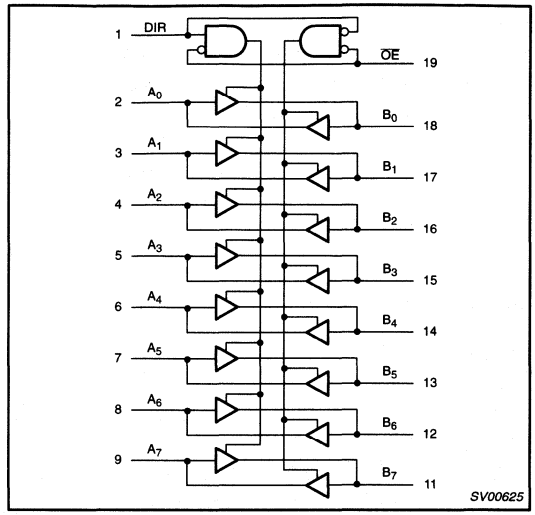
NOTES:

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

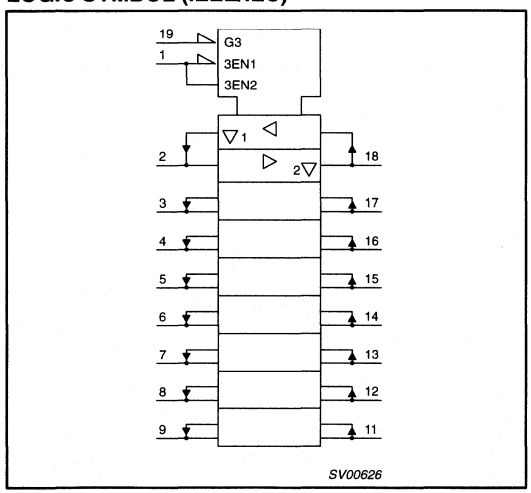
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics –40 –40			+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n; B_n to A_n	Figures 1	1.2		45	28			ns
			2.0		15	28		34	
			2.7		11	19		24	
			3.0 to 3.6		9[2]	16		20	
			4.5 to 5.5		8[3]	11		14	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n	Figures 2	1.2		55				ns
			2.0		19	31		39	
			2.7		14	23		29	
			3.0 to 3.6		10[2]	18		23	
			4.5 to 5.5		8.5[3]	14		18	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n	Figures 2	1.2		65				ns
			2.0		24	32		39	
			2.7		18	24		29	
			3.0 to 3.6		14[2]	20		24	
			4.5 to 5.5		11.5[3]	16		19	

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.
3. Typical values are measured at $V_{CC} = 5.0$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V and ≤ 3.6 V
$V_M = 0.5$ V × V_{CC} at $V_{CC} < 2.7$ V and ≥ 4.5 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V and ≤ 3.6 V
$V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V and ≥ 4.5 V
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$V and ≤ 3.6 V
$V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V and ≥ 4.5 V

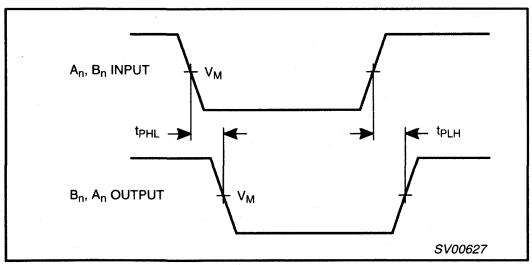


Figure 1. Input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

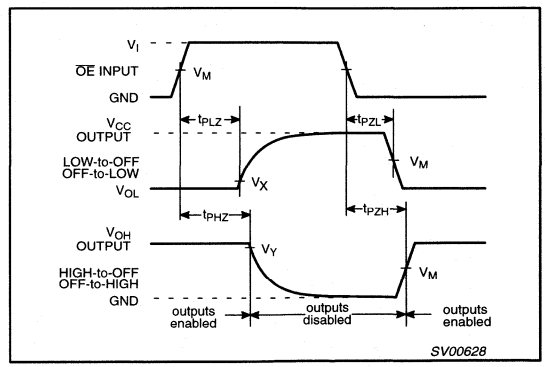
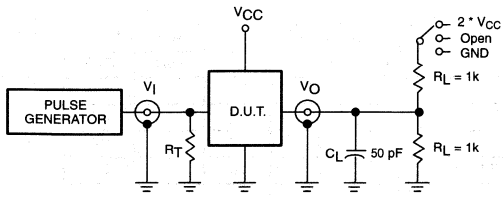


Figure 2. 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitiance.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5V	V_{CC}

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Figure 3. Load circuitry for switching times.

8-input multiplexer (3-State) 74LV251

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- True and complement outputs
- Both outputs are 3-State for further multiplexer expansion
- Multifunction capability
- Permits multiplexing from n-lines to one line
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV251 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT251.

The 74LV251 is an 8-input multiplexer with 8 binary inputs (I_0 to I_7), an output enable input ($\overline{OE}$) and three select inputs (S_0, S_1, S_2). One of the eight binary inputs is selected by the select inputs and is routed to the outputs ($\overline{Y}$, Y). Both outputs are in the high impedance OFF-state (Z) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay I_n to Y I_n to $\overline{Y}$ S_n to Y S_n to $\overline{Y}$	C_L = 15 pF; V_{CC} = 3.3 V	 14 16 19 20	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	44	pF

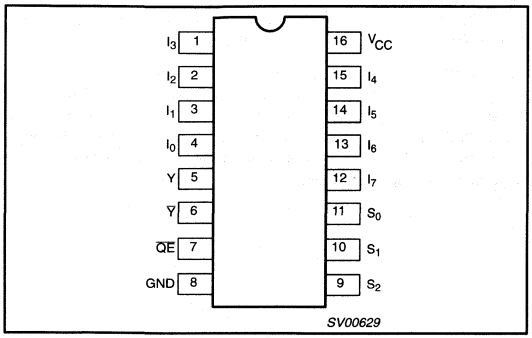
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV251 N	74LV251 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV251 D	74LV251 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV251 DB	74LV251 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV251 PW	74LV251PW DH	SOT403-1

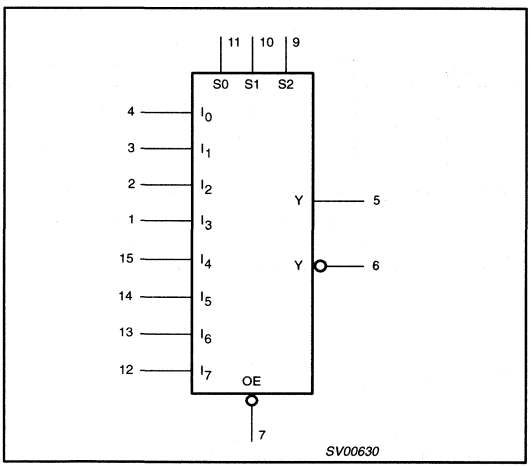
PIN CONFIGURATION



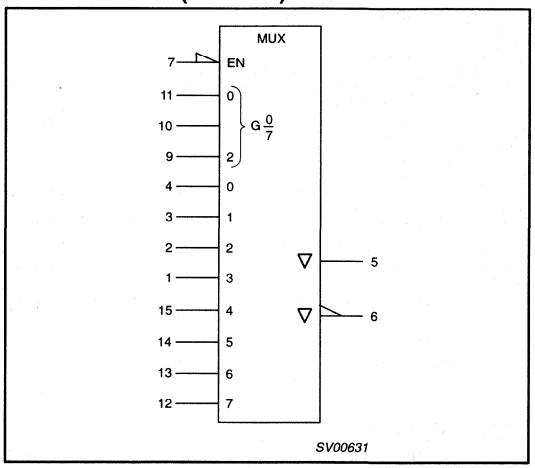
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	Multiplexer inputs
5	Y	Multiplexer output
6	$\overline{Y}$	Complementary multiplexer output
7	$\overline{OE}$	3-State output enable input (active LOW)
8	GND	Ground (0 V)
11, 10, 9	S_0 to S_2	Select inputs
16	V_{CC}	Positive supply voltage

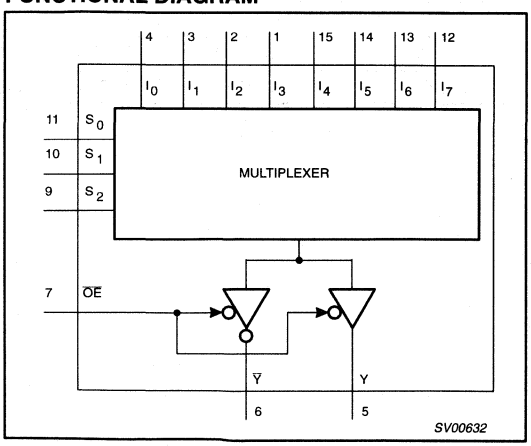
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f = 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay I_n to Y	Figure 1	1.2		90				ns
			2.0		31	58		70	
			2.7		23	43		51	
			3.0 to 3.6		17[2]	34		41	
t_{PHL}/t_{PLH}	Propagation delay I_n to $\overline{Y}$	Figure 2	1.2		100				ns
			2.0		34	65		77	
			2.7		25	48		56	
			3.0 to 3.6		19[2]	38		45	
t_{PHL}/t_{PLH}	Propagation delay S_n to Y	Figure 1	1.2		120				ns
			2.0		41	77		92	
			2.7		30	56		68	
			3.0 to 3.6		23[2]	45		54	
t_{PHL}/t_{PLH}	Propagation delay S_n to $\overline{Y}$	Figure 2	1.2		125				ns
			2.0		43	82		97	
			2.7		31	60		71	
			3.0 to 3.6		24[2]	48		57	
t_{PZH}/t_{PZL}	3-State output disable time $\overline{OE}$ to Y, $\overline{Y}$	Figure 2	1.2		65				ns
			2.0		22	43		51	
			2.7		16	31		38	
			3.0 to 3.6		12[2]	25		30	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Y, $\overline{Y}$	Figure 2	1.2		60				ns
			2.0		22	39		48	
			2.7		17	29		36	
			3.0 to 3.6		13[2]	24		29	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 V × V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 × V_{CC} at V_{CC} < 2.7 V
$V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH}$ – 0.1 × V_{CC} at V_{CC} < 2.7 V

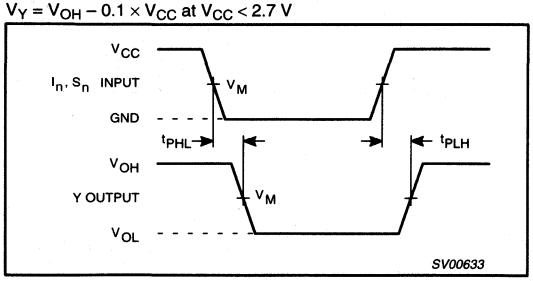


Figure 1. Multiplexer input (I_n) and select input (S_n) to output (Y) propagation delays.

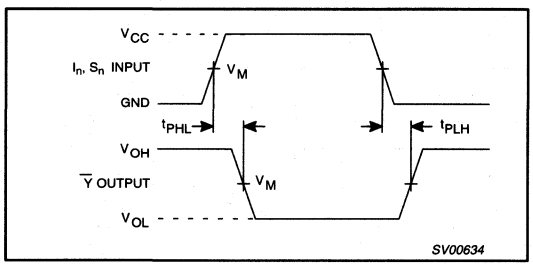


Figure 2. Multiplexer input (I_n) and the select input (S_n) to output ($\overline{Y}$) propagation delays.

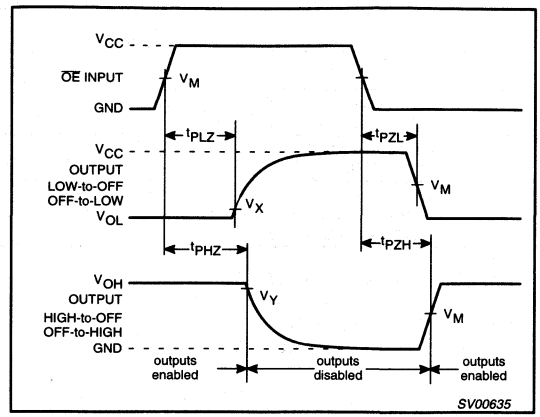


Figure 3. 3-State enable and disable times

TEST CIRCUIT

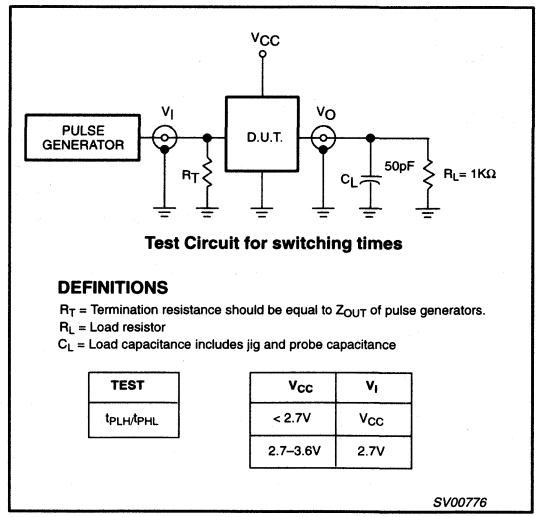


Figure 4. Load circuitry for switching times.

Quad 2-input multiplexer (3-State) 74LV257

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Non-inverting data path
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV257 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT257.

The 74LV257 is a quad 2-input multiplexer with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S). The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S in HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) from the selected inputs. The 74LV257 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S. The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$1Y = \overline{OE} \times (1I_1 \times S + 1I_0 \times \overline{S})$
$2Y = \overline{OE} \times (2I_1 \times S + 2I_0 \times \overline{S})$
$3Y = \overline{OE} \times (3I_1 \times S + 3I_0 \times \overline{S})$
$4Y = \overline{OE} \times (4I_1 \times S + 4I_0 \times \overline{S})$

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nI_0, nI_1 to nY S to nY	C_L = 15 pF; V_{CC} = 3.3 V	 10 14	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	30	pF

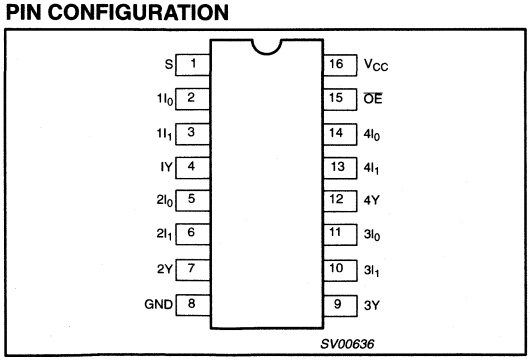
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV257 N	74LV257 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV257 D	74LV257 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV257 DB	74LV257 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV257 PW	74LV257PW DH	SOT403-1

PIN CONFIGURATION

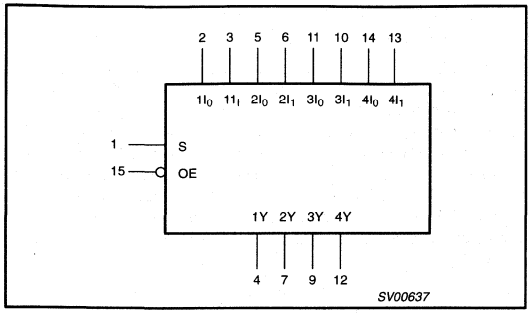


PIN DESCRIPTION

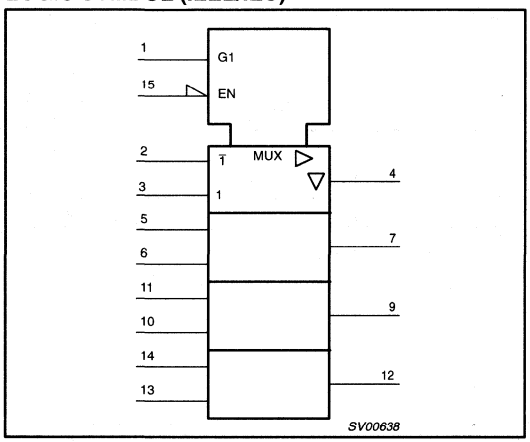
PIN NUMBER	SYMBOL	FUNCTION
1	S	Common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	Data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	Data inputs from source 1
4, 7, 9, 12	1Y to 4Y	3-state multiplexer outputs
8	GND	Ground (0 V)
15	$\overline{OE}$	3-State output enable input (active LOW)
16	V_{CC}	Positive supply voltage

Quad 2-input multiplexer (3-State) 74LV257

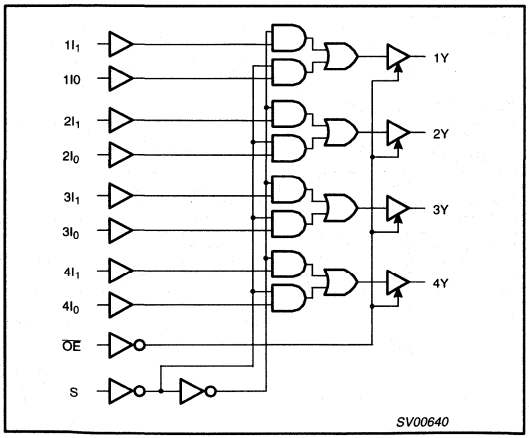
LOGIC SYMBOL



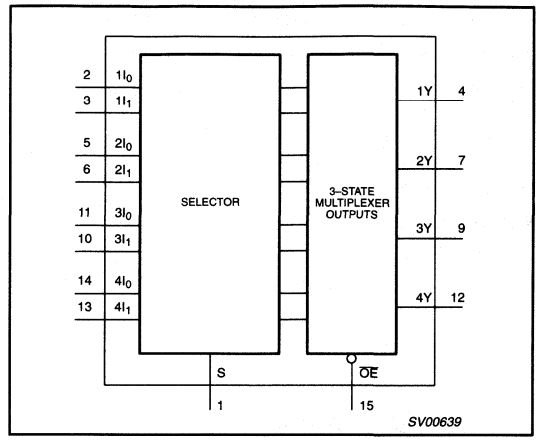
LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}$	S	nI_0	nI_1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} =3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA		1.2				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100μA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0				V
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 100μA		0	0.2		0.2	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0 V; V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND			1.0		1.0	μA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	μA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	μA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nI_0 to nY nI_1 to nY	Figure 1	1.2		65				ns
			2.0		22	43		51	
			2.7		16	31		38	
			3.0 to 3.6		12[2]	25		30	
t_{PHL}/t_{PLH}	Propagation delay S to nY	Figure 1	1.2		85				ns
			2.0		29	56		66	
			2.7		21	41		49	
			3.0 to 3.6		16[2]	33		39	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to nY	Figure 2	1.2		60				ns
			2.0		20	39		46	
			2.7		15	29		34	
			3.0 to 3.6		11[2]	23		27	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to nY	Figure 2	1.2		65				ns
			2.0		24	40		49	
			2.7		18	32		37	
			3.0 to 3.6		14[2]	26		30	

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$V
$V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

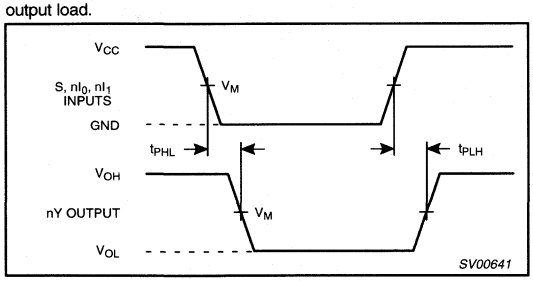


Figure 1. Input (S, nI_0, nI_1) to output (nY) propagation delays.

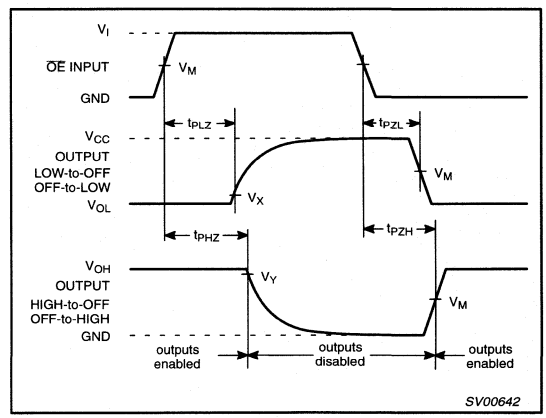
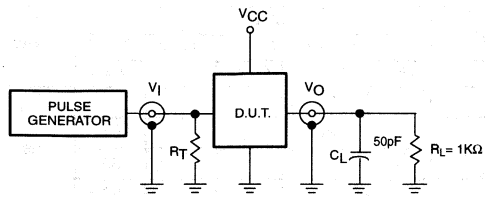


Figure 2. 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance

TEST
t_{PLH}/t_{PHL}

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00776

Figure 3. Load circuitry for switching times.

8-bit addressable latch 74LV259

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV259 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT259.

The 74LV259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. The 74LV259 is a multifunction device capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q_0 to Q_7), functions are available. The 74LV259 also incorporate an active LOW common reset ($\overline{MR}$) for resetting all latches, as well as an active LOW enable input ($\overline{LE}$). The 74LV259 has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A_0 to A_2) and date (D) input. When operating the 74LV259 as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the 74LV259.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D, A_n to Q_n $\overline{LE}$ to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF; V_{CC} = 3.3 V	 17 16 14	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	19	pF

NOTE:

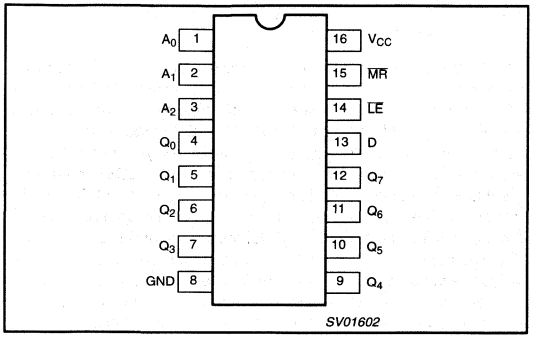
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV259 N	74LV259 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV259 D	74LV259 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV259 DB	74LV259 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV259 PW	74LV259PW DH	SOT403-1

8-bit addressable latch 74LV259

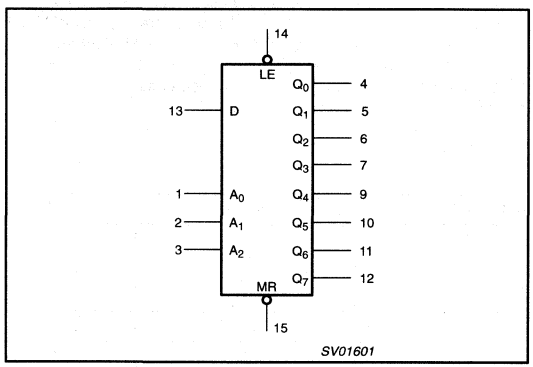
PIN CONFIGURATION



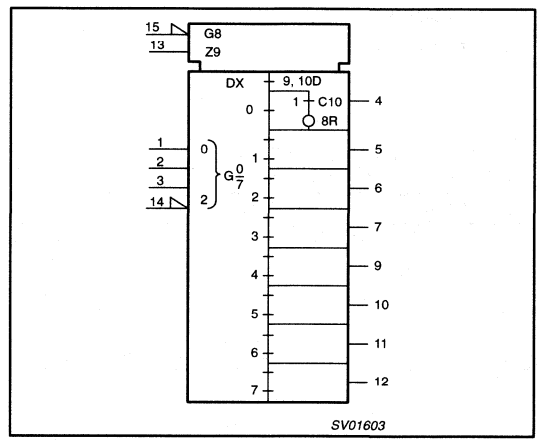
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3	A_0 to A_2	Address inputs
4, 5, 6, 7, 9, 10, 11, 12	Q_0 to Q_7	Latch outputs
8	GND	Ground (0 V)
13	D	Data input
14	$\overline{LE}$	Latch enable input (active LOW)
15	$\overline{MR}$	Conditional reset input (active LOW)
16	V_{CC}	Positive supply voltage

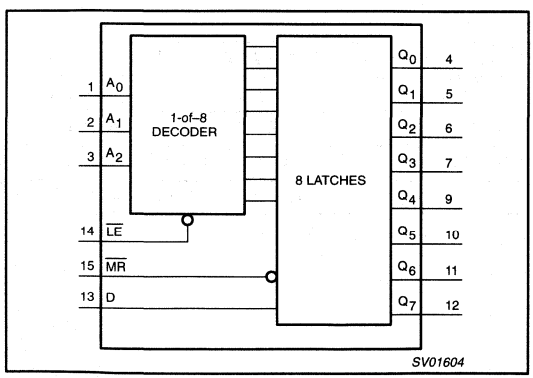
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



MODE SELECT TABLE

$\overline{LE}$	$\overline{MR}$	MODE
L	H	Addressable latch
H	H	Memory
L	L	Active HIGH 8-channel demultiplexer
H	L	Reset

FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS							
	$\overline{MR}$	$\overline{LE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Store (do nothing)	H	H	X	X	X	X	q0	q1	q2	q3	q4	q5	q6	q7
Addressable latch	H	L	d	L	L	L	Q=d	q1	q2	q3	q4	q5	q6	q7
	H	L	d	H	L	L	q0	Q=d	q2	q3	q4	q5	q6	q7
	H	L	d	L	H	L	q0	q1	Q=d	q3	q4	q5	q6	q7
	H	L	d	H	H	L	q0	q1	q2	Q=d	q4	q5	q6	q7
	H	L	d	L	L	H	q0	q1	q2	q3	Q=d	q5	q6	q7
	H	L	d	H	L	H	q0	q1	q2	q3	q4	Q=d	q6	q7
	H	L	d	L	H	H	q0	q1	q2	q3	q4	q5	Q=q	q7
	H	L	d	H	H	H	q0	q1	q2	q3	q4	q5	q6	Q=d

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{LE}$ transition
q = lower case letters indicate the state of the referenced output established during the last cycle established during the last cycle in which it was addressed or cleared

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} − 0.6 V			500		850	μA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay D to Q_n	Figure 2	1.2		105				ns
			2.0		36	49		61	
			2.7		26	36		45	
			3.0 to 3.6		20[2]	29		36	
t_{PHL}/t_{PLH}	Propagation delay A_n to Q_n	Figure 3	1.2		105				ns
			2.0		36	49		61	
			2.7		26	36		45	
			3.0 to 3.6		20[2]	29		36	
t_{PHL}/t_{PLH}	Propagation delay $\overline{LE}$ to Q_n	Figure 1	1.2		100				ns
			2.0		34	48		60	
			2.7		25	35		44	
			3.0 to 3.6		19[2]	28		35	
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Figure 4	1.2		90				ns
			2.0		31	43		53	
			2.7		23	31		39	
			3.0 to 3.6		17[2]	25		31	
t_w	$\overline{LE}$ pulse width HIGH or LOW	Figure 1	2.0	34	10		41		ns
			2.7	25	8		30		
			3.0 to 3.6	20	6[2]		24		
t_w	$\overline{MR}$ pulse width LOW	Figure 4	2.0	34	10		41		ns
			2.7	25	8		30		
			3.0 to 3.6	20	6[2]		24		
t_{su}	Set-up time D, A_n to $\overline{LE}$	Figure 5 and 6	1.2		35				ns
			2.0	24	12		29		
			2.7	18	9		21		
			3.0 to 3.6	14	7[2]		17		
t_h	Hold time D to $\overline{LE}$	Figure 5	1.2		−30				ns
			2.0	5	−10		5		
			2.7	5	−8		5		
			3.0 to 3.6	5	−6[2]		5		

AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	–40 to +85 °C			–40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_h	Hold time A_n to $\overline{LE}$	Figure 6	1.2		–20				ns
			2.0	5	–7		5		
			2.7	5	–5		5		
			3.0 to 3.6	5	–4[2]		5		

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V and ≤ 3.6V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V and ≥ 4.5 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

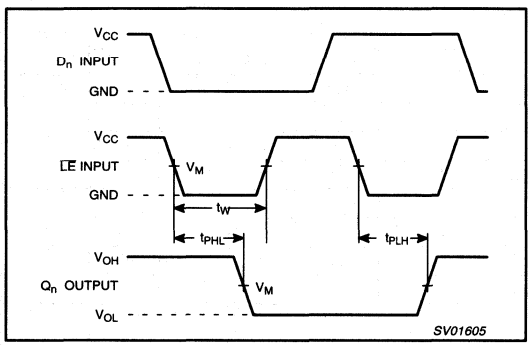


Figure 1. Enable input ($\overline{LE}$) to output (Q_n) propagation delays and the enable input pulse width.

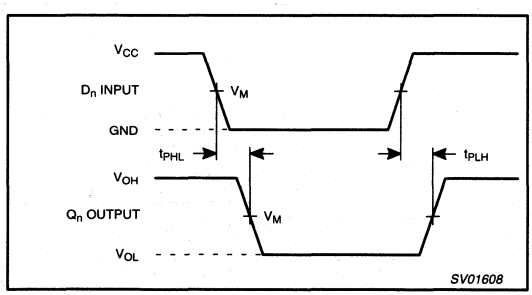


Figure 2. Data input (D) to output (Q_n) propagation delays.

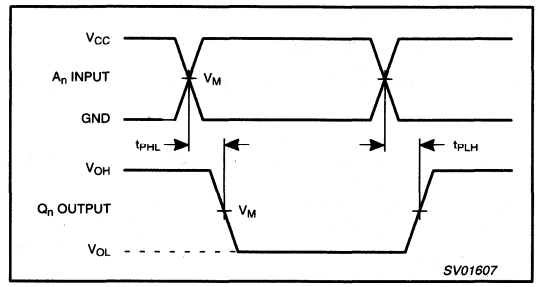


Figure 3. Address inputs (A_n) to output (Q_n) propagation delays.

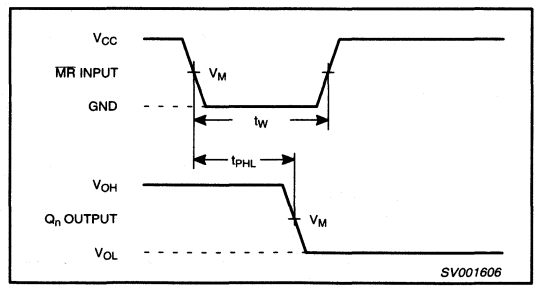


Figure 4. Conditional reset input ($\overline{MR}$) to output (Q_n) propagation delays.

AC WAVEFORMS (Continued)

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V and $\geq$ 4.5 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

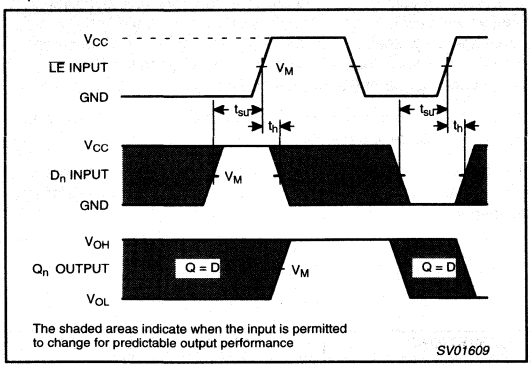


Figure 5. Data set-up and hold times for D input to $\overline{LE}$ input.

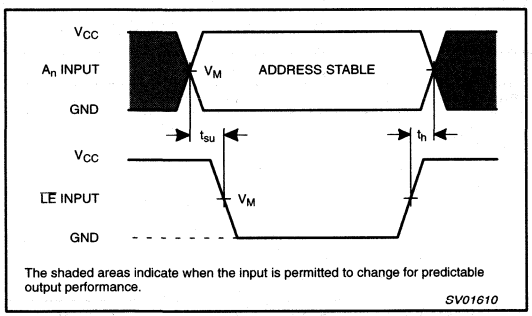


Figure 6. Address set-up and hold times for A_n inputs to $\overline{LE}$ input.

TEST CIRCUIT

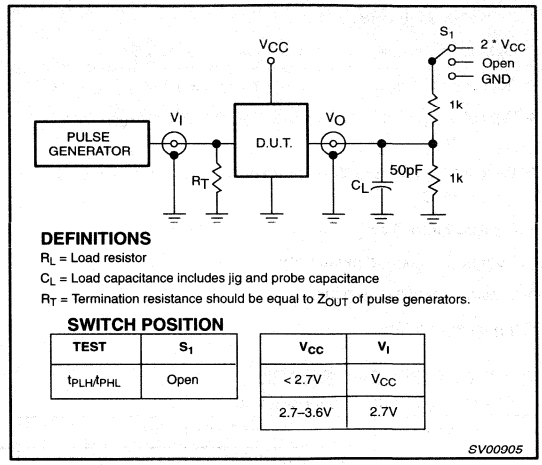


Figure 7. Load circuitry for switching times.

Octal D-type flip-flop with reset; positive edge-trigger 74LV273

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV273 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT273.

The 74LV273 has eight edge-triggered , D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n; $\overline{MR}$ to Q_n	C_L = 15pF V_{CC} = 3.3V	12 13	ns
f_{max}	Maximum clock frequency		110	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	20	pF

NOTES:

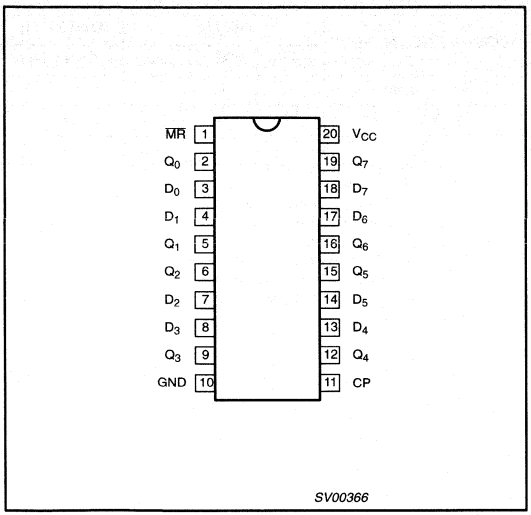
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

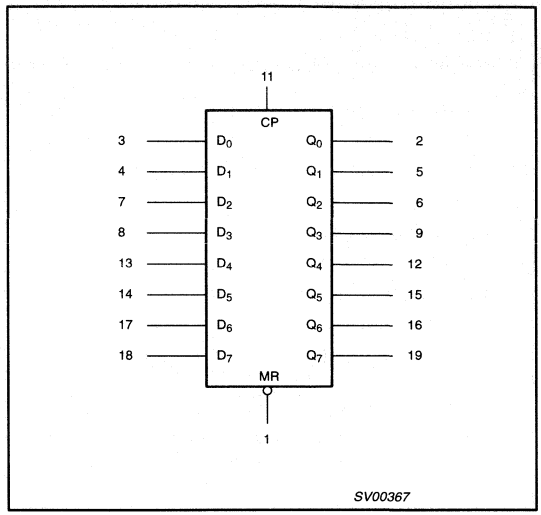
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV273 N	74LV273 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV273 D	74LV273 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV273 DB	74LV273 DB	SOT339-1
20-Pin Plastic TSSOP	–40°C to +125°C	74LV273 PW	74LV273PW DH	SOT360-1

Octal D-type flip-flop with reset; positive edge-trigger 74LV273

PIN CONFIGURATION



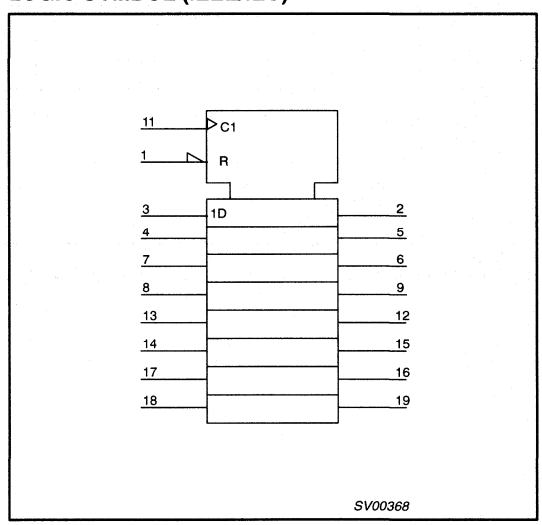
LOGIC SYMBOL



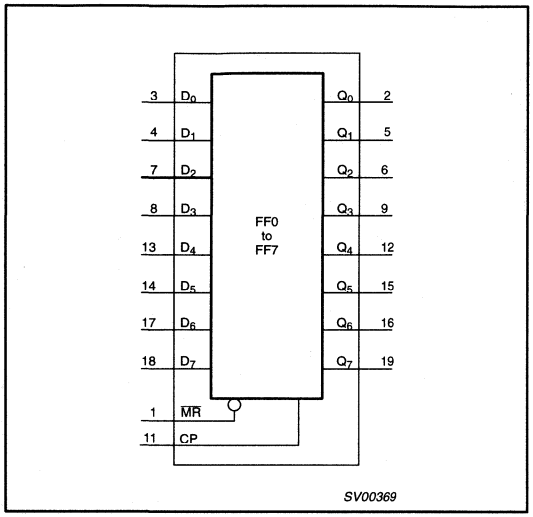
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	Master reset input (active-LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	Flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_0 to Q_7
Reset (clear)	L	X	X	L
Load ('1')	H	↑	h	H
Load ('0')	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW–to–HIGH clock transition
X = Don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTES:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	$0.7*V_{CC}$			$0.7*V_{CC}$		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			$0.3*V_{CC}$		$0.3*V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	

DC CHARACTERISTICS FOR THE LV FAMILY (Continued)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_r = t_f = 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	Figure 1	1.2	–	75	–	–	–	ns
			2.0	–	26	32	–	41	
			2.7	–	19	24	–	30	
			3.0 to 3.6	–	14[2]	19	–	24	
			4.5 to 5.5	–	–	16	–	20	
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Figure 2	1.2	–	80	–	–	–	ns
			2.0	–	27	44	–	56	
			2.7	–	20	33	–	41	
			3.0 to 3.6	–	15[2]	26	–	33	
			4.5 to 5.5	–	–	22	–	28	
t_W	Clock pulse width HIGH or LOW	Figure 1	2.0	34	9	–	41	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5[2]	–	24	–	
t_W	Master reset pulse width LOW	Figure 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6[2]	–	24	–	
t_{rem}	Removal time $\overline{MR}$ to CP	Figure 2	1.2	–	–10	–	–	–	ns
			2.0	5	–4	–	5	–	
			2.7	5	–3	–	5	–	
			3.0 to 3.6	5	–2[2]	–	5	–	
t_{su}	Set-up time D_n to CP	Figure 3	1.2	–	20	–	–	–	ns
			2.0	22	7	–	26	–	
			2.7	16	5	–	19	–	
			3.0 to 3.6	13	4[2]	–	15	–	
t_h	Hold time D_n to CP	Figure 3	1.2	–	–10	–	–	–	ns
			2.0	5	–4	–	5	–	
			2.7	5	–3	–	5	–	
			3.0 to 3.6	5	–2[2]	–	5	–	
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40	–	12	–	MHz
			2.7	19	75	–	16	–	
			3.0 to 3.6	24	100[2]	–	20	–	

NOTE:

1. Unless otherwise stated, all typical values are at T_{amb} = 25°C.
2. Typical value measured at V_{CC} = 3.3V.
3. Typical value measured at V_{CC} = 5.0V.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V ≤ 3.6V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

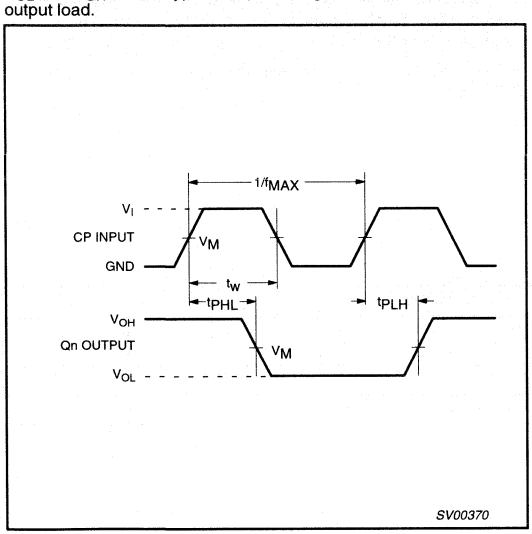


Figure 1. The clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency

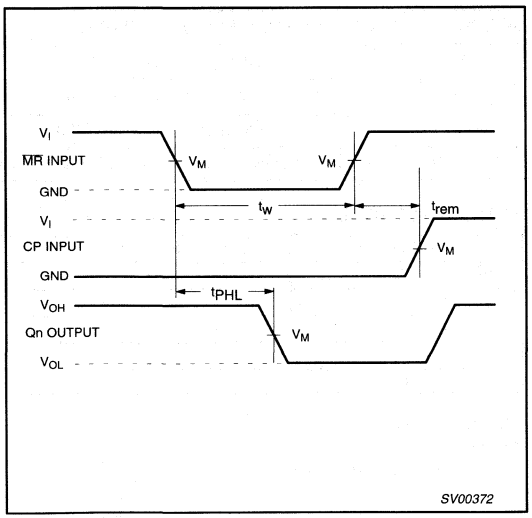


Figure 2. The master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagations delay and the master reset to clock (CP) removal time

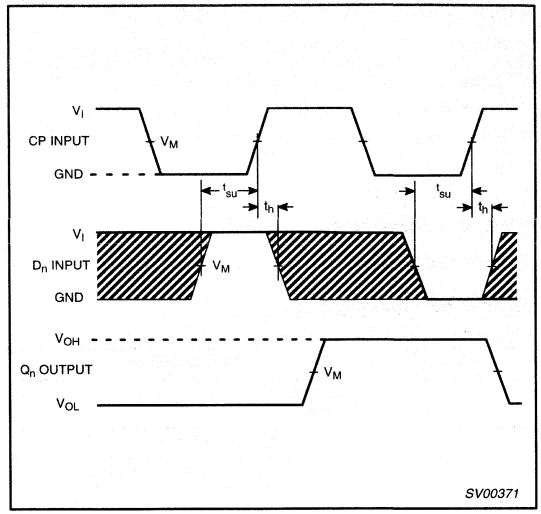


Figure 3. Data set-up and hold times for the data input (D_n)

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT

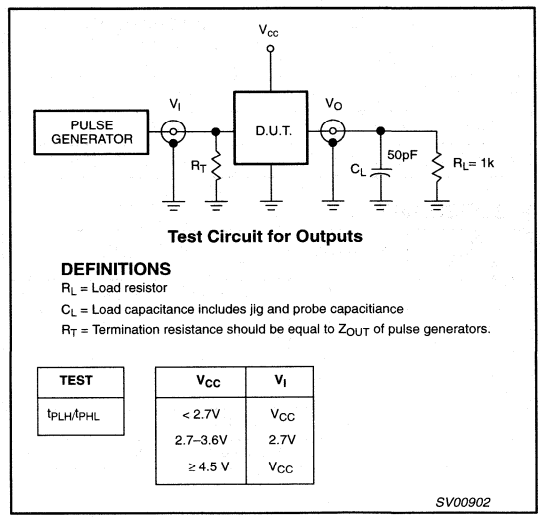


Figure 4. Load circuitry for switching times

Hex buffer/line driver (3-State) 74LV365

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV365 is a low-voltage CMOS device and is pin and function compatible 74HC/HCT365.

The 74LV365 is a hex non-inverting buffer/line driver with 3-State outputs. The 3-State outputs (nY) are controlled by the output enable inputs ($\overline{OE}1$, $\overline{OE}2$).

A HIGH on $\overline{OE}$n, causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 15pF V_{CC} = 3.3V	9	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1 and 2	40	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV365 N	74LV365 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV365 D	74LV365 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV365 DB	74LV365 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV365 PW	74LV365PW DH	SOT403-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	$\overline{OE}1$, $\overline{OE}2$	Output enable inputs (active-LOW)
2, 4, 6, 10, 12, 14	1A to 6A	Data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	Data outputs
8	GND	Ground (0V)
16	V_{CC}	Positive supply voltage

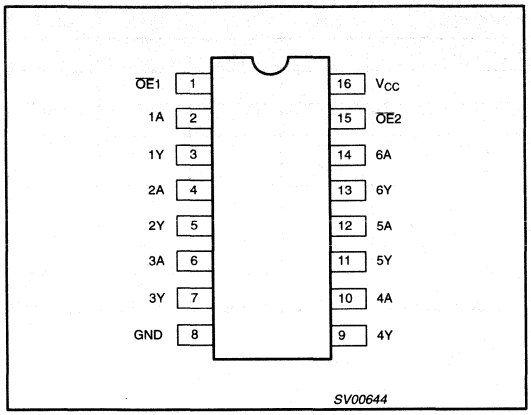
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}1$	$\overline{OE}2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

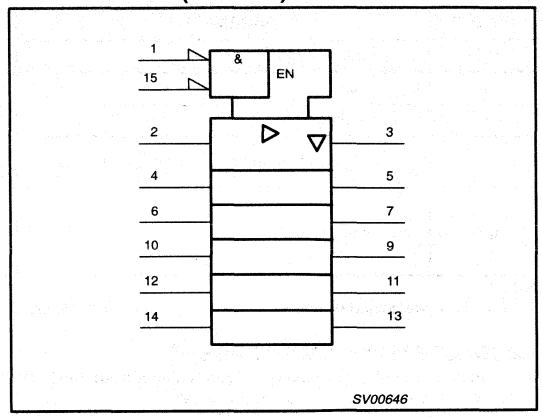
H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

Hex buffer/line driver (3-State) 74LV365

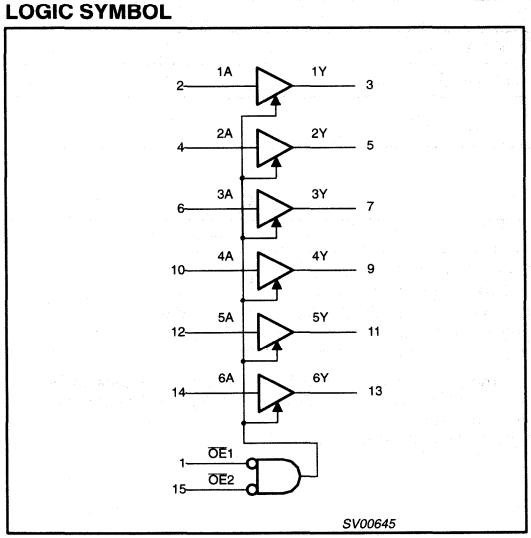
PIN CONFIGURATION



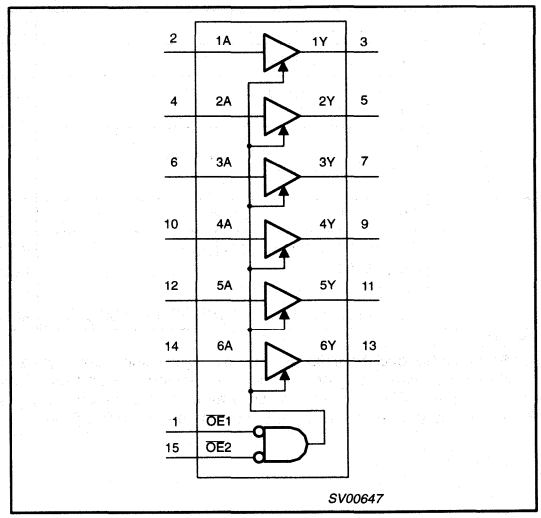
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC} - 0.6V$			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA to nY	Figure 1	1.2	–	55	–	–	–	ns
			2.0	–	19	36	–	44	
			2.7	–	14	26	–	33	
			3.0 to 3.6	–	10[2]	21	–	26	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$n to nY	Figure 2	1.2	–	85	–	–	–	ns
			2.0	–	29	56	–	66	
			2.7	–	21	41	–	49	
			3.0 to 3.6	–	16[2]	33	–	39	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$n to nY	Figure 2	1.2	–	100	–	–	–	ns
			2.0	–	36	66	–	78	
			2.7	–	27	48	–	58	
			3.0 to 3.6	–	21[2]	39	–	47	

NOTES:
1. All typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3V$

AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$
$V_M = 0.5V * V_{CC}$ at $V_{CC} < 2.7V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$
$V_X = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7V$
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$
$V_Y = V_{OH} - 0.1V_{CC}$ at $V_{CC} < 2.7V$

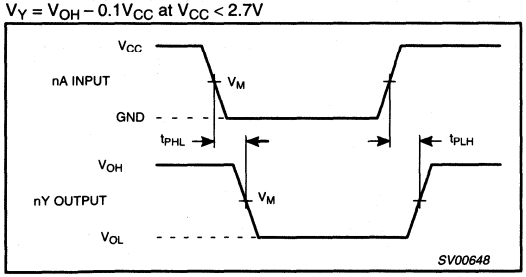


Figure 1. Input (nA) to output (nY) propagation delays.

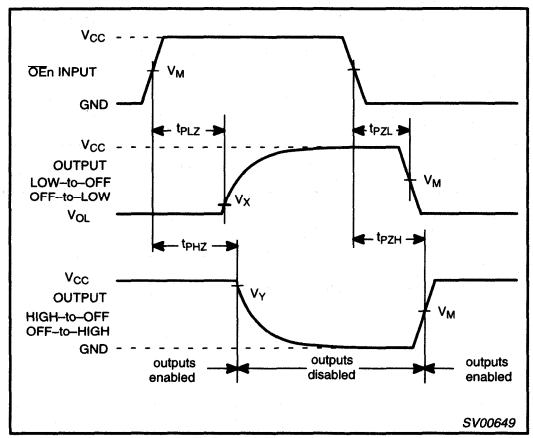
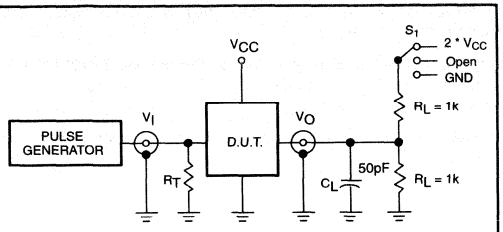


Figure 2. 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00895

Figure 3. Load circuitry for switching times

Hex buffer/line driver (3-State) 74LV367

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV367 is a low-voltage CMOS device and is pin and function compatible 74HC/HCT367.

The 74LV367 is a hex non-inverting buffer/line driver with 3-State outputs. The 3-State outputs (nY) are controlled by the output enable inputs ($1\overline{OE}$, $2\overline{OE}$).

A HIGH on $n\overline{OE}$, causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 15pF V_{CC} = 3.3V	8	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1 and 2	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV367 N	74LV367 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV367 D	74LV367 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV367 DB	74LV367 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV367 PW	74LV367PW DH	SOT403-1

PIN DESCRIPTION

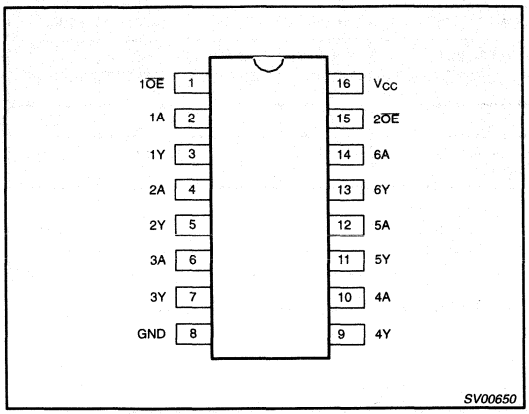
PIN NUMBER	SYMBOL	FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-LOW)
2, 4, 6, 10, 12, 14	1A to 6A	Data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	Data outputs
8	GND	Ground (0V)
16	V_{CC}	Positive supply voltage

FUNCTION TABLE

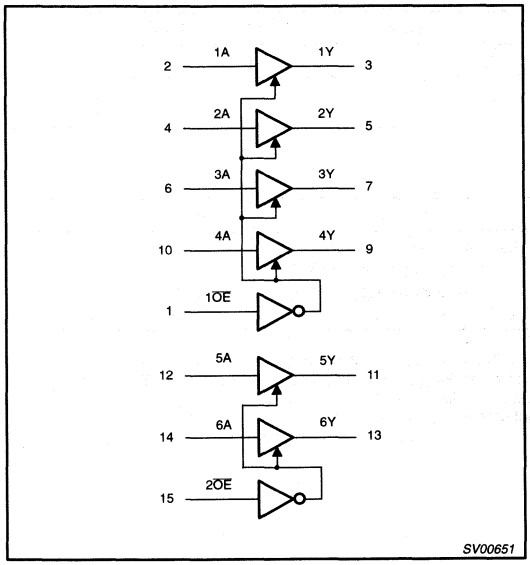
INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

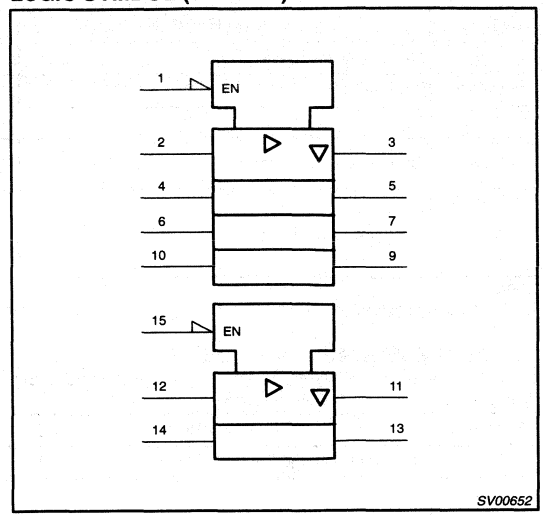
PIN CONFIGURATION



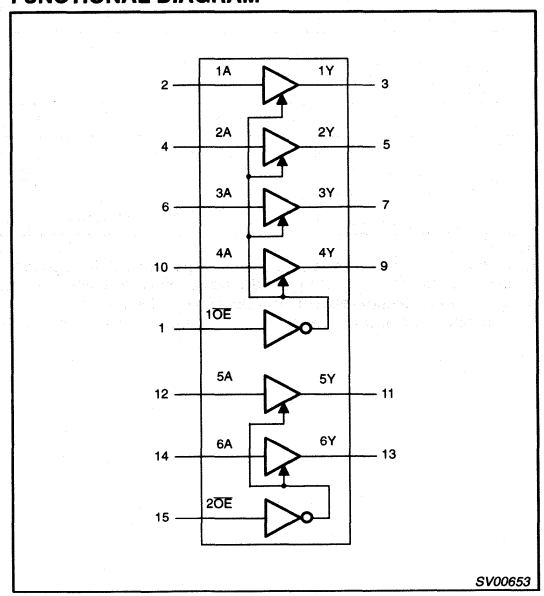
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC} - 0.6V$			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA to nY	Figure 1	1.2	–	50	–	–	–	ns
			2.0	–	17	32	–	39	
			2.7	–	13	24	–	29	
			3.0 to 3.6	–	10[2]	19	–	23	
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nY	Figure 2	1.2	–	80	–	–	–	ns
			2.0	–	27	51	–	60	
			2.7	–	20	38	–	44	
			3.0 to 3.6	–	15[2]	30	–	36	
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nY	Figure 2	1.2	–	90	–	–	–	ns
			2.0	–	32	59	–	70	
			2.7	–	24	44	–	52	
			3.0 to 3.6	–	19[2]	36	–	42	

NOTES:
1. All typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3V$

AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$
$V_M = 0.5V * V_{CC}$ at $V_{CC} < 2.7V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$
$V_X = V_{OL}$ $0.1V_{CC}$ at $V_{CC} < 2.7V$
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$
$V_Y = V_{OH} - 0.1V_{CC}$ at $V_{CC} < 2.7V$

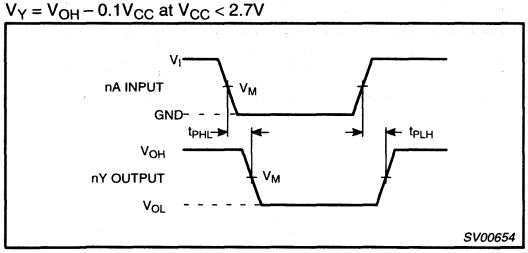


Figure 1. Input (nA) to output (nY) propagation delays.

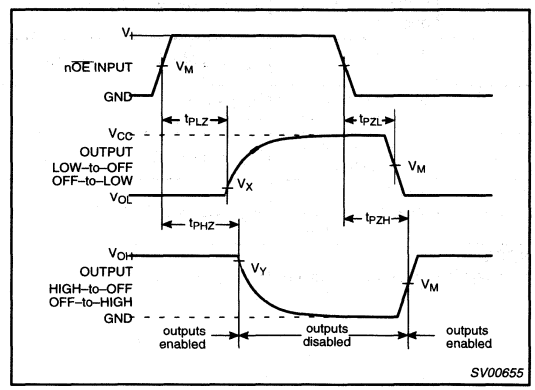
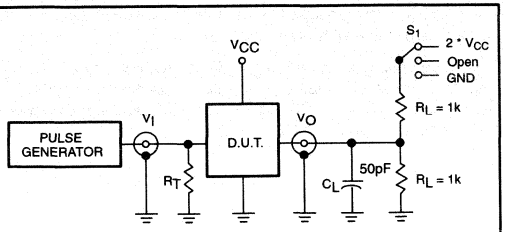


Figure 2. 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00895

Figure 3. Load circuitry for switching times.

Hex buffer/line driver; inverting (3-State) 74LV368

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Inverting outputs
- Output capability: bus driver
- I_{CC} category: SSI

DESCRIPTION

The 74LV368 a low–voltage Si–gate CMOS device and is pin and function compatible with 74HC/HCT368.

The 74LV368 is a hex inverting buffer/line driver with 3–state outputs. The 3–state outputs (nY) are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF–state.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to $n\overline{Y}$	C_L = 15pF V_{CC} = 3.3V	9.0	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	30	pF

NOTES:

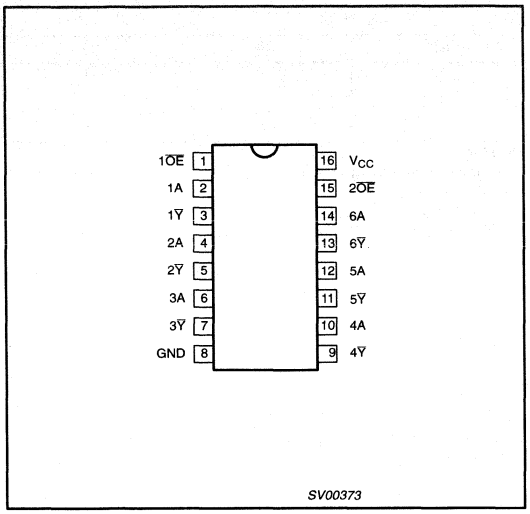
1 C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacitance in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2 The condition is V_I = GND to V_{CC}

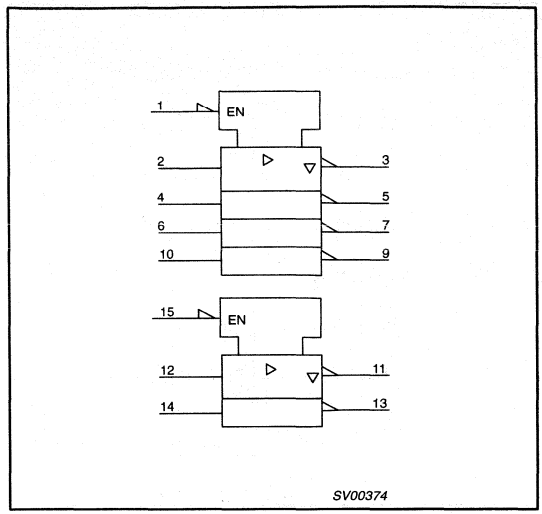
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV368 N	74LV368 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV368 D	74LV368 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV368 DB	74LV368 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV368 PW	74LV368PW DH	SOT403-1

PIN CONFIGURATION



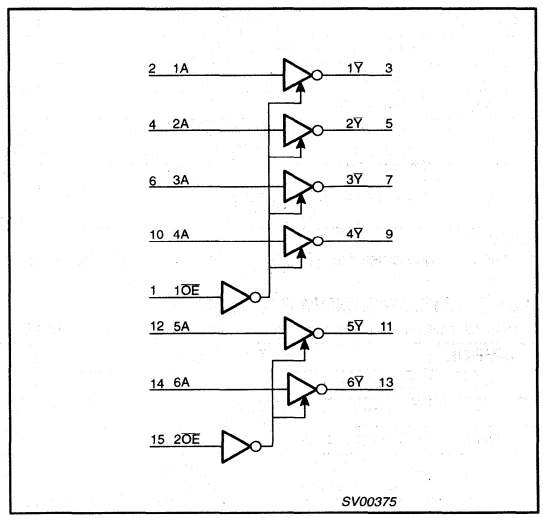
LOGIC SYMBOL (IEEE/IEC)



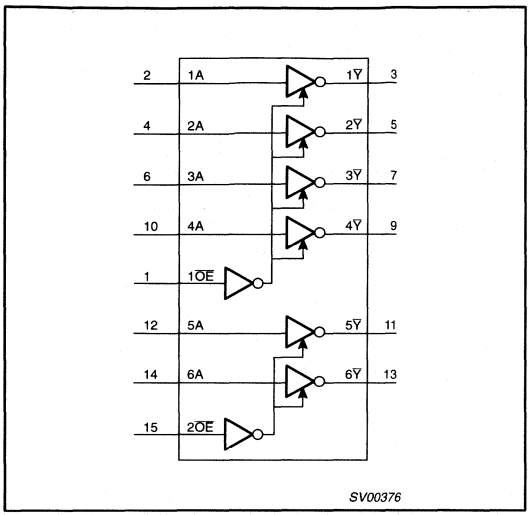
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	1$\overline{OE}$ to 2$\overline{OE}$	Output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	Data inputs
3, 5, 7, 9, 11, 13	1$\overline{Y}$ to 6$\overline{Y}$	Bus outputs
8	GND	Ground (0V)
16	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	$n\overline{Y}$
L	L	H
L	H	L
H	X	Z

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTES:
1 The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134); Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{iL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100μA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		0	0.2		0.2	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			1.0		1.0	μA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND			5		10	μA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	μA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V			500		850	μA

NOTE:

1 All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PZL}/t_{PLH}	Propagation delay nA, to nȲ	Figures, 1, 3	1.2	–	55	–	–	–	ns
			2.0	–	19	36	–	44	
			2.7	–	14	26	–	33	
			3.0 to 3.6	–	10[2]	21	–	26	
t_{PZH}/t_{PZL}	3-State output enable time nOE to nȲ	Figures, 2, 3	1.2	–	75	–	–	–	ns
			2.0	–	26	49	–	60	
			2.7	–	19	36	–	44	
			3.0 to 3.6	–	14[2]	29	–	35	
t_{PHZ}/t_{PLZ}	3-State output disable time nOE to nȲ	Figures, 2, 3	1.2	–	90	–	–	–	ns
			2.0	–	32	59	–	70	
			2.7	–	24	44	–	52	
			3.0 to 3.6	–	19[2]	36	–	42	

NOTE:

1 Unless otherwise stated, all typical values are at T_{amb} = 25°C.

2 Typical value measured at V_{CC} = 3.3V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V

V_M = 0.5V * V_{CC} at V_{CC} < 2.7V

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V

$V_X = V_{OL}$ + 0.1 * V_{CC} at V_{CC} < 2.7V

$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 2.7V

$V_Y = V_{OH}$ – 0.1V_{CC} at V_{CC} < 2.7V

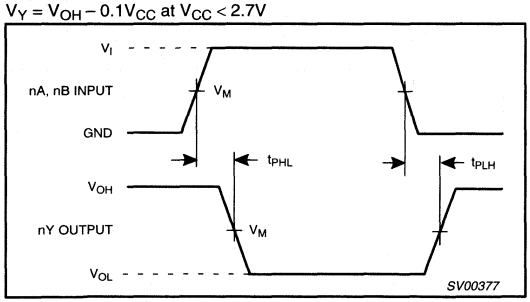


Figure 1.Input (nA) to output (nȲ) propagation delay

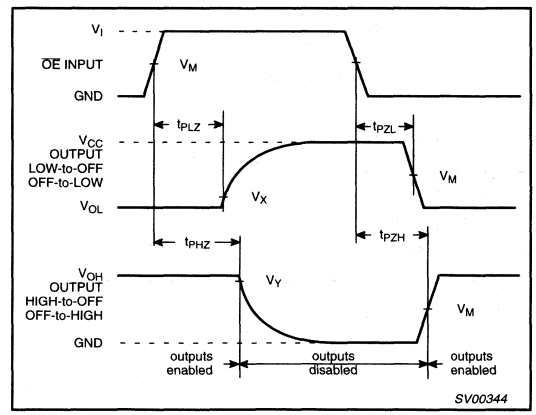
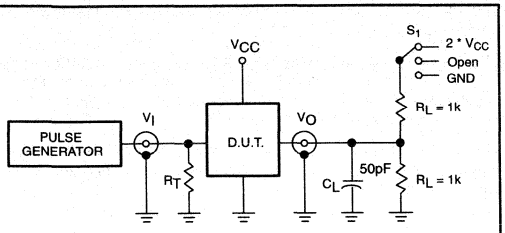


Figure 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00895

Figure 3. Load circuitry for switching times

Octal D-type transparent latch (3-State) 74LV373

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Common 3-State output enable input
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV373 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT373.

The 74LV373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '373' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '373' is functionally identical to the '573', but the '573' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n LE to Q_n	C_L = 15pF V_{CC} = 3.3V	 10 12	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	22	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

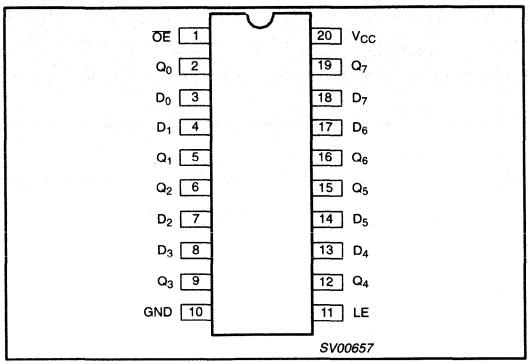
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV373 N	74LV373 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV373 D	74LV373 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV373 DB	74LV373 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV373 PW	74LV373PW DH	SOT360-1

PIN DESCRIPTION

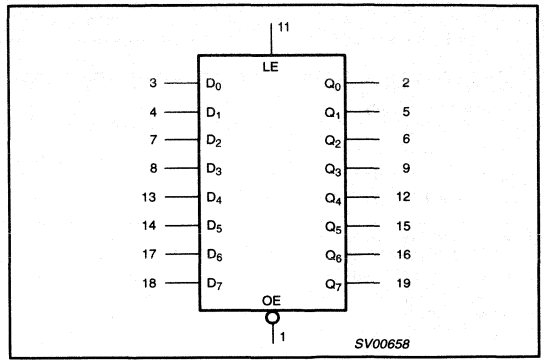
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enabled input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0–Q_7	3-State latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0–D_7	Data inputs
10	GND	Ground (0V)
11	LE	Latch enable input (active HIGH)
20	V_{CC}	Positive supply voltage

Octal D-type transparent latch (3-State) 74LV373

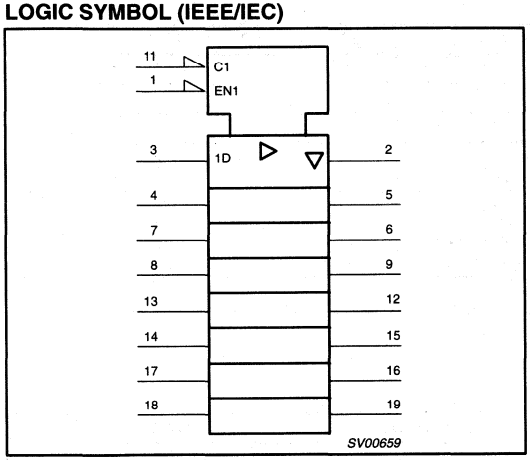
PIN CONFIGURATION



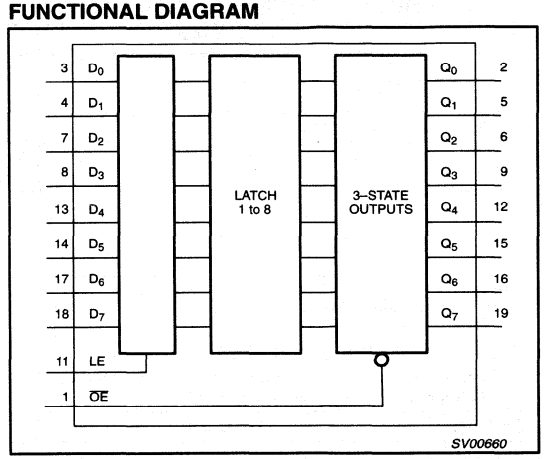
LOGIC SYMBOL



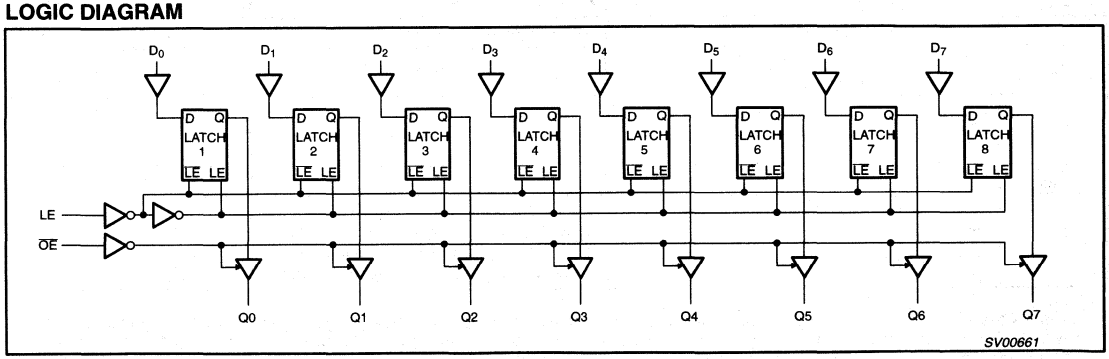
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q_0 to Q_7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n	Figure 1, 5	1.2	–	65	–	–	–	ns
			2.0	–	22	37	–	48	
			2.7	–	16	28	–	35	
			3.0 to 3.6	–	13[2]	22	–	28	
			4.5 to 5.5	–	–	16	–	20	
t_{PHL}/t_{PLH}	Propagation delay LE to Q_n	Figure 2, 5	1.2	–	80	–	–	–	ns
			2.0	–	27	43	–	54	
			2.7	–	20	26	–	33	
			3.0 to 3.6	–	15[2]	25	–	31	
			4.5 to 5.5	–	9.5[3]	19	–	24	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	Figure 3	1.2	–	80	–	–	–	ns
			2.0	–	27	46	–	58	
			2.7	–	20	28	–	35	
			3.0 to 3.6	–	15[2]	27	–	34	
			4.5 to 5.5	–	–	23	–	29	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	Figure 3	1.2	–	75	–	–	–	ns
			2.0	–	27	46	–	58	
			2.7	–	21	28	–	35	
			3.0 to 3.6	–	16[2]	27	–	34	
			4.5 to 5.5	–	–	23	–	29	
t_W	LE pulse width HIGH	Figure 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6[2]	–	24	–	
t_{su}	Setup time D_n to LE	Figure 4	1.2	–	25	–	–	–	ns
			2.0	17	9	–	20	–	
			2.7	13	6	–	15	–	
			3.0 to 3.6	10	5[2]	–	12	–	
t_h	Hold time D_n to LE	Figure 4	1.2	–	–15	–	–	–	ns
			2.0	5	–5	–	5	–	
			2.7	5	–3	–	5	–	
			3.0 to 3.6	5	–3[2]	–	5	–	

NOTES:
1. All typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$V
3. Typical values are measured at $V_{CC} = 5.0$V

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V and ≤ 3.6V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_X = V_{OL} + 0.3V at V_{CC} ≥ 2.7V and ≤ 3.6V
V_X = V_{OL} + 0.1V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_Y = V_{OH} − 0.3V at V_{CC} ≥ 2.7V and ≤ 3.6V
V_Y = V_{OH} − 0.1V_{CC} at V_{CC} < 2.7V and ≥ 4.5V

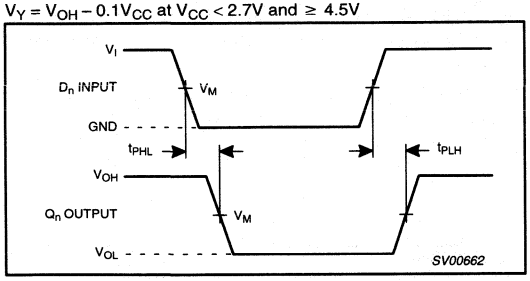


Figure 1. Data input (D_n) to output (Q_n) propagation delays and the output transition times.

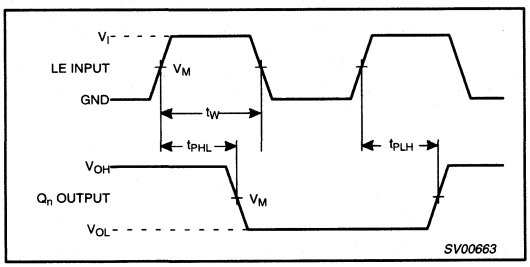


Figure 2. Latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

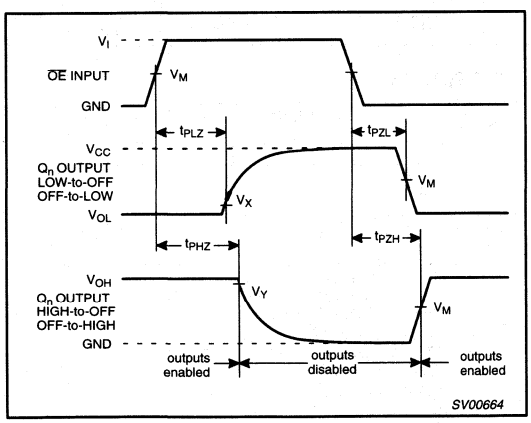


Figure 3. 3-State enable and disable times.

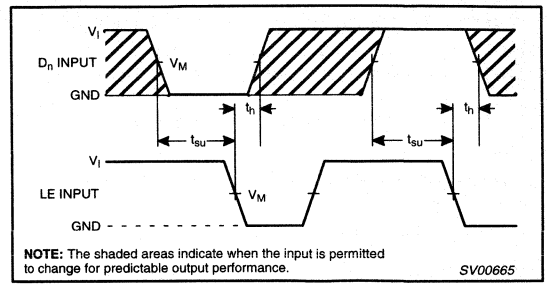


Figure 4. Data set-up and hold times for the D_n input to the LE input.

TEST CIRCUIT

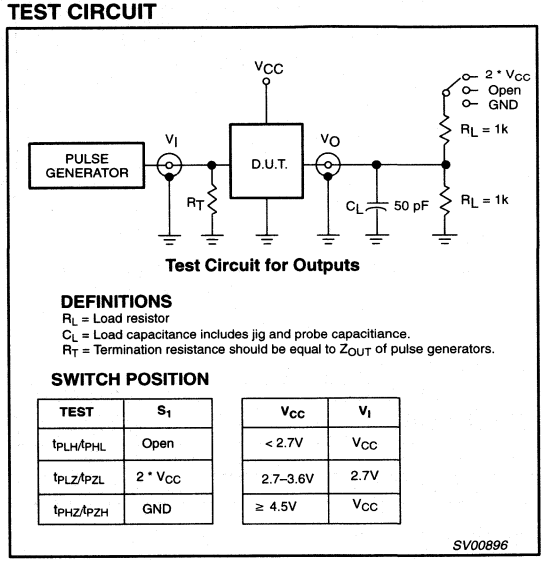


Figure 5. Load circuitry for switching times

Octal D-type flip-flop; positive edge-trigger (3-State) 74LV374

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Common 3-State output enable input
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV374 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT374.

The 74LV374 is an octal D-type flip–flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	C_L = 15pF V_{CC} = 3.3V	14	ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV374 N	74LV374 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV374 D	74LV374 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV374 DB	74LV374 DB	SOT339-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3-State flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive supply voltage

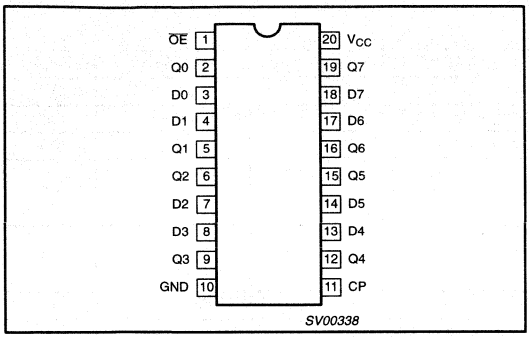
FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	Dn		Q0 to Q7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

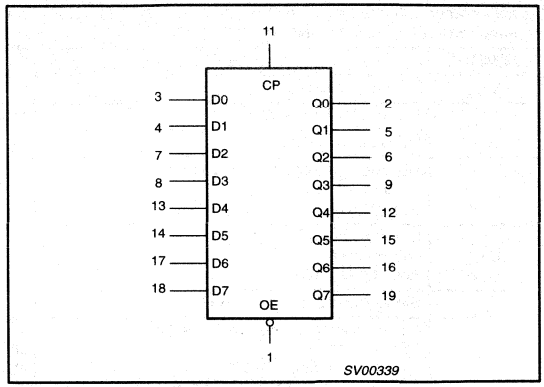
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = High impedance OFF-state
↑ = LOW–to–HIGH clock transition

Octal D-type flip-flop; positive edge-trigger (3-State) 74LV374

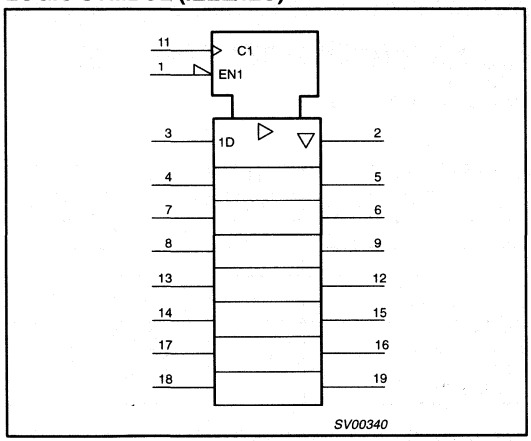
PIN CONFIGURATION



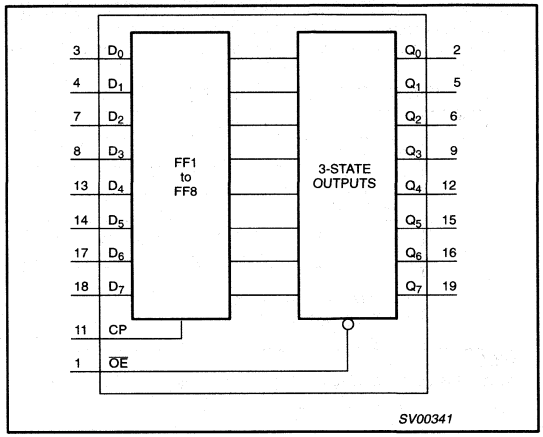
LOGIC SYMBOL



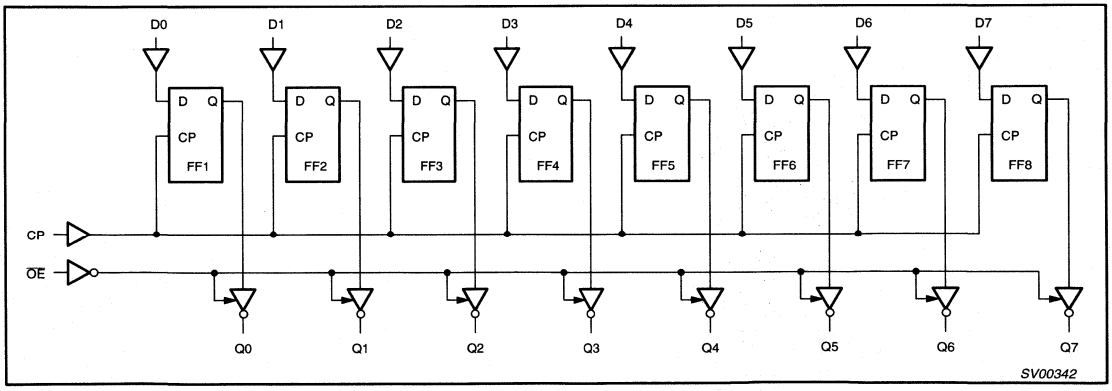
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	 25 35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs –bus driver outputs		 50 70	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTES:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		40	µA
	Quiescent supply current; flip-flops	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		80	
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
	Quiescent supply current; LSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			500		1000	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS −40 to +85 °C			LIMITS −40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	Figure 1	1.2	–	90	–	–	–	ns
			2.0	–	31	39	–	49	
			2.7	–	23	29	–	36	
			3.0 to 3.6	–	17[2]	23	–	29	
			4.5 to 5.5	–	–	19	–	24	
t_{PZH}/t_{PZL}	Propagation delay $\overline{OE}$ to Qn	Figure 2	1.2	–	75	–	–	–	ns
			2.0	–	26	34	–	43	
			2.7	–	19	25	–	31	
			3.0 to 3.6	–	14[2]	20	–	25	
			4.5 to 5.5	–	–	17	–	21	
t_{PHZ}/t_{PLZ}	Propagation delay $\overline{OE}$ to Qn	Figure 2	1.2	–	80	–	–	–	ns
			2.0	–	29	39	–	48	
			2.7	–	22	29	–	36	
			3.0 to 3.6	–	17[2]	24	–	29	
			4.5 to 5.5	–	–	20	–	24	
t_W	Clock pulse width HIGH or LOW	Figure 1	2.0	34	12	–	41	–	ns
			2.7	25	9	–	30	–	
			3.0 to 3.6	20	7[2]	–	24	–	
t_{su}	Set-up time Dn to CP	Figure 3	1.2	–	25	–	–	–	ns
			2.0	22	9	–	26	–	
			2.7	16	6	–	19	–	
			3.0 to 3.6	13	5[2]	–	15	–	
t_h	Hold time Dn to CP	Figure 3	1.2	–	−10	–	–	–	ns
			2.0	5	−3	–	5	–	
			2.7	5	−2	–	5	–	
			3.0 to 3.6	5	−2[2]	–	5	–	
f_{max}	Maximum clock pulse frequency	Figure 2	2.0	15	40	–	12	–	MHz
			2.7	19	58	–	16	–	
			3.0 to 3.6	24	70[2]	–	20	–	

NOTE:

1. Unless otherwise stated, all typical values are at T_{amb} = 25°C.
2. Typical value measured at V_{CC} = 3.3V.
3. Typical value measured at V_{CC} = 5.0V.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V ≤ 3.6V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

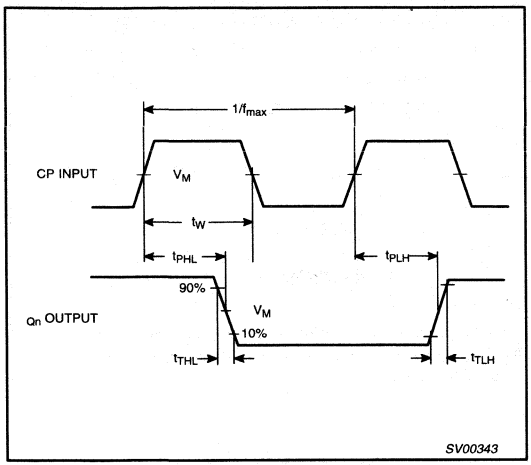


Figure 1. Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency

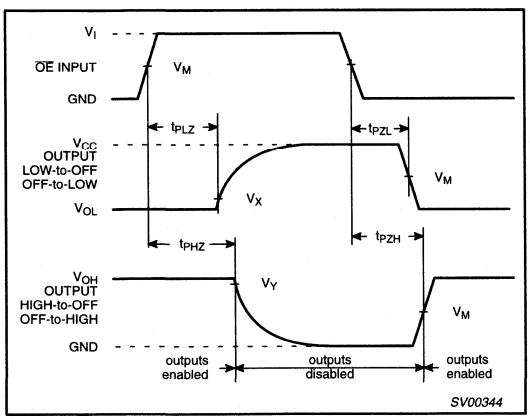


Figure 2. Waveforms showing the 3-state enable and disable times

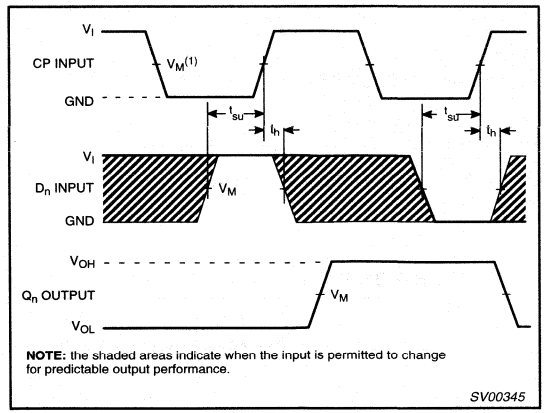
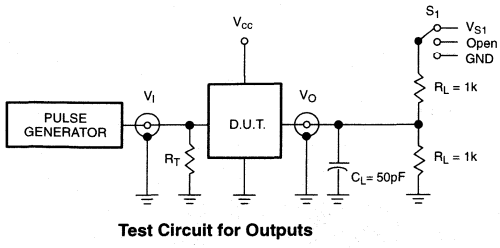


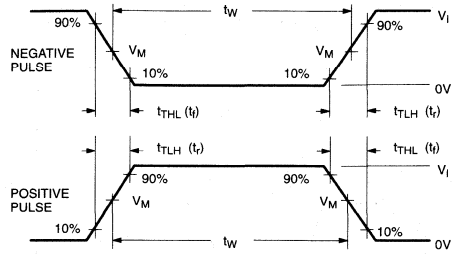
Figure 3. Waveforms showing the data set-up and hold times for the Dn input to the CP input

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{S1}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_{S1}
< 2.7V	V_{CC}	2 * V_{CC}
2.7–3.6V	2.7V	2 * V_{CC}
≥ 4.5 V	V_{CC}	2 * V_{CC}

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SY00044

Figure 4. Load circuitry for switching times

Octal D-type flip-flop with data enable; positive edge-trigger

74LV377

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Ideal for addressable register applications
- Data enable for address and data synchronization applications
- Eight positive-edge triggered D-type flip-flops
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV377 is a low–voltage CMOS device and is pin and function compatible with 74HC/HCT377.

The 74LV377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. A common clock (CP) input loads all flip-flops simultaneously when the data enable ($\overline{E}$) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop. The $\overline{E}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	C_L = 15pF, V_{CC} = 3.3V	13	ns
f_{max}	Maximum clock frequency		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	20	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV377 N	74LV377 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV377 D	74LV377 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV377 DB	74LV377 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV377 PW	74LV377PW DH	SOT360-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{E}$	Data enable input (active-LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

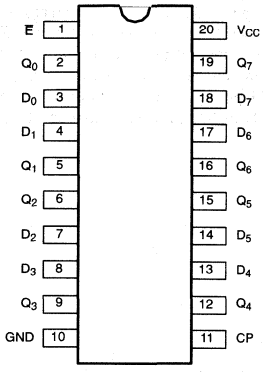
OPERATING MODES	INPUTS			OUTPUTS
	CP	$\overline{E}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	No change
	X	H	X	No change

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW–to–HIGH CP transition
X = Don't care

Octal D-type flip-flop with data enable; positive edge-trigger

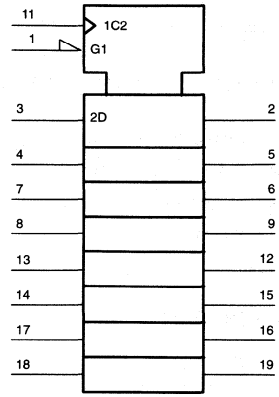
74LV377

PIN CONFIGURATION



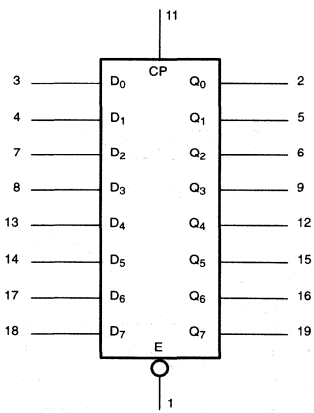
SV00667

LOGIC SYMBOL (IEEE/IEC)



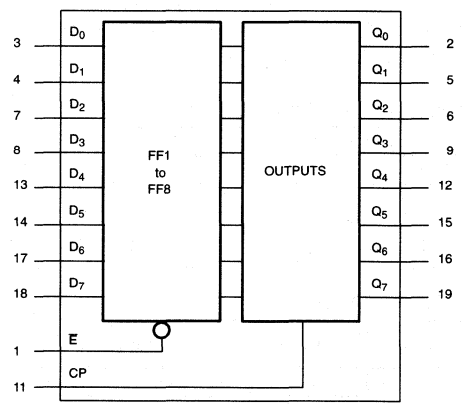
SV00669

LOGIC SYMBOL



SV00668

FUNCTIONAL DIAGRAM



SV00670

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	
I_I	Input leakage current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC} - 0.6V$			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	Figure 1	1.2	–	80	–	–	–	ns
			2.0	–	27	51	–	61	
			2.7	–	20	38	–	45	
			3.0 to 3.6	–	15[2]	30	–	36	
t_W	Clock pulse width HIGH or LOW	Figure 2	2.0	34	9	–	41	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5[2]	–	24	–	
t_{su}	Set-up time D_n to CP	Figure 2	1.2	–	25	–	–	–	ns
			2.0	22	9	–	26	–	
			2.7	16	6	–	19	–	
			3.0 to 3.6	13	5[2]	–	15	–	
t_{su}	Set-up time $\overline{E}$ to CP	Figure 2	1.2	–	10	–	–	–	ns
			2.0	22	4	–	26	–	
			2.7	16	3	–	19	–	
			3.0 to 3.6	13	2[2]	–	15	–	
t_h	Hold time D_n to CP	Figure 2	1.2	–	−15	–	–	–	ns
			2.0	5	−5	–	5	–	
			2.7	5	−4	–	5	–	
			3.0 to 3.6	5	−3[2]	–	5	–	
t_h	Hold time $\overline{E}$ to CP	Figure 2	1.2	–	−5	–	–	–	ns
			2.0	5	−2	–	5	–	
			2.7	5	−2	–	5	–	
			3.0 to 3.6	5	−1[2]	–	5	–	
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	40	–	12	–	MHz
			2.7	19	58	–	16	–	
			3.0 to 3.6	24	70[2]	–	20	–	

NOTES:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25$°C.
2. Typical value measured at $V_{CC} = 3.3$V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

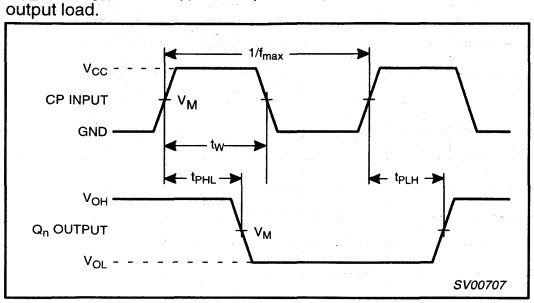


Figure 1. Clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

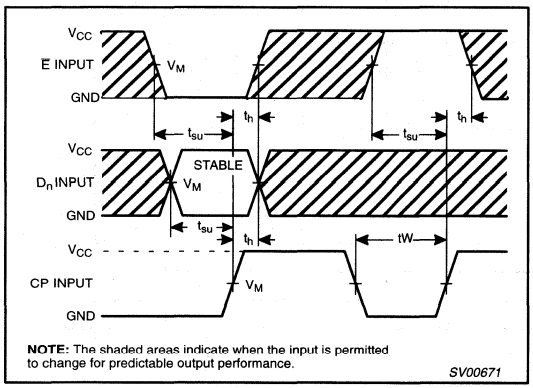


Figure 2. Data set-up and hold times from the data input (Dn) and from the enable input ($\overline{E}$) to the clock (CP).

TEST CIRCUIT

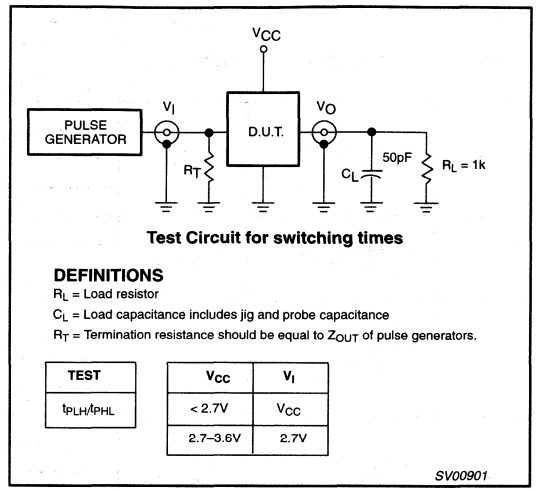


Figure 3. Load circuitry for switching times

Dual 4-bit binary ripple counter — 74LV393

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV393 is a low–voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT393.

The 74LV393 is a dual 4-bit binary ripple counter with separate clocks (1$\overline{CP}$, 2$\overline{CP}$) and master reset (1MR, 2MR) inputs to each counter.

The operation of each half of the "393" is the same as the "93" except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description.

A HIGH level on the nMR input overrides the clock and sets the outputs LOW.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay n$\overline{CP}$ to nQ_0 nQ to nQn+1 nMR to nQn	C_L = 15pF V_{CC} = 3.3V	12 4 11	ns
f_{max}	Maximum clock frequency		99	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_I = GND to V_{CC} [1]	23	pF

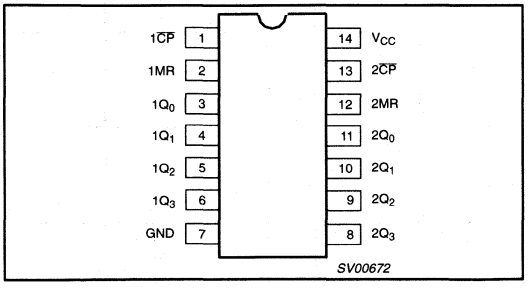
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +125°C	74LV393 N	74LV393 N	SOT27-1
14-Pin Plastic SO	–40°C to +125°C	74LV393 D	74LV393 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LV393 DB	74LV393 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV393 PW	74LV393PW DH	SOT402-1

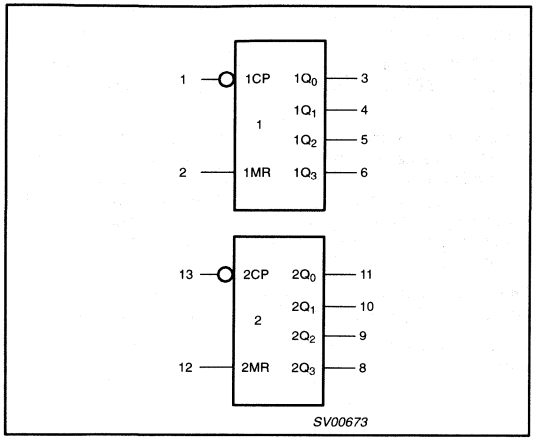
PIN CONFIGURATION



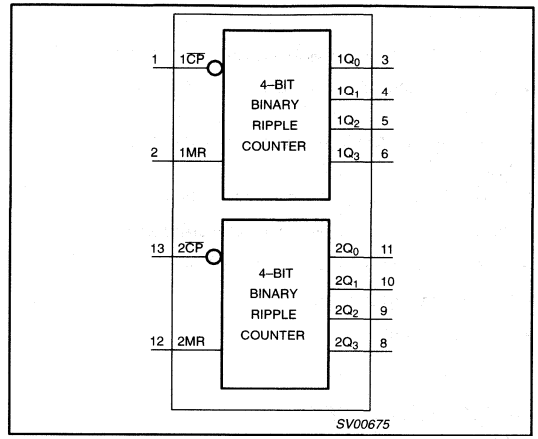
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 13	1$\overline{CP}$, 2$\overline{CP}$	Clock inputs (HIGH-to-LOW, edge-triggered)
2, 12	1MR, 2MR	Asynchronous master reset inputs (active HIGH)
3, 4, 5, 6 11, 10, 9, 8	$1Q_0$ to $1Q_3$ $2Q_0$ to $2Q_3$	Flip-flop outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

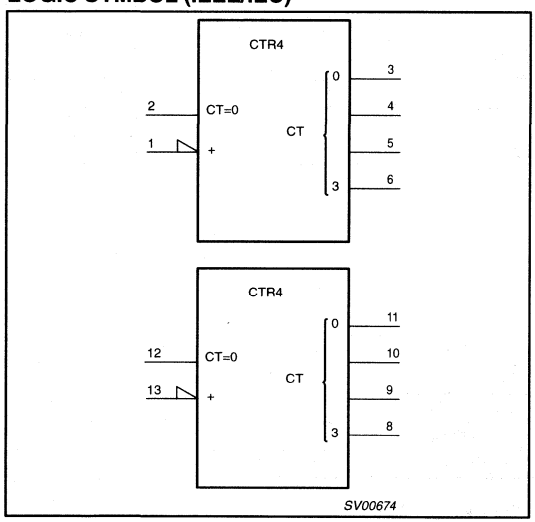
LOGIC SYMBOL



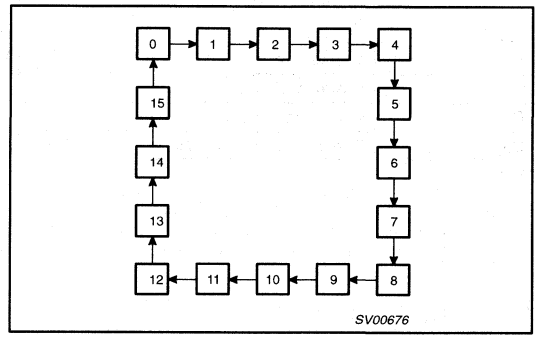
FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



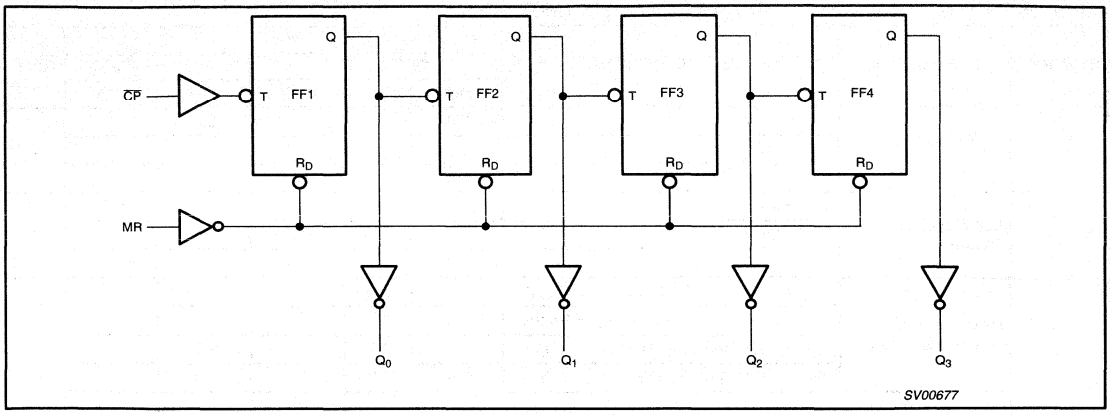
STATE DIAGRAM



COUNT SEQUENCE FOR 1 COUNTER

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTES:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} =3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	
I_I	Input leakage current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC} - 0.6V$			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $n\overline{CP}$ to nQ_0	Figure 1	1.2	–	75	–	–	–	ns
			2.0	–	26	49	–	60	
			2.7	–	19	36	–	44	
			3.0 to 3.6	–	14[2]	29	–	35	
t_{PHL}/t_{PLH}	Propagation delay nQn to nQn+1	Figure 1	1.2	–	25	–	–	–	ns
			2.0	–	9	17	–	20	
			2.7	–	6	13	–	15	
			3.0 to 3.6	–	5[2]	10	–	12	
t_{PHL}	Propagation delay nMR to nQn	Figure 2	1.2	–	70	–	–	–	ns
			2.0	–	24	44	–	54	
			2.7	–	18	33	–	40	
			3.0 to 3.6	–	13[2]	26	–	32	
t_W	Clock pulse width HIGH or LOW	Figure 1	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6[2]	–	24	–	
t_W	Master reset pulse width; HIGH	Figure 2	2.0	34	12	–	41	–	ns
			2.7	25	9	–	30	–	
			3.0 to 3.6	20	7[2]	–	24	–	
t_{rem}	Removal time nMR to $n\overline{CP}$	Figure 2	1.2	–	5	–	–	–	ns
			2.0	5	2	–	5	–	
			2.7	5	2	–	5	–	
			3.0 to 3.6	5	1[2]	–	5	–	
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	14	53	–	12	–	MHz
			2.7	19	72	–	16	–	
			3.0 to 3.6	24	90[2]	–	20	–	

NOTES:

1. All typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$V

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5 * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

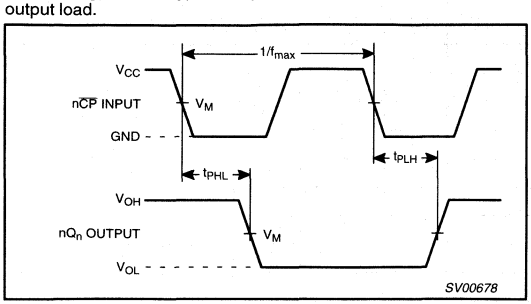


Figure 1. Clock (n$\overline{CP}$) to output (1Qn, 2Qn) propagation delays, the clock pulse width, and the maximum clock frequency

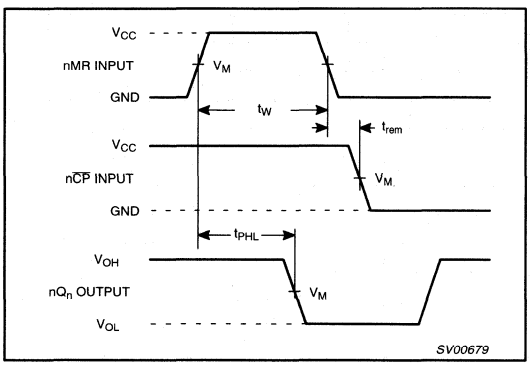


Figure 2. Master reset (nMR) pulse width, the master reset to output (Qn) propagation delays, and the master reset to clock (n$\overline{CP}$) removal time

TEST CIRCUIT

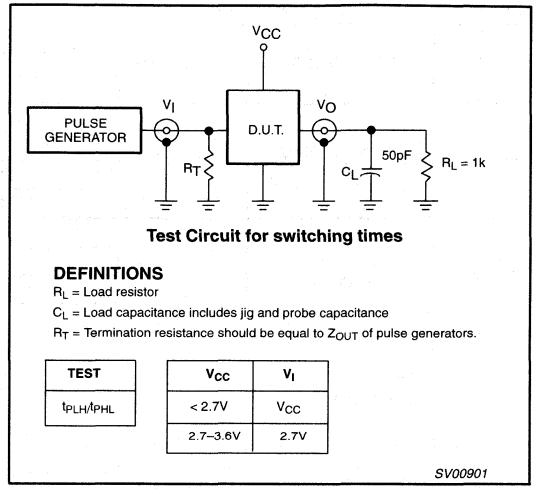


Figure 3. Load circuitry for switching times

Octal buffer/line driver (3-State) 74LV541

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Non-inverting outputs
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV541 is a low–voltage CMOS device and is pin and function compatible with 74HC/HCT541.

The 74LV541 is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$.

A HIGH on $\overline{OE}$n causes the outputs to assume a high impedance OFF–state.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n to Y_n	C_L = 15pF V_{CC} = 3.3V	10	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC} [1]	37	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV541 N	74LV541 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV541 D	74L541 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV541 DB	74LV541 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV541 PW	74LV541PW DH	SOT360-1

PIN DESCRIPTION

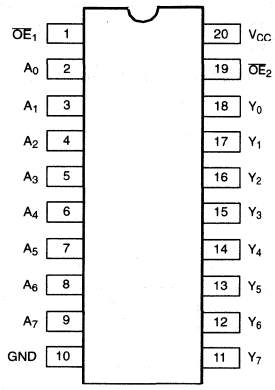
PIN NUMBER	SYMBOL	FUNCTION
1, 19	$\overline{OE}_1$, $\overline{OE}_2$	Output enable input (active-LOW)
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	Data inputs
10	GND	Ground (0V)
18, 17, 16, 15, 14, 13, 12, 11	Y_0 to Y_7	Bus outputs
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_1$	$\overline{OE}_2$	nA	nY
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

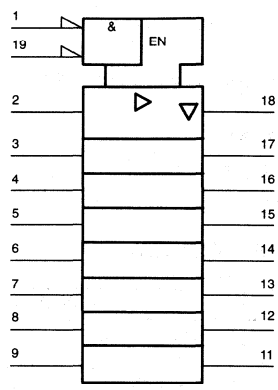
H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

PIN CONFIGURATION



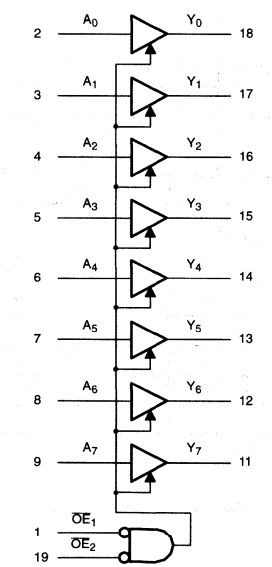
SV00680

LOGIC SYMBOL (IEEE/IEC)



SV00682

LOGIC SYMBOL



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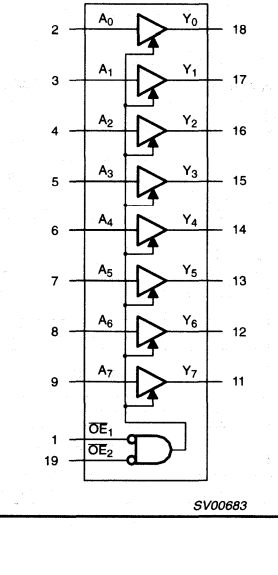
FUNCTIONAL DIAGRAM



SV00683

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay A_n to Y_n	Figure 1	1.2	–	60	–	–	–	ns
			2.0	–	20	39	–	46	
			2.7	–	15	29	–	34	
			3.0 to 3.6	–	11[2]	23	–	27	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}_n$ to Y_n	Figure 2	1.2	–	100	–	–	–	ns
			2.0	–	34	65	–	77	
			2.7	–	25	48	–	56	
			3.0 to 3.6	–	19[2]	38	–	45	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}_n$ to Y_n	Figure 2	1.2	–	100	–	–	–	ns
			2.0	–	36	66	–	78	
			2.7	–	27	48	–	58	
			3.0 to 3.6	–	21[2]	39	–	47	

NOTES:
1. Unless otherwise stated, all typical values are at $T_{amb} = 25°C$.
2. Typical value measured at $V_{CC} = 3.3$V.

AC WAVEFORMS

$V_M = 1.5$V at $V_{CC} \geq 2.7$V
$V_M = 0.5 * V_{CC}$ at $V_{CC} < 2.7$V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$V at $V_{CC} \geq 2.7$V
$V_X = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7$V
$V_Y = V_{OH} - 0.3$V at $V_{CC} \geq 2.7$V
$V_Y = V_{OH} - 0.1\ V_{CC}$ at $V_{CC} < 2.7$V

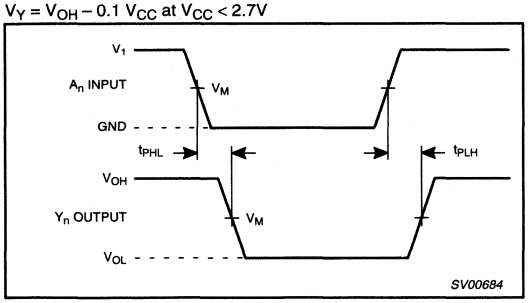


Figure 1. Input (A_n) to output (Y_n) propagation delays

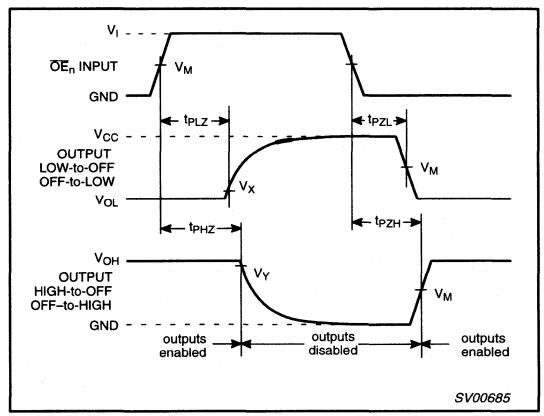
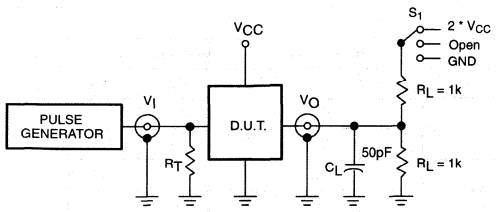


Figure 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00895

Figure 3. Load circuitry for switching times

Octal D-type transparent latch (3-State) 74LV573

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/microcomputer
- Common 3-State output enable input
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV573 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT573.

The 74LV573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '573' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '573' is functionally identical to the '563' and the '373', but the '563' has inverted outputs and the '373' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn LE to Qn	C_L = 15pF V_{CC} = 3.3V	 12 13	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	26	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV573 N	74LV573 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV573 D	74LV573 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV573 DB	74LV573 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV573 PW	74LV573PW DH	SOT360-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enabled input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0–D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0–Q7	Data outputs
10	GND	Ground (0V)
11	LE	Latch enable input (active HIGH)
20	VCC	Positive supply voltage

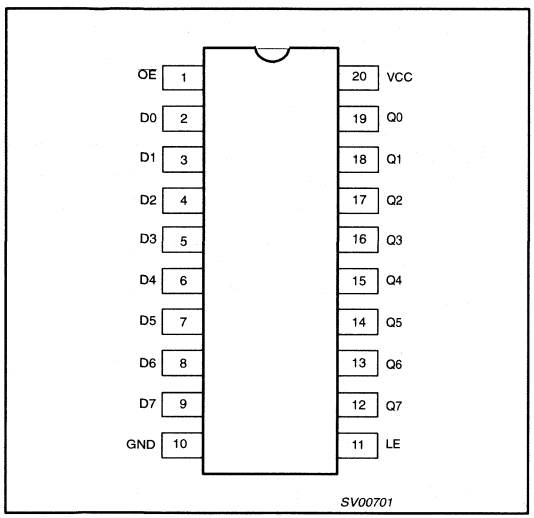
Octal D-type transparent latch (3-State) 74LV573

FUNCTION TABLE

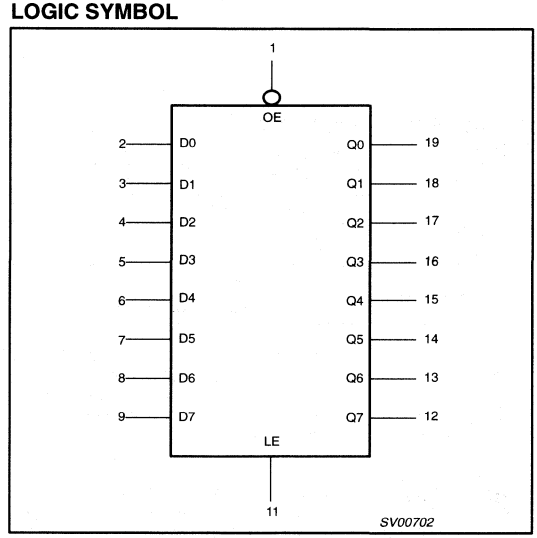
OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q0 to Q7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = High impedance OFF-state

PIN CONFIGURATION

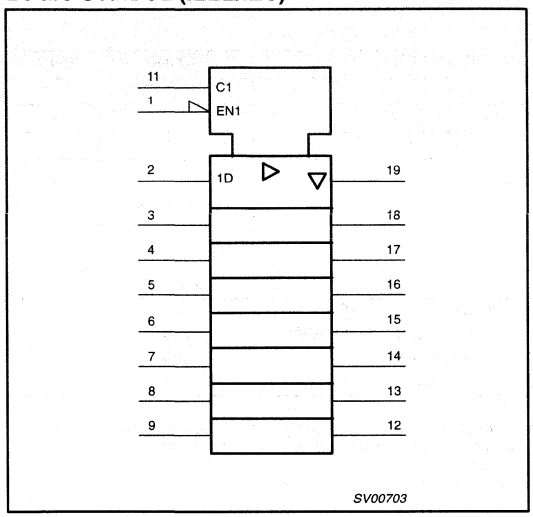


LOGIC SYMBOL

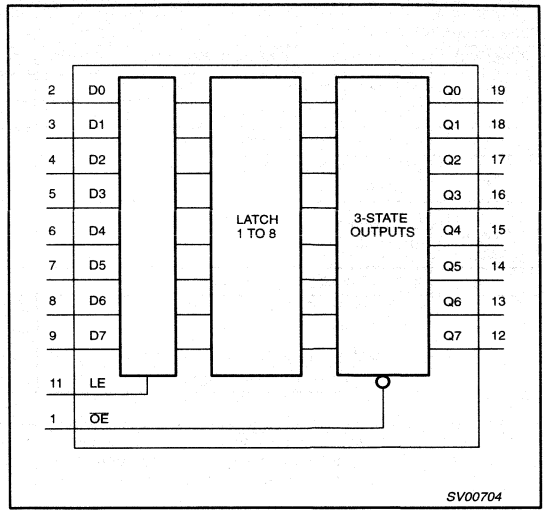


Octal D-type transparent latch (3-State) 74LV573

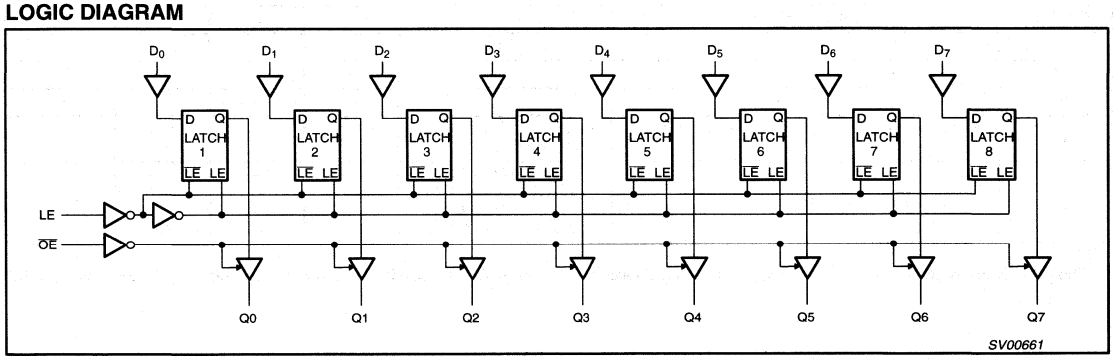
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{tot}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	
		V_{CC} = 4.5V;V_I = V_{IH} or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn	Figures 1, 5	1.2	–	75	–	–	–	ns
			2.0	–	26	39	–	49	
			2.7	–	19	29	–	36	
			3.0 to 3.6	–	14[2]	23	–	29	
			4.5 to 5.5	–	–	19	–	24	
t_{PHL}/t_{PLH}	Propagation delay LE to Qn	Figures 2, 5	1.2	–	80	–	–	–	ns
			2.0	–	27	43	–	53	
			2.7	–	20	31	–	34	
			3.0 to 3.6	–	15[2]	25	–	31	
			4.5 to 5.5	–	–	21	–	26	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Qn	Figures 3, 5	1.2	–	70	–	–	–	ns
			2.0	–	24	37	–	48	
			2.7	–	18	28	–	35	
			3.0 to 3.6	–	13[2]	22	–	28	
			4.5 to 5.5	–	–	18	–	23	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Qn	Figures 3, 5	1.2	–	80	–	–	–	ns
			2.0	–	29	39	–	48	
			2.7	–	22	29	–	36	
			3.0 to 3.6	–	17[2]	24	–	29	
			4.5 to 5.5	–	–	20	–	24	
t_W	LE pulse width HIGH	Figure 2	2.0	34	9	–	41	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5[2]	–	24	–	
t_{su}	Setup time Dn to LE	Figure 4	1.2	–	25	–	–	–	ns
			2.0	17	9	–	20	–	
			2.7	13	6	–	15	–	
			3.0 to 3.6	10	5[2]	–	12	–	
t_h	Hold time Dn to LE	Figure 4	1.2	–	5	–	–	–	ns
			2.0	8	2	–	8	–	
			2.7	8	2	–	8	–	
			3.0 to 3.6	8	1[2]	–	8	–	

NOTES:

All typical values are measured at $T_{amb} = 25°C$

1. Typical values are measured at $V_{CC} = 3.3$V

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V and ≤ 3.6V
V_M = 0.5 * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_X = V_{OL} + 0.3V at V_{CC} > 2.7V and < 3.6V
V_X = V_{OL} + 0.1V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_Y = V_{OH} − 0.3V at V_{CC} ≥ 2.7V and ≤ 3.6V
V_Y = V_{OH} − 0.1V_{CC} at V_{CC} < 2.7V and ≥ 4.5V

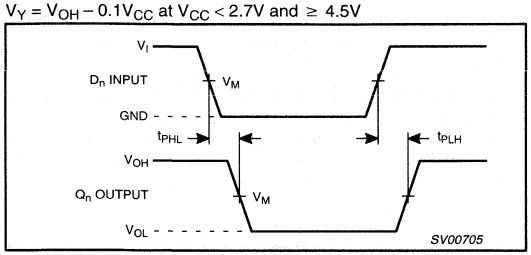


Figure 1. Data input (D_n) to output (Q_n) propagation delays and the output transition times

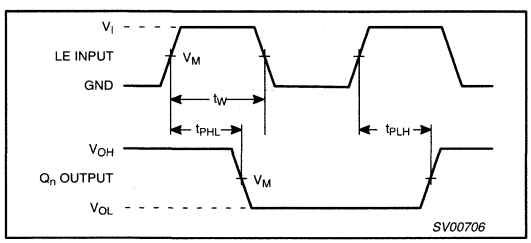


Figure 2. Latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

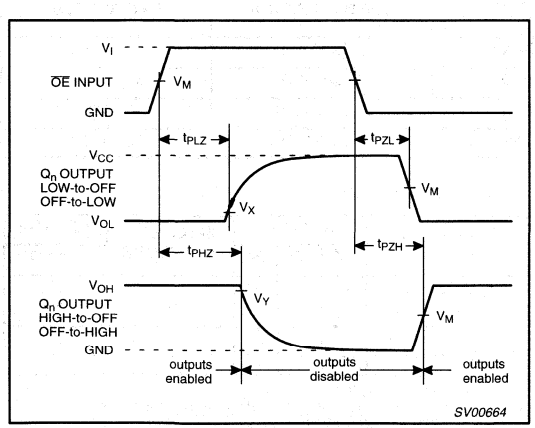


Figure 3. 3-State enable and disable times

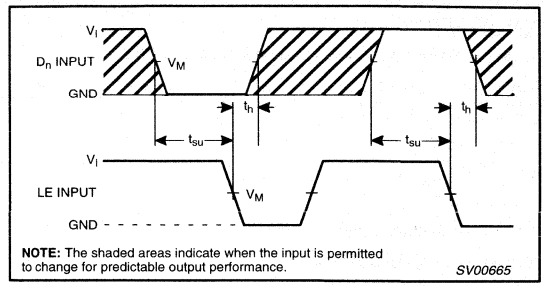
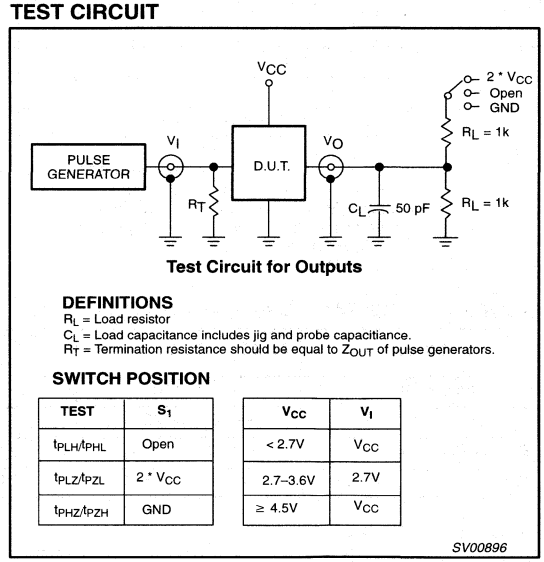


Figure 4. Data set-up and hold times for the D_n input to the LE input

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS
R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitiance.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5V	V_{CC}

SV00896

Figure 5. Load circuitry for switching times

Octal D-type flip-flop; positive edge-trigger (3-State) 74LV574

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Common 3-State output enable input
- Output capability: bus driver
- I_{CC} category: MSI

DESCRIPTION

The 74LV574 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT574.

The 74LV574 is an octal D-type flip–flop featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	C_L = 15pF V_{CC} = 3.3V	13	ns
f_{max}	Maximum clock frequency	C_L = 15pF, V_{CC} = 3.3V	77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV574 N	74LV574 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV574 D	74LV574 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV574 DB	74LV574 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV574 PW	74LV574PW DH	SOT360-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enabled input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0–D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0–Q7	3-State flip-flop outputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	VCC	Positive supply voltage

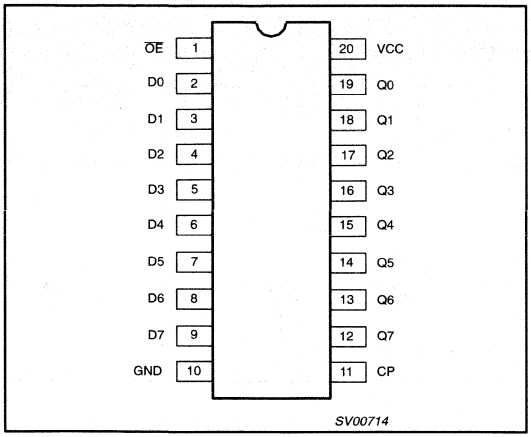
FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	Dn		Q0 to Q7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

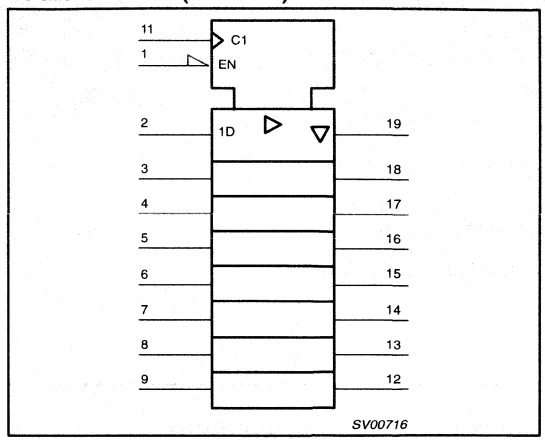
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = High impedance OFF-state
↑ = LOW–to–HIGH clock transition

Octal D-type flip-flop; positive edge-trigger (3-State) 74LV574

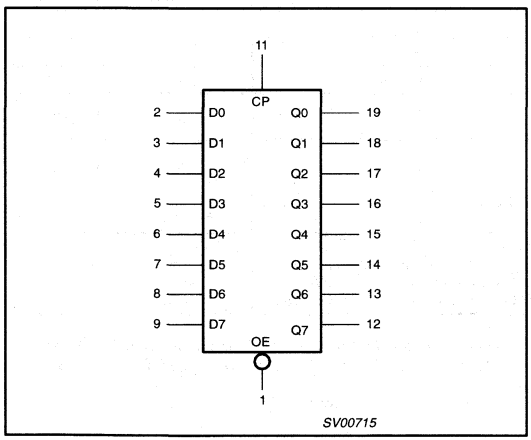
PIN CONFIGURATION



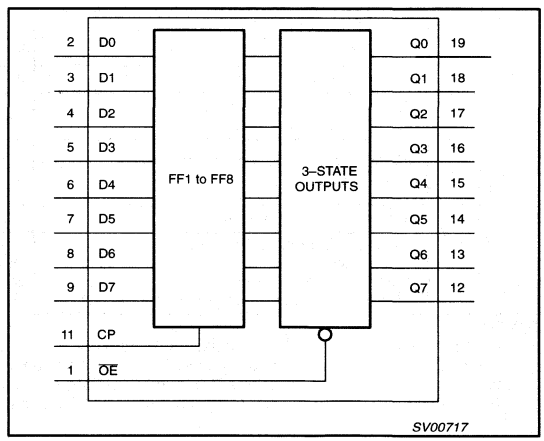
LOGIC SYMBOL (IEEE/IEC)



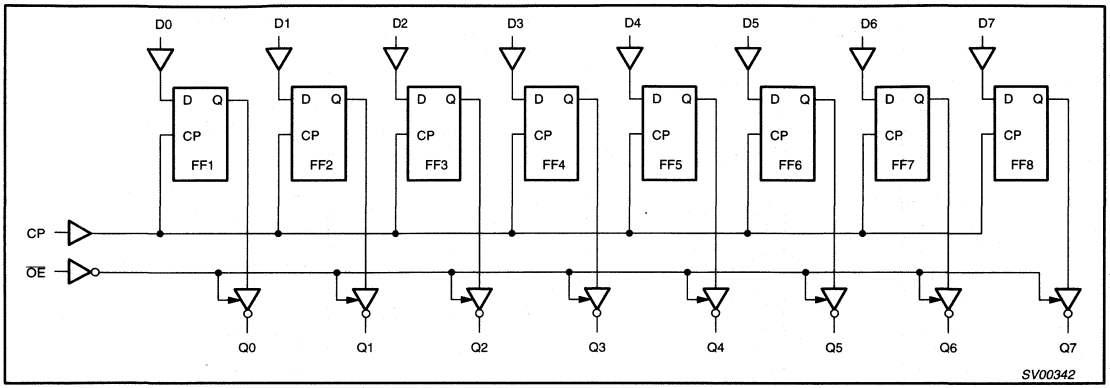
LOGIC SYMBOL



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTES:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 16mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 16mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 5.5V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	Figure 1, 4	1.2	–	80	–	–	–	ns
			2.0	–	27	34	–	43	
			2.7	–	20	25	–	31	
			3.0 to 3.6	–	15[2]	20	–	25	
			4.5 to 5.5	–	–	17	–	21	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Qn	Figure 2, 4	1.2	–	70	–	–	–	ns
			2.0	–	24	34	–	43	
			2.7	–	18	25	–	31	
			3.0 to 3.6	–	13[2]	20	–	25	
			4.5 to 5.5	–	–	17	–	21	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Qn	Figure 2, 4	1.2	–	75	–	–	–	ns
			2.0	–	27	27	–	34	
			2.7	–	21	21	–	26	
			3.0 to 3.6	–	16[2]	17	–	21	
			4.5 to 5.5	–	–	15	–	18	
t_W	Clock pulse width HIGH or LOW	Figure 1	2.0	34	9	–	41	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5[2]	–	24	–	
t_{su}	Set-up time Dn to CP	Figure 3	1.2	–	10	–	–	–	ns
			2.0	22	4	–	26	–	
			2.7	16	3	–	19	–	
			3.0 to 3.6	13	2[2]	–	15	–	
t_h	Hold time Dn to CP	Figure 3	1.2	–	–10	–	–	–	ns
			2.0	5	–4	–	5	–	
			2.7	5	–3	–	5	–	
			3.0 to 3.6	5	–2[2]	–	5	–	
f_{max}	Maximum clock pulse frequency	Figure 1	2.0	15	40	–	12	–	MHz
			2.7	19	58	–	16	–	
			3.0 to 3.6	24	70[2]	–	20	–	

NOTE:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25$°C.
2. Typical value measured at $V_{CC} = 3.3$V.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V and ≤ 3.6V
V_M = 0.5 * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_X = V_{OL} + 0.3V at V_{CC} ≥ 2.7V and ≤ 3.6V
V_X = V_{OL} + 0.1V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_Y = V_{OH} − 0.3V at V_{CC} ≥ 2.7V and ≤ 3.6V
V_Y = V_{OH} − 0.1V_{CC} at V_{CC} < 2.7V and ≥ 4.5V

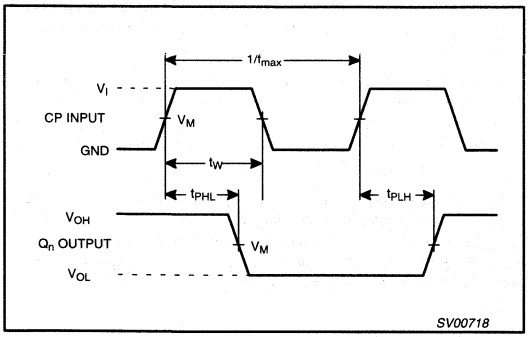


Figure 1. Clock (CP) to output (Qn) propagation delays, the clock pulse (CP) and the maximum clock pulse frequency

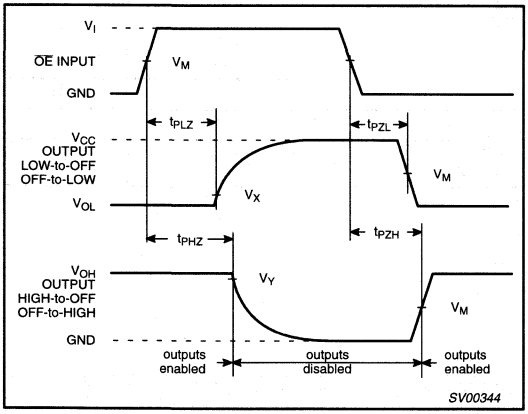


Figure 2. 3-state enable and disable times

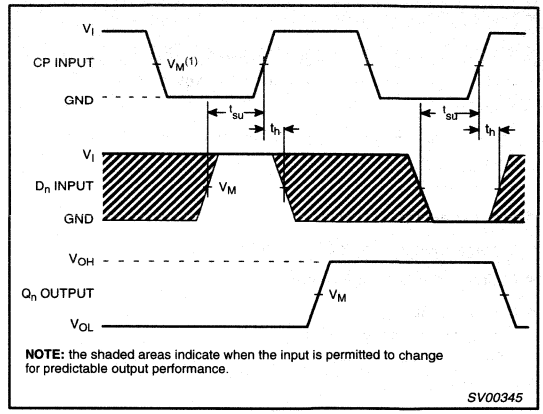
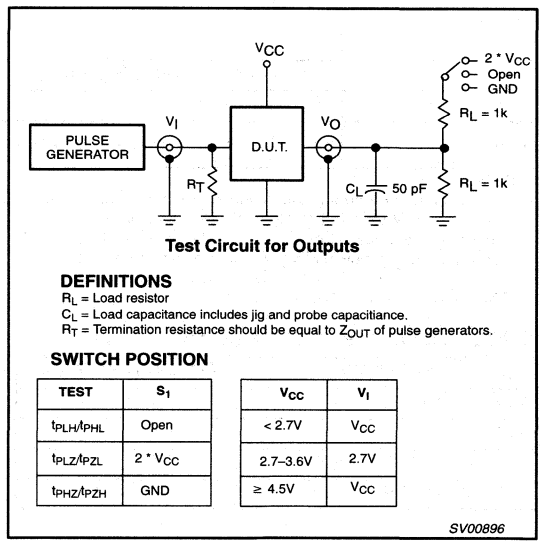


Figure 3. Data set-up and hold times for the Dn input to the CP input

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT



TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5V	V_{CC}

Figure 4. Load circuitry for switching times

8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

74LV595

FEATURES

- Optimized for Low Voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-State outputs
- Shift register with direct clear
- Output capability:
  - parallel outputs; bus driver
  - serial output; standard
- I_{CC} category: MSI

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register

DESCRIPTION

The 74LV595 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT595.

The74LV595 is an 8-stage serial shift register with a storage register and 3-State outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_{CP} input. The data in each register is transferred to the storage register on a positive-going transition of the ST_{CP} input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (D_S) and a serial standard output ($Q_{7'}$) all for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-State bus driver outputs. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay SH_{CP} to $Q_{7'}$ ST_{CP} to $Q_{7'}$ $\overline{MR}$ to $Q_{7'}$	C_L = 15pF V_{CC}= 3.3V	 15 16 14	ns
f_{max}	Maximum clock frequency SH_{CP}, ST_{CP}		77	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_{CC} = 3.3V Notes 1 and 2	115	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV595 N	74LV595 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV595 D	74LV595 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV595 DB	74LV595 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV595 PW	74LV595PW DH	SOT403-1

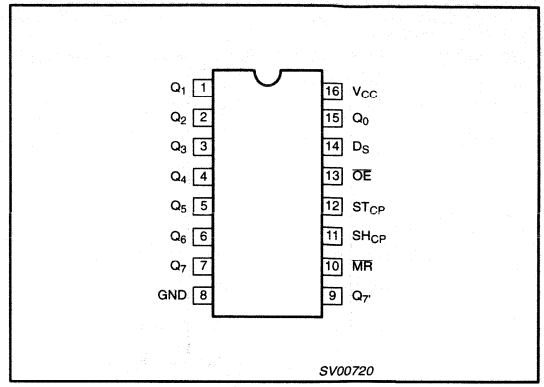
8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

74LV595

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
15, 1, 2, 3, 4, 5, 6, 7	Q_0 to Q_7	Parallel data output
8	GND	Ground (0V)
9	$Q_{7'}$	Serial data output
10	$\overline{MR}$	Master reset (active LOW)
11	SH_{CP}	Shift register clock input
12	ST_{CP}	Storage register clock input
13	$\overline{OE}$	Output enable input (active LOW)
14	D_S	Serial data input
16	V_{CC}	Positive supply voltage

PIN CONFIGURATION



FUNCTION TABLE

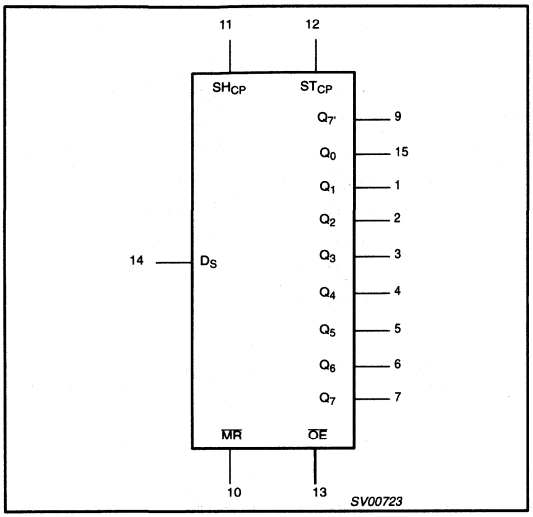
INPUTS					OUTPUTS		FUNCTION
SH_{CP}	ST_{CP}	$\overline{OE}$	$\overline{MR}$	D_S	$Q_{7'}$	Qn	
X	X	L	L	X	L	NC	A LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	Empty shift register loaded into storage register
X	X	H	L	X	L	Z	Shift register clear. Parallel outputs in high-impedance OFF-states
↑	X	L	H	H	$Q_{6'}$	NC	Logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal $Q_{6'}$) appears on the serial output ($Q_{7'}$)
X	↑	L	H	X	NC	$Q_{n'}$	Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	$Q_{6'}$	$Q_{n'}$	Contents of shift register shifted through. Previous contents of the shift register are transferred to the storage register and the parallel output stages

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state
NC = No change
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW transition

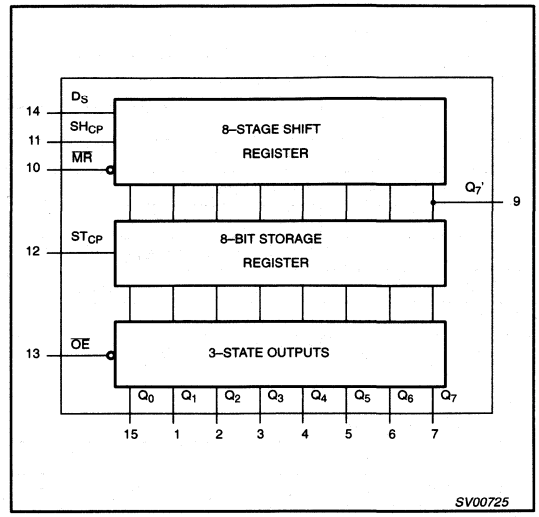
8-bit serial-in/serial or parallel-out shift register with output latches (3-State)

74LV595

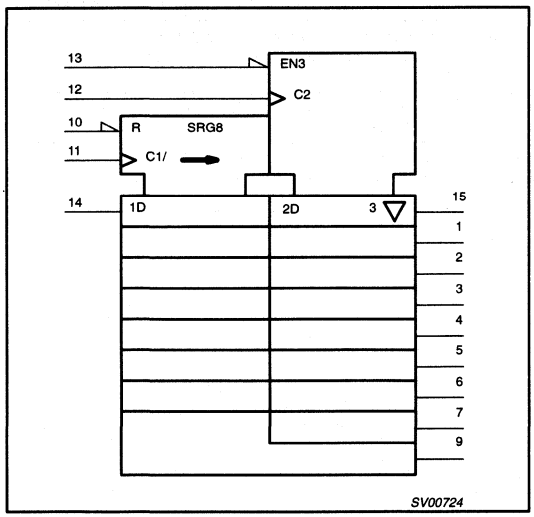
LOGIC SYMBOL



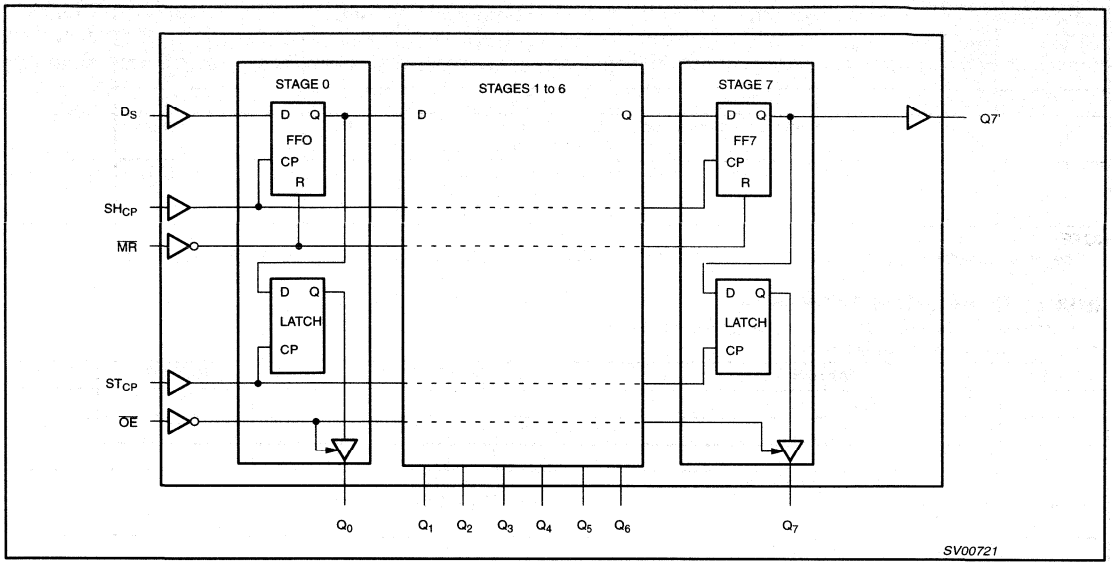
FUNCTIONAL DIAGRAM



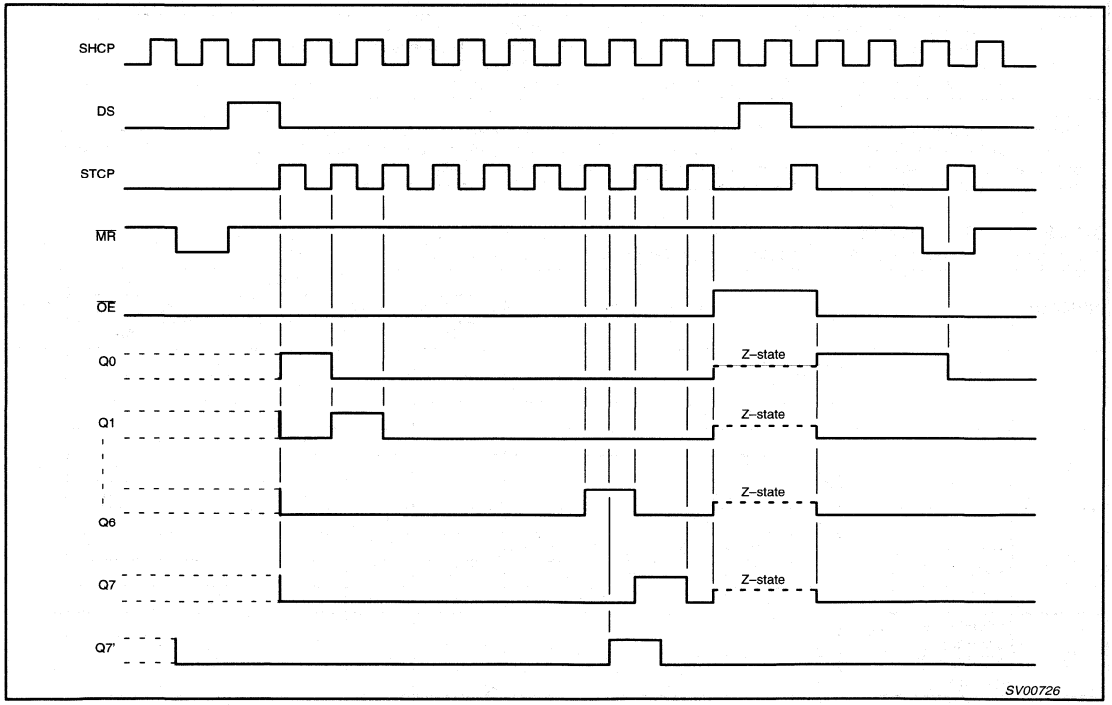
LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



TIMING DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} =3.6V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25 35	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs –bus driver outputs		50 70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V

DC CHARACTERISTICS (Continued)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
V_{OH}	HIGH level output voltage; BUS driver outputs	V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; $-I_O$ = 8mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
V_{OL}	LOW level output voltage; BUS driver outputs	V_{CC} = 3.0V;V_I = V_{IH} or V_{IL}; I_O = 8mA		0.20	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			5		10	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay SH_{CP} to Q_7'	Figure 1	1.2	–	95	–	–	–	ns
			2.0	–	32	61	–	75	
			2.7	–	24	45	–	55	
			3.0 to 3.6	–	18[2]	36	–	44	
t_{PHL}/t_{PLH}	Propagation delay ST_{CP} to Q_n	Figure 2	1.2	–	100	–	–	–	ns
			2.0	–	34	65	–	77	
			2.7	–	25	48	–	56	
			3.0 to 3.6	–	19[2]	38	–	45	
t_{PHL}	Propagation delay $\overline{MR}$ to Q_7'	Figure 5	1.2	–	85	–	–	–	ns
			2.0	–	29	56	–	66	
			2.7	–	21	41	–	49	
			3.0 to 3.6	–	16[2]	33	–	33	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	Figure 3	1.2	–	85	–	–	–	ns
			2.0	–	29	56	–	66	
			2.7	–	21	41	–	49	
			3.0 to 3.6	–	16[2]	33	–	39	
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	Figure 3	1.2	–	65	–	–	–	ns
			2.0	–	24	40	–	49	
			2.7	–	18	32	–	37	
			3.0 to 3.6	–	14[2]	26	–	30	

AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_W	Shift clock pulse width HIGH or LOW	Figure 1	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6[2]	–	24	–	
t_W	Storage clock pulse width HIGH or LOW	Figure 2	2.0	34	7	–	41	–	ns
			2.7	25	5	–	30	–	
			3.0 to 3.6	20	4[2]	–	24	–	
t_W	Master reset pulse width LOW	Figure 5	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6[2]	–	24	–	
t_{su}	Set-up time D_S to SH_{CP}	Figure 4	1.2	–	40	–	–	–	ns
			2.0	26	14	–	31	–	
			2.7	19	10	–	23	–	
			3.0 to 3.6	15	8[2]	–	18	–	
t_{su}	Set-up time SH_{CP} to ST_{CP}	Figure 2	1.2	–	40	–	–	–	ns
			2.0	26	14	–	31	–	
			2.7	19	10	–	23	–	
			3.0 to 3.6	15	8[2]	–	18	–	
t_h	Hold time D_S to SH_{CP}	Figure 4	1.2	–	–10	–	–	–	ns
			2.0	5	–4	–	5	–	
			2.7	5	–3	–	5	–	
			3.0 to 3.6	5	–2[2]	–	5	–	
t_{rem}	Removal time $\overline{MR}$ to SH_{CP}	Figure 5	1.2	–	–35	–	–	–	ns
			2.0	5	–12	–	5	–	
			2.7	5	–9	–	5	–	
			3.0 to 3.6	5	–7[2]	–	5	–	
f_{max}	Maximum clock pulse frequency SH_{CP} or ST_{CP}	Figure 1, 2	2.0	14	40	–	12	–	MHz
			2.7	19	58	–	16	–	
			3.0 to 3.6	24	70[2]	–	20	–	

NOTES:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25$°C.
2. Typical value measured at $V_{CC} = 3.3$V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5 * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V
$V_X = V_{OL}$ + 0.1V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH}$ – 0.1V_{CC} at V_{CC} < 2.7V

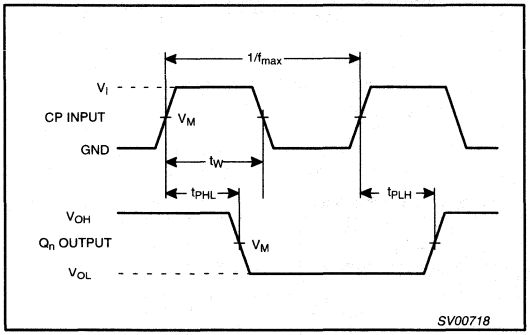


Figure 1. Clock (SH_{CP}) to output ($Q_{7'}$), propagation delays, the shift clock pulse width and the maximum shift clock frequency.

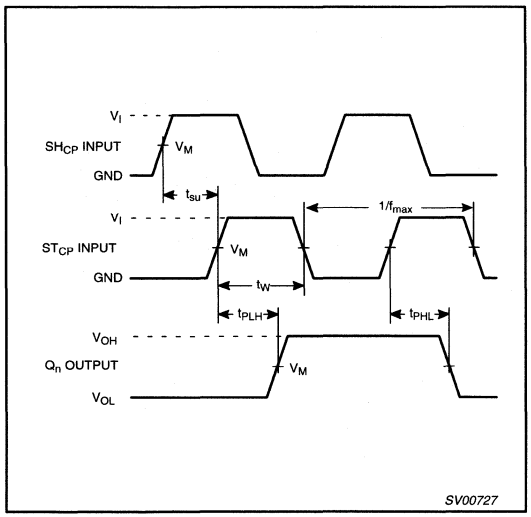


Figure 2. Storage clock (ST_{CP}) to output (Q_n) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.

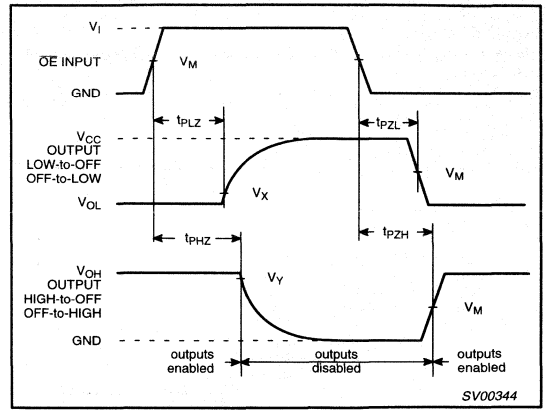


Figure 3. 3-State enable and disable times for input $\overline{OE}$.

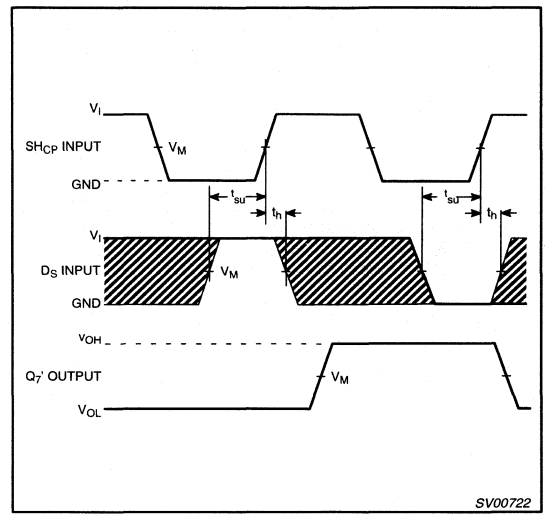


Figure 4. Data set-up and hold times for the data input (D_S).

AC WAVEFORMS (Continued)

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5 * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$
$V_X = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7V$
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$
$V_Y = V_{OH} - 0.1V_{CC}$ at $V_{CC} < 2.7V$

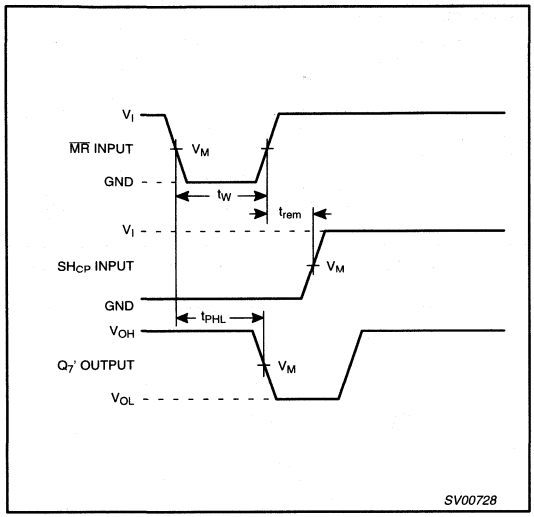
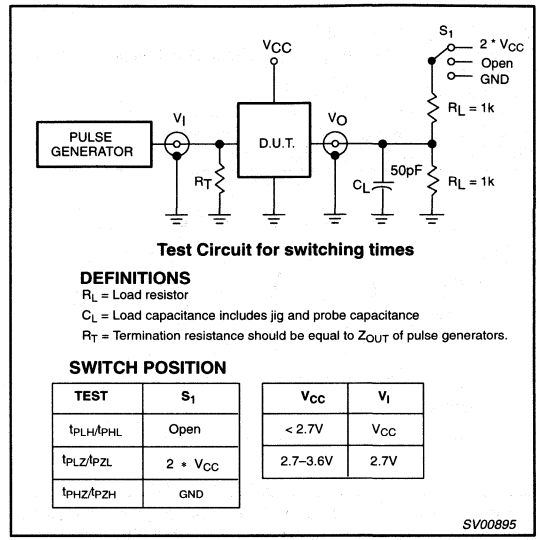


Figure 5. Master reset ($\overline{MR}$) pulse width, the master reset to output ($Q_{7'}$) propagation delay and the master reset to shift clock (SH_{CP}) removal time.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Figure 6. Load circuitry for switching times.

8-bit magnitude comparator | 74LV688

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for low voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V at V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V at V_{CC} = 3.3V, T_{amb} = 25°C
- Compare two 8-bit words
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV688 is a high-speed Si-gate CMOS device, pin compatible with the 74HC/HCT688

The 74LV688 is an 8-bit magnitude comparator. It performs comparisons of two 8-bit binary or BCD words. The output provides $\overline{P = Q}$ (equal-to).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay P_n, Q_n to $\overline{P=Q}$	C_L = 15pF V_{CC} = 3.3V	17	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	22	pF

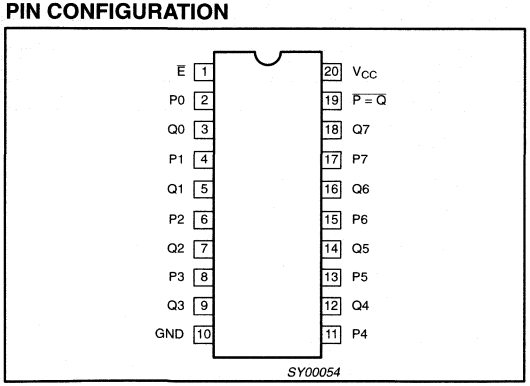
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	–40°C to +125°C	74LV688 N	74LV688 N	SOT146-1
20-Pin Plastic SO	–40°C to +125°C	74LV688 D	74LV688 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +125°C	74LV688 DB	74LV688 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV688 PW	74LV688PW DH	SOT360-1

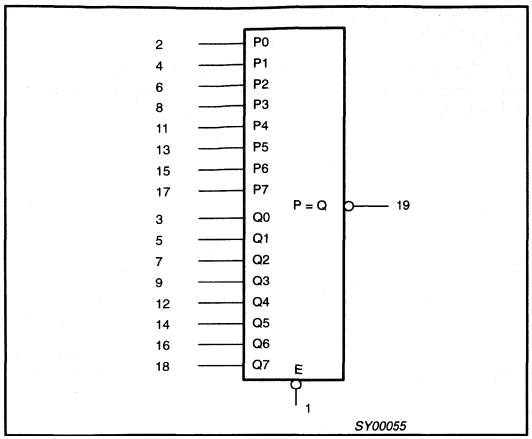
PIN CONFIGURATION



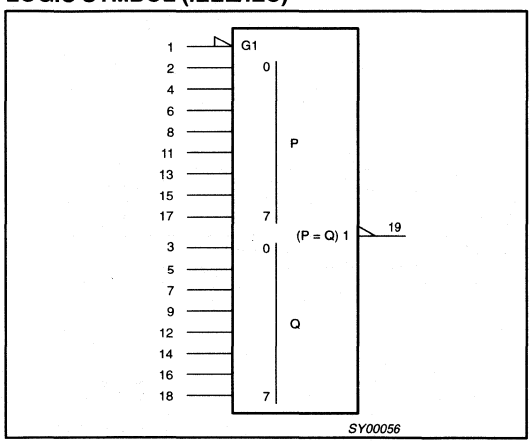
PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1	$\overline{E}$	Enable input (active LOW)
2, 4, 6, 8, 11, 13, 15, 17	P0 to P7	Word inputs
3, 5, 7, 9, 12, 14, 16, 18	Q0 to Q7	Word inputs
10	GND	Ground (0V)
19	$\overline{P=Q}$	Equal to output
20	V_{CC}	Positive Supply Voltage

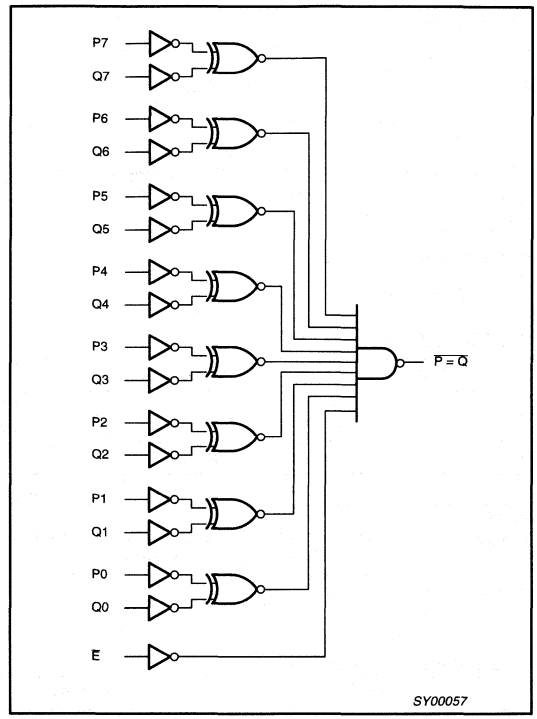
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
DATA Pn, Qn	ENABLE $\overline{E}$	$\overline{P = Q}$
P = Q	L	L
X	H	H
P > Q	L	H
P < Q	L	H

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage		−0.5	+7.0	V
I_{IK}	DC input diode current	$V_I < -0.5$ V or $V_1 > V_{CC} + 0.5$V	–	± 20	mA
I_{OK}	DC output diode current	$V_O < -0.5$ V or $V_0 > V_{CC} + 0.5$V	–	± 50	mA
I_O	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$		± 25	mA
± I_{GND}, ± I_{CC}	DC V_{CC} or GND current for types with – standard outputs			± 50	mA
T_{stg}	Storage temperature range		−65	+150	°C
P_{tot}	power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic medium-shrink SO (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 – – –	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The performance capability of a high–performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	see note 1	1.0	3.3	5.5	V
V_I	DC Input voltage		0	–	V_{CC}	V
V_O	DC output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free–air	See DC and AC characteristics	−40 −40	– –	+85 +125	°C
t_r, t_f ($\Delta t/\Delta v$)	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V		– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7 * V_{CC}			0.7 * V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3 * V_{CC}		0.3 * V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

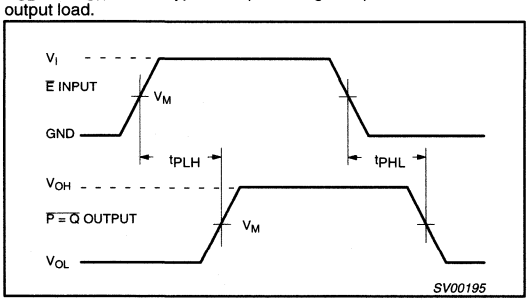
GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay P_n, Q_n to $\overline{P=Q}$	2	1.2		100	–		–	ns
			2.0		28	45		57	
			2.7		20	32		40	
			3.0 to 3.6		16[2]	26		33	
			4.5 to 5.5		11[2]	18		22	
t_{PHL}/t_{PLH}	Propagation delay $\overline{E}$ to $\overline{P=Q}$	1	1.2		50	–		–	ns
			2.0		17	29		38	
			2.7		13	21		27	
			3.0 to 3.6		10[2]	17		22	
			4.5 to 5.5		7[2]	12		15	

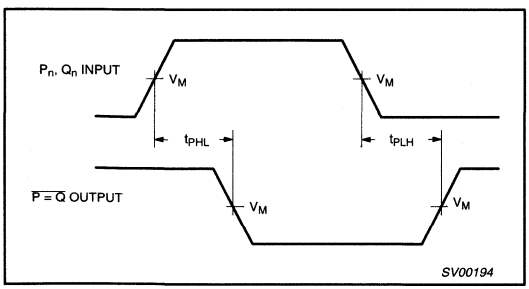
NOTES:
1. Unless otherwise stated, all typical values are at T_{amb} = 25°C.
2. Typical value measured at V_{CC} = 3.3V.
3. Typical value measured at V_{CC} = 5.0V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

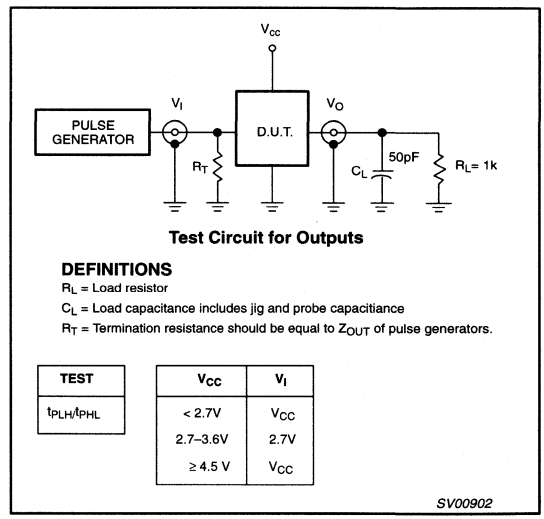


Waveform 1. Propagation delays from the enable input ($\overline{E}$) to the equal-to output ($\overline{P = Q}$).



Waveform 2. Propagation delays from the inputs (P_n, Q_n) to the equal-to output ($\overline{P = Q}$).

TEST CIRCUIT



Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitiance

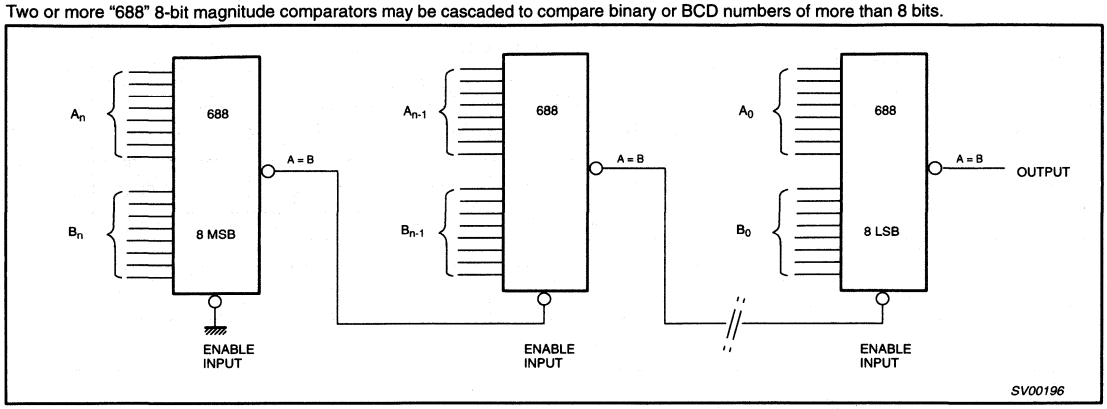
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V
	≥ 4.5 V	V_{CC}

Waveform 3. Load circuitry for switching times

APPLICATION INFORMATION

Two or more "688" 8-bit magnitude comparators may be cascaded to compare binary or BCD numbers of more than 8 bits.



Waveform 4. Binary or BCD comparator

14-stage binary ripple counter 74LV4020

FEATURES

- Optimized for Low Voltage applications: 1.0 to 5.5V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Frequency dividing circuits
- Time delay circuits
- Control counters
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4020 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT4020.

The 74LV4020 is a 14-stage binary ripple counter with a click input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q_0, Q_3 to Q_{13}). The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $\overline{CP}$ to Q_0 Q_n to Q_{n+1} MR to Q_n	C_L = 15pF V_{CC} = 3.3V	12 7 16	ns
f_{max}	Maximum clock frequency		100	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	20	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV4020 N	74LV4020 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV4020 D	74LV4020 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV4020 DB	74LV4020 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV4020 PW	74LV4020PW DH	SOT403-1

PIN CONFIGURATION

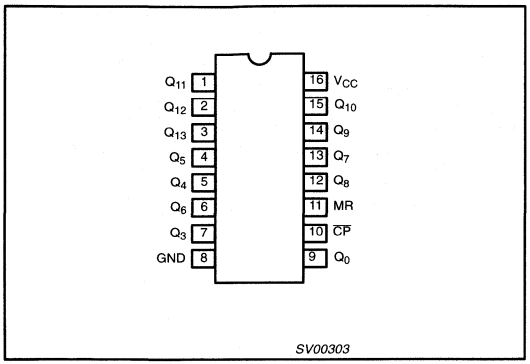


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	Q_0, Q_3 to Q_{13}	Parallel outputs
8	GND	Ground (0V)
10	$\overline{CP}$	Clock input (HIGH-to-LOW, edge-triggered)
11	MR	Master reset input (active HIGH)
16	V_{CC}	Positive supply voltage

LOGIC SYMBOL

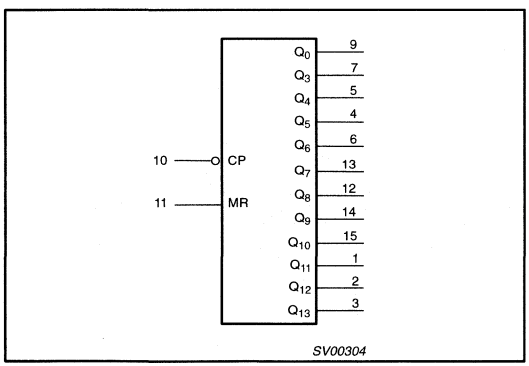


Figure 2. Logic symbol

LOGIC SYMBOL (IEEE/IEC)

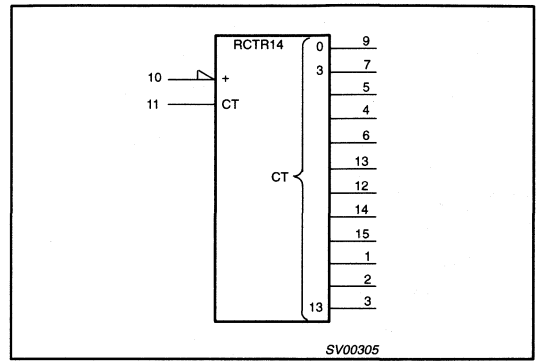


Figure 3. IEC Logic symbol

FUNCTIONAL DIAGRAM

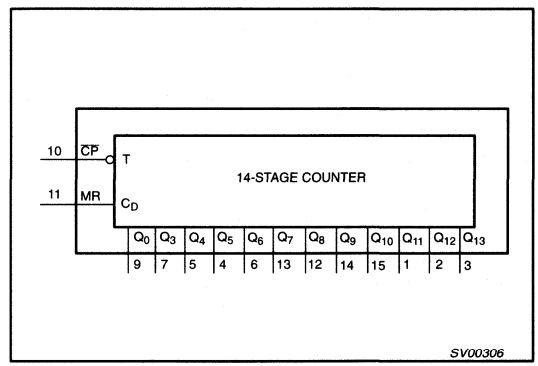


Figure 4. Functional diagram

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_0, Q_3 to Q_{13}
↑	L	no change
↓	L	count
X	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW -to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

LOGIC DIAGRAM

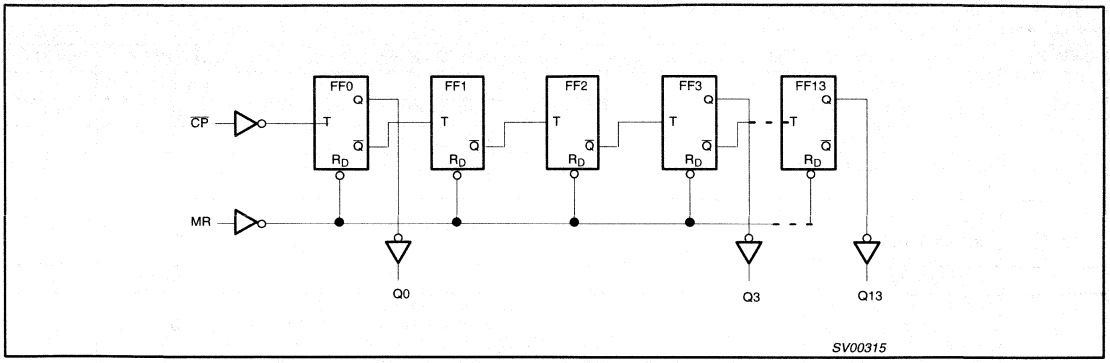


Figure 5. Logic diagram (one Schmitt-trigger)

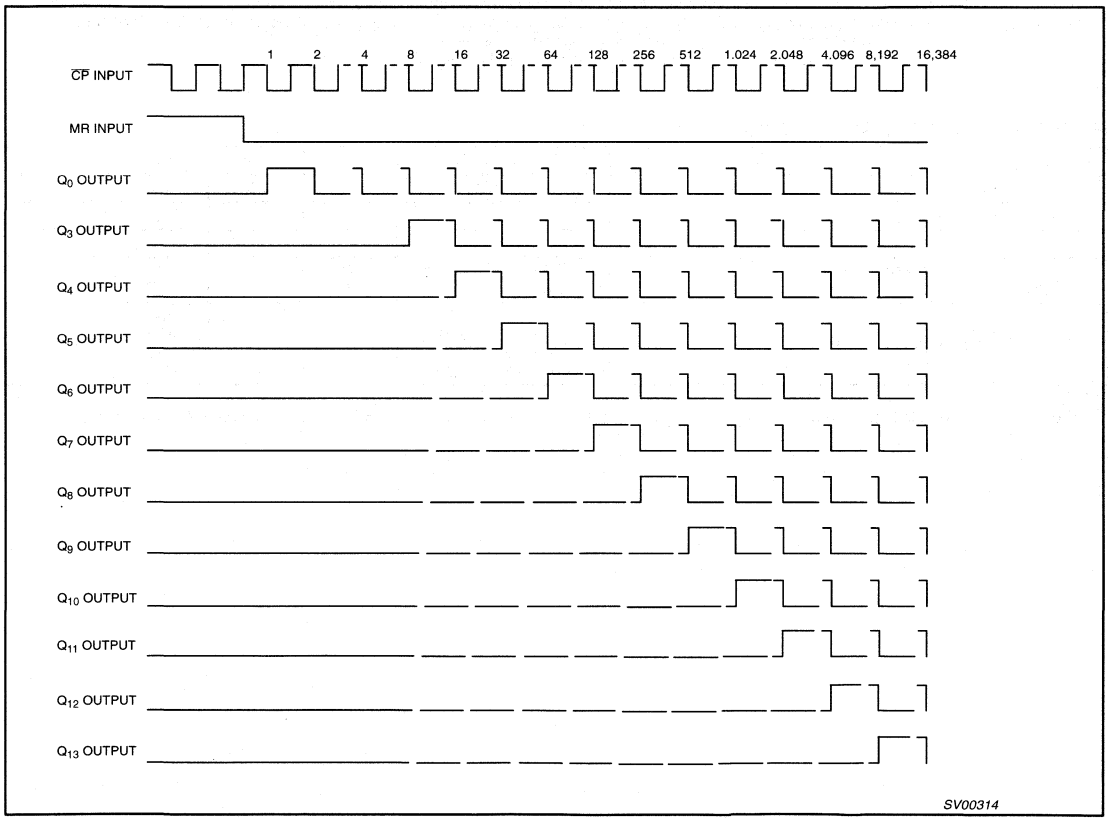


Figure 6. Timing diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 1kΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $\overline{CP}$ to Q_0	Figure 7, 9	1.2	–	60	–	–	–	ns
			2.0	–	27	43	–	54	
			2.7	–	19	31	–	38	
			3.0 to 3.6	–	16[2]	26	–	32	
			4.5 to 5.5	–	11[3]	17	–	22	
t_{PHL}/t_{PLH}	Propagation delay Q_n to Q_{n+1}	Figure 7, 9	1.2	–	40	–	–	–	ns
			2.0	–	18	29	–	37	
			2.7	–	13	21	–	26	
			3.0 to 3.6	–	11[2]	18	–	22	
			4.5 to 5.5	–	7[3]	12	–	15	
t_{PHL}	Propagation delay MR to Q_n	Figure 8, 9	1.2	–	55	–	–	–	ns
			2.0	–	27	44	–	55	
			2.7	–	19	31	–	39	
			3.0 to 3.6	–	16[2]	26	–	32	
			4.5 to 5.5	–	11[3]	17	–	22	
t_W	Clock pulse width HIGH to LOW	Figure 7	2.0	35	7	–	41	–	ns
			2.7	25	5	–	30	–	
			3.0 to 3.6	20	4[2]	–	24	–	
			4.5 to 5.5	15	3[3]	–	18	–	
t_W	Master reset pulse width HIGH	Figure 8	2.0	35	11	–	41	–	ns
			2.7	25	9	–	30	–	
			3.0 to 3.6	20	8[2]	–	24	–	
			4.5 to 5.5	15	7[3]	–	18	–	
t_{rem}	Removal time MR to $\overline{CP}$	Figure 8	1.2	–	10	–	–	–	ns
			2.0	22	5	–	26	–	
			2.7	16	4	–	19	–	
			3.0 to 3.6	13	3[2]	–	15	–	
			4.5 to 5.5	10	2[3]	–	12	–	
f_{max}	Maximum clock pulse frequency	Figure 7	2.0	14	60	–	12	–	MHz
			2.7	19	76	–	16	–	
			3.0 to 3.6	24	94[2]	–	20	–	
			4.5 to 5.5	36	112[3]	–	30	–	

NOTES:

1. Unless otherwise stated, all typical values are at T_{amb} = 25°C.
2. Typical value measured at V_{CC} = 3.3V.
3. Typical value measured at V_{CC} = 5.0V.

AC WAVEFORMS

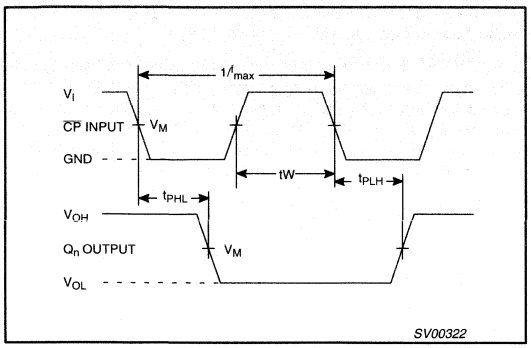


Figure 7.Clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency

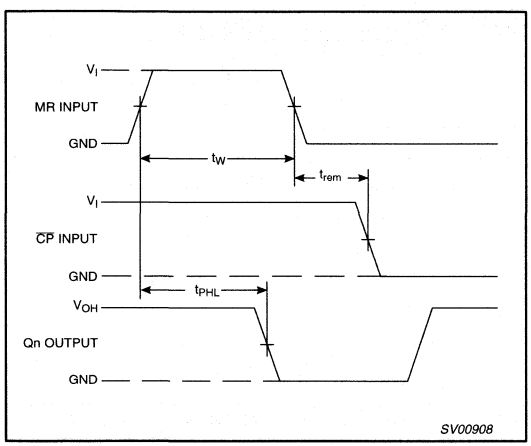
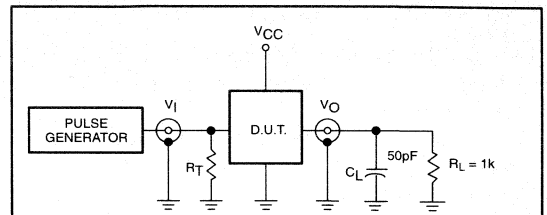


Figure 8. Master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V

SV00901

Figure 9.Load circuitry for switching times

12-stage binary ripple counter 74LV4040

FEATURES

- Optimized for Low Voltage applications: 1.0 to 5.5V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Typical V_{OLP} (output ground bounce) < 0.8V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2V @ V_{CC} = 3.3V, T_{amb} = 25°C
- Frequency dividing circuits
- Time delay circuits
- Control counters
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4040 is a low–voltage Si–gate CMOS device and is pin and function compatible with 74HC/HCT4040.

The 74LV4040 is a 12-stage binary ripple counter with a click input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q_0 to Q_{11}). The counter is advanced on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $\overline{CP}$ to Q_0 Q_n to Q_{n+1} MR to Q_n	C_L = 15pF V_{CC} = 3.3V	12 7 16	ns
f_{max}	Maximum clock frequency		100	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV4040 N	74LV4040 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV4040 D	74LV4040 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV4040 DB	74LV4040 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV4040 PW	74LV4040PW DH	SOT403-1

PIN CONFIGURATION

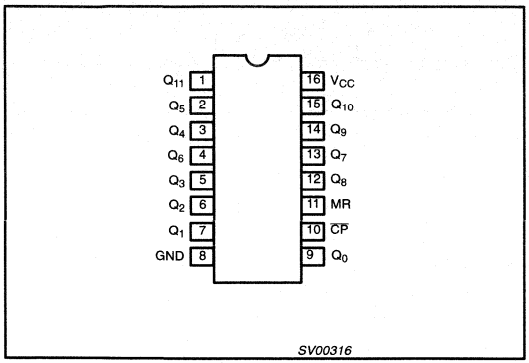


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q_0 to Q_{11}	Parallel outputs
8	GND	Ground (0V)
10	$\overline{CP}$	Clock input (HIGH-to-LOW, edge-triggered)
11	MR	Master reset input (active HIGH)
16	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)

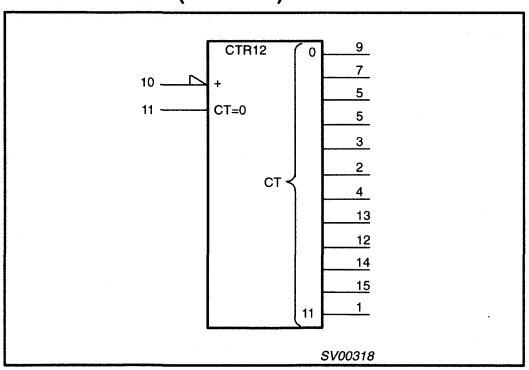


Figure 2. IEC Logic symbol

LOGIC SYMBOL

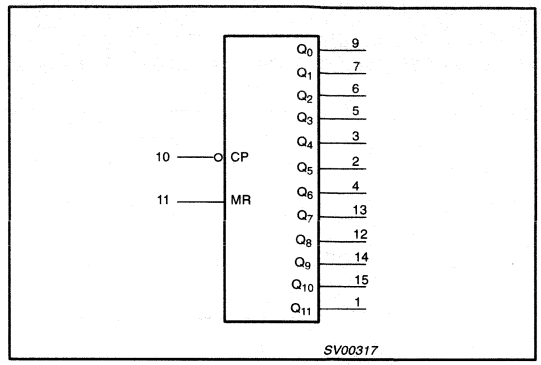


Figure 3. Logic symbol

FUNCTIONAL DIAGRAM

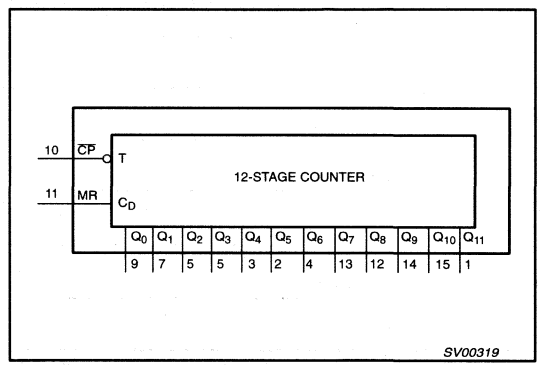


Figure 4. Functional diagram

LOGIC DIAGRAM

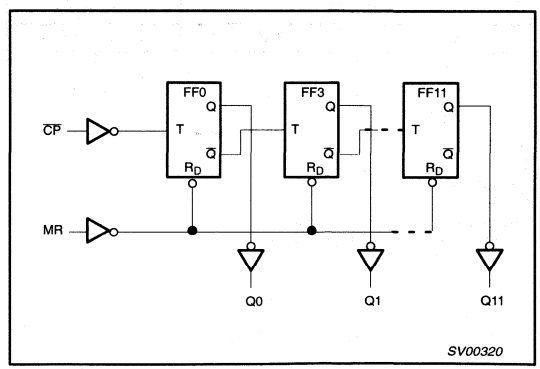


Figure 5. Logic diagram

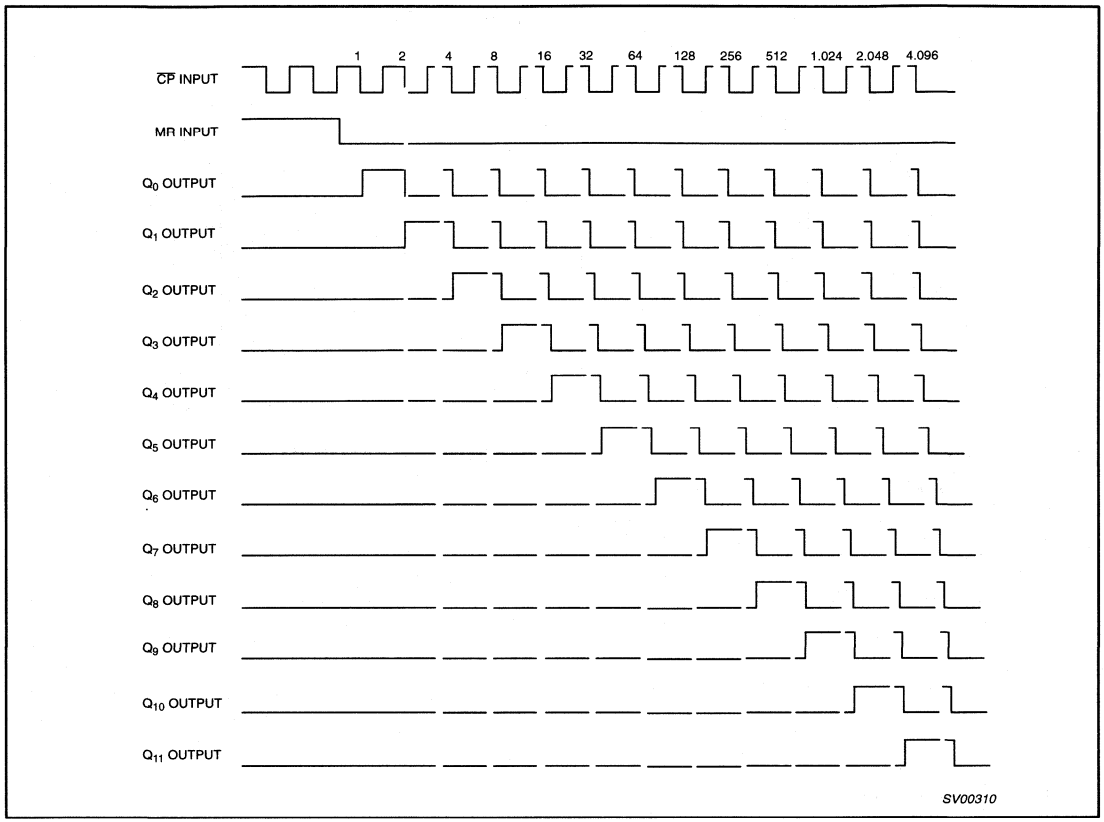


Figure 6. Timing diagram

FUNCTION TABLE

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↑	L	no change
↓	L	count
X	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW -to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

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$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	0.9			0.9		V
		V_{CC} = 2.0V	1.4			1.4		
		V_{CC} = 2.7 to 3.6V	2.0			2.0		
		V_{CC} = 4.5 to 5.5V	0.7*V_{CC}			0.7*V_{CC}		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			0.3		0.3	V
		V_{CC} = 2.0V			0.6		0.6	
		V_{CC} = 2.7 to 3.6V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			0.3*V_{CC}		0.3*V_{CC}	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $\overline{CP}$ to Q_0	Figure 7, 9	1.2	–	60	–	–	–	ns
			2.0	–	27	43	–	54	
			2.7	–	19	31	–	38	
			3.0 to 3.6	–	16[2]	26	–	32	
			4.5 to 5.5	–	1[3]	17	–	22	
t_{PHL}/t_{PLH}	Propagation delay Q_n to Q_{n+1}	Figure 7, 9	1.2	–	40	–	–	–	ns
			2.0	–	18	29	–	54	
			2.7	–	13	21	–	38	
			3.0 to 3.6	–	11[2]	18	–	32	
			4.5 to 5.5	–	7[3]	12	–	22	
t_{PHL}	Propagation delay MR to Q_n	Figure 8, 9	1.2	–	55	–	–	–	ns
			2.0	–	27	44	–	54	
			2.7	–	19	31	–	38	
			3.0 to 3.6	–	16[2]	26	–	32	
			4.5 to 5.5	–	11[3]	17	–	22	
t_W	Clock pulse width HIGH to LOW	Figure 7	2.0	35	7	–	41	54	ns
			2.7	25	5	–	30	–	
			3.0 to 3.6	20	4[2]	–	24	–	
			4.5 to 5.5	15	3[3]	–	18	–	
t_W	Master reset pulse width HIGH	Figure 8	2.0	35	11	–	41	–	ns
			2.7	25	9	–	30	–	
			3.0 to 3.6	20	8[2]	–	24	–	
			4.5 to 5.5	15	7[3]	–	18	–	
t_{rem}	Removal time MR to CP	Figure 8	1.2	–	10	–	–	–	ns
			2.0	22	5	–	26	–	
			2.7	16	4	–	19	–	
			3.0 to 3.6	13	3[2]	–	15	–	
			4.5 to 5.5	10	2[3]	–	12	–	
f_{max}	Maximum clock pulse frequency	Figure 7	2.0	14	60	–	12	–	MHz
			2.7	19	76	–	16	–	
			3.0 to 3.6	24	94[2]	–	20	–	
			4.5 to 5.5	36	112[3]	–	30	–	

NOTES:

1. Unless otherwise stated, all typical values are at $T_{amb} = 25°C$.
2. Typical value measured at $V_{CC} = 3.3$V.
3. Typical value measured at $V_{CC} = 5.0$V.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq 2.7V \leq 3.6V$
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V and ≥ 4.5V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

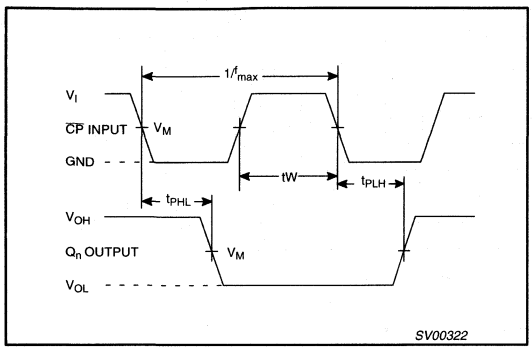


Figure 7. Clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency

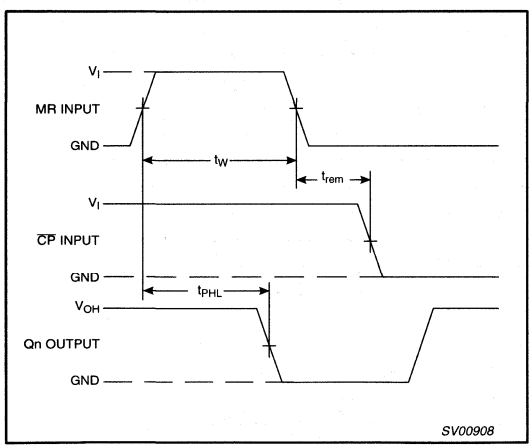


Figure 8. Master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time

TEST CIRCUIT

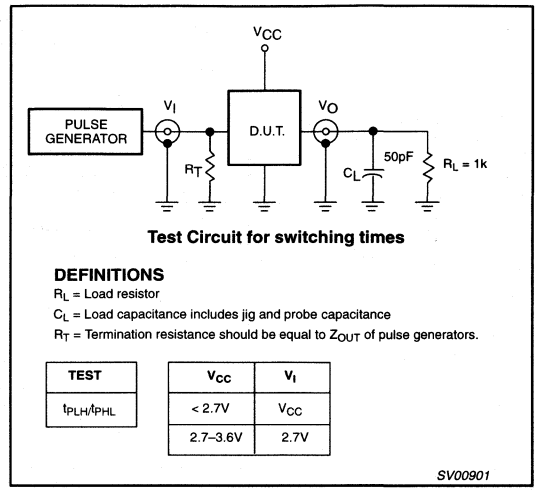


Figure 9.Load circuitry for switching times

8-channel analog multiplexer/demultiplexer 74LV4051

FEATURES

- Optimized for low voltage applications: 1.0 to 6.0 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Low typ "ON" resistance:
  60 Ω at $V_{cc} - V_{EE}$ = 4.5 V
  90 Ω at $V_{cc} - V_{EE}$ = 3.0 V
  145 Ω at $V_{cc} - V_{EE}$ = 2.0 V
- Logic level translation: to enable 3 V logic to communicate with ± 3 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4051 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4051.

The 74LV4051 is an 8-channel analog multiplexer/demultiplexer with three digital select inputs (S_0 to S_2) an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by S_0 to S_2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 to S_2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 to S_2, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0 V. The analog inputs/outputs (Y_0 to Y_7 and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} - V_{EE} may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq$ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn "ON" time $\overline{E}$ to V_{OS} S_n to V_{OS}	C_L = 15 pF R_L = 1KΩ V_{CC} = 3.3 V	 23 22	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time $\overline{E}$ to V_{OS} S_n to V_{OS}		 25 20	
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	See Notes 1 and 2	25	
C_S	Maximum switch capacitance independent (Y) common (Z)		5 25	

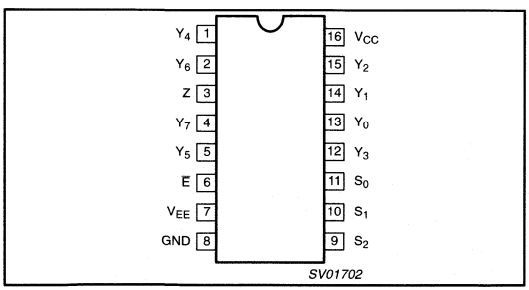
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = maximum switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	Code
16-Pin Plastic DIL	–40°C to +125°C	74LV4051 N	74LV4051 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV4051 D	74LV4051 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV4051 DB	74LV4051 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV4051 PW	74LV4051PW DH	SOT403-1

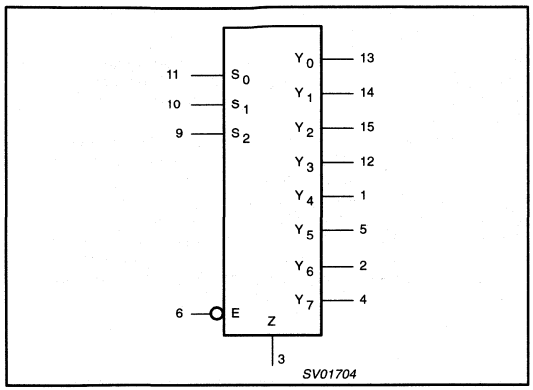
PIN CONFIGURATION



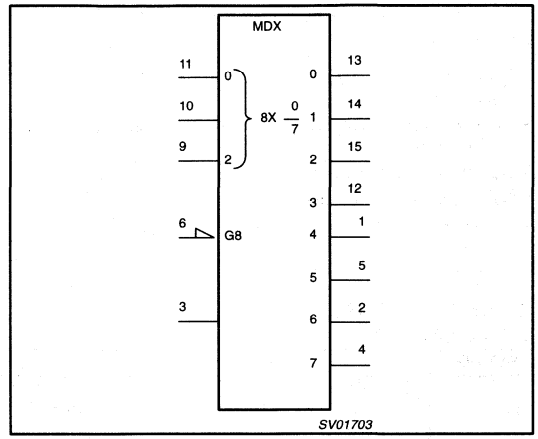
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
3	Z	Common input/output
6	$\overline{E}$	Enable input (active LOW)
7	V_{FF}	Negative supply voltage
8	GND	Ground (0 V)
11, 10, 9	S_0 to S_2	Select inputs
13, 14, 15, 12, 1, 5, 2, 4	Y_0 to Y_7	Independent inputs/outputs
16	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

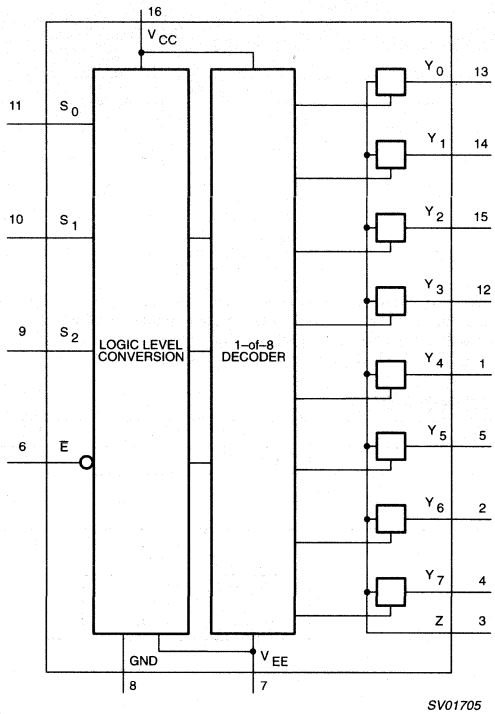


FUNCTION TABLE

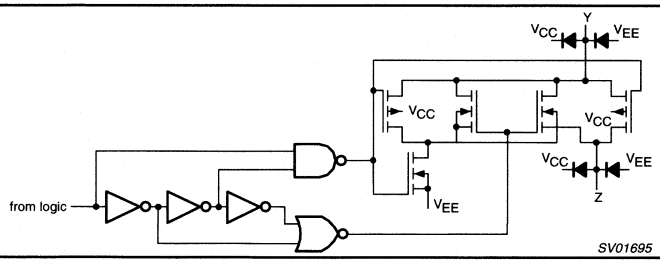
INPUTS			INPUTS	CHANNEL ON
$\overline{E}$	S_2	S_1	S_0	
L	L	L	L	$Y_0 - Z$
L	L	L	H	$Y_1 - Z$
L	L	H	L	$Y_2 - Z$
L	L	H	H	$Y_3 - Z$
L	H	L	L	$Y_4 - Z$
L	H	L	H	$Y_5 - Z$
L	H	H	L	$Y_6 - Z$
L	H	H	H	$Y_7 - Z$
H	X	X	X	None

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM (ONE SWITCH)



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V	20	mA
$\pm I_{SK}$	DC switch diode current	$V_S < -0.5$ or $V_S > V_{CC} + 0.5$ V	20	mA
$\pm I_S$	DC switch current	-0.5 V $< V_S < V_{CC} + 0.5$ V	25	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1 and Figure 5	1.0	3.3	6.0	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 6.0 V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 6.0V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				-40°C to +85°C			-40°C to +125°C		
				MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V		0.9			0.9		V
		V_{CC} = 2.0 V		1.4			1.4		
		V_{CC} = 2.7 to 3.6 V		2.0			2.0		
		V_{CC} = 4.5 V		3.15			3.15		
		V_{CC} = 6.0 V		4.20			4.20		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V				0.3		0.3	V
		V_{CC} = 2.0 V				0.6		0.6	
		V_{CC} = 2.7 to 3.6 V				0.8		0.8	
		V_{CC} = 4.5 V				1.35		1.35	
		V_{CC} = 6.0 V				1.80		1.80	
$\pm I_I$	Input leakage current	V_{CC} = 3.6	V_I = V_{CC} or GND			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
$\pm I_S$	Analog switch OFF-state current per channel	V_{CC} = 3.6	V_I = V_{IH} or V_{IL}; $\lvert V_S \rvert$ = V_{CC} - GND (See Figure 2)			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
$\pm I_S$	Analog switch ON-state current	V_{CC} = 3.6	V_I = V_{IH} or V_{IL}; $\lvert V_S \rvert$ = V_{CC} - GND (See Figure 3)			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
I_{CC}	Quiescent supply current	V_{CC} = 3.6 V	V_I = V_{CC} or GND; V_{IS} = GND or V_{CC}; V_{OS} = V_{CC} or GND			20.0		40	µA
		V_{CC} = 6.0 V				40.0		80	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 to 3.6 V	V_I = V_{CC} – 0.6 V			500		850	µA
R_{ON}	ON-resistance (peak)	V_{CC} = 1.2 V	V_I = V_{IH} or V_{IL}; I_S = 100 µA; V_{IS} = V_{CC} to GND						Ω
		V_{CC} = 2.0 V	V_I = V_{IH} or V_{IL}; I_S = 1000 µA; V_{IS} = V_{CC} to GND		145	325		375	
		V_{CC} = 2.7 V			90	200		235	
		V_{CC} = 3.0 to 3.6 V			80	180		210	
		V_{CC} = 4.5 V			60	135		160	
		V_{CC} = 6.0 V			55	125		145	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V	V_I = V_{IH} or V_{IL}; I_S = 100 µA; V_{IS} = GND		225				Ω
		V_{CC} = 2.0 V	V_I = V_{IH} or V_{IL}; I_S = 1000 µA; V_{IS} = GND		110	235		270	
		V_{CC} = 2.7 V			70	145		165	
		V_{CC} = 3.0 to 3.6 V			60	130		150	
		V_{CC} = 4.5 V			45	100		115	
		V_{CC} = 6.0 V			40	85		100	

NOTES:

1. All typical values are measured at T_{amb} = 25°C.
2. At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
3. R_{ON} (MAX) data is preliminary.

DC ELECTRICAL CHARACTERISTICS (*Continued*)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				-40°C to +85°C			-40°C to +125°C		
				MIN	TYP[1]	MAX	MIN	MAX	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V	$V_I = V_{IH}$ or V_{IL}; I_S = 100 μA; $V_{IS} = V_{CC}$		250				Ω
		V_{CC} = 2.0 V	$V_I = V_{IH}$ or V_{IL}; I_S = 1000 μA; $V_{IS} = V_{CC}$		120	320		370	Ω
		V_{CC} = 2.7 V			75	195		225	
		V_{CC} = 3.0 to 3.6 V			70	175		205	
		V_{CC} = 4.5 V			50	130		150	
		V_{CC} = 6.0 V			45	120		135	
ΔR_{ON}	Maximum variation of ON-resistance between any two channels	V_{CC} = 1.2 V	$V_I = V_{IH}$ or V_{IL}; $V_{IS} = V_{CC}$ to GND						Ω
		V_{CC} = 2.0 V			5				
		V_{CC} = 2.7 V			4				
		V_{CC} = 3.0 to 3.6 V			4				
		V_{CC} = 4.5 V			3				
		V_{CC} = 6.0 V			2				

NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
3. R_{ON} (MAX) data is preliminary.

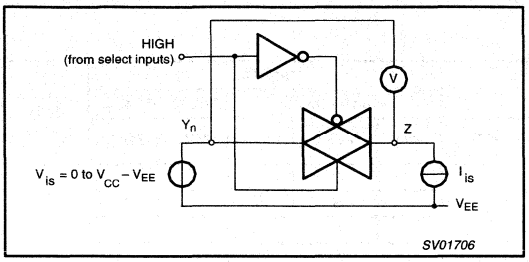


Figure 1. Test circuit for measuring ON-resistance (R_{ON}).

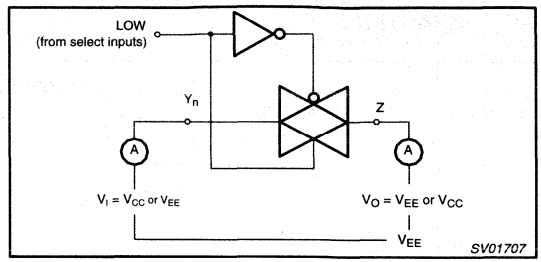


Figure 2. Test circuit for measuring OFF-state current.

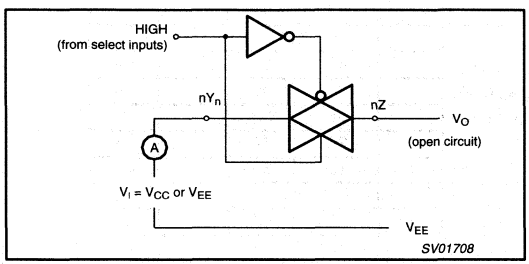


Figure 3. Test circuit for measuring ON-state current.

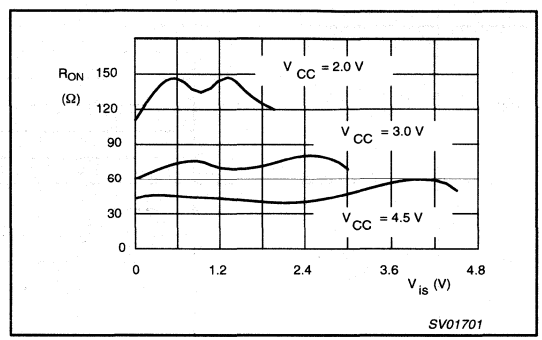


Figure 4. Typical ON-resistance (R_{on}) as a function of input voltage (V_{is}) for V_{is} = 0 to $V_{CC} - V_{EE}$.

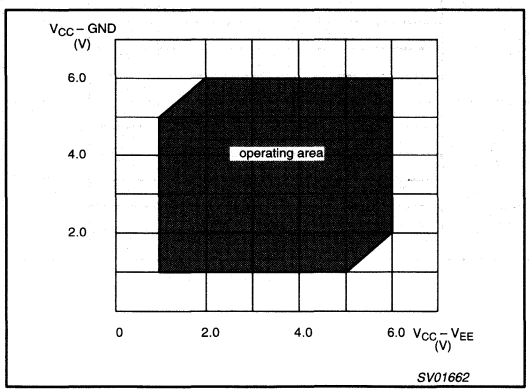


Figure 5. Guaranteed operating area as a function of the supply voltages.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF

SYMBOL	PARAMETER	CONDITION		LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
		V_{CC} (V)	OTHER	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay V_{is} to V_{os}	1.2	$R_L = \infty$; $C_L = 50$ pF Figure 12		25				ns
		2.0			9	17		20	
		2.7			6	13		15	
		3.0 to 3.6			5[2]	10		12	
		4.5			4	9		10	
		6.0			3	8		8	
t_{PZH}/t_{PZL}	Turn-on time $\overline{E}$ to V_{OS}	1.2	$R_L = 1k\Omega$; $C_L = 50$ pF Figures 13 and 1		145				ns
		2.0			49	94		112	
		2.7			36	69		83	
		3.0 to 3.6			28[2]	55		66	
		4.5			25	47		56	
		6.0			19	38		43	
t_{PZH}/t_{PZL}	Turn-on time S_n to V_{OS}	1.2	$R_L = 1k\Omega$; $C_L = 50$ pF Figures 13 and 1		140				ns
		2.0			48	90		107	
		2.7			35	66		79	
		3.0 to 3.6			27[2]	53		63	
		4.5			24	45		54	
		6.0			18	34		41	
t_{PHZ}/t_{PLZ}	Turn-off time $\overline{E}$ to V_{OS}	1.2	$R_L = 1k\Omega$ $C_L = 50$ pF Figures 13 and 1		145				ns
		2.0			51	93		110	
		2.7			38	69		82	
		3.0 to 3.6			30[2]	56		66	
		4.5			29	48		56	
		6.0			21	37		44	
t_{PHZ}/t_{PLZ}	Turn-off time S_n to V_{OS}	1.2	$R_L = 1k\Omega$ $C_L = 50$ pF Figures 13 and 1		115				ns
		2.0			41	73		90	
		2.7			31	54		67	
		3.0 to 3.6			24[2]	44		54	
		4.5			22	37		46	
		6.0			17	29		36	

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

ADDITIONAL AC CHARACTERISTICS

Recommended conditions and typical values
GND = 0 V; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	Sine-wave distortion f = 1 kHz	0.80 0.40	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pf Figure 9 and 10
	Sine-wave distortion f = 10 kHz	2.40 1.20	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pf Figure 9 and 10
	Switch "OFF" signal feed through	–50 –50	dB	3.0 6.0	Note 1	R_L = 600 Ω; C_L = 50 pf; f= 1 MHz Figures 5 and 11
	Crosstalk between any two switches/multiplexers	–60 –60	dB	3.0 6.0	Note 1	R_L = 600 Ω; C_L = 50 pf; f= 1 MHz Figure 8
$V_{(p-p)}$	Crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 120	mV	3.0 6.0		R_L = 600 Ω; C_L = 50 pf; f= 1 MHz (S_n or $\overline{E}$, square wave between V_{CC} and GND $t_r = t_f$ = 6 ns) Figure 8
f_{max}	Minimum frequency response (–3 dB)	180 200	MHz	3.0 6.0	Note 2	R_L = 50 Ω; C_L = 50 pF Figures 5, 8 and 9
C_S	Maximum switch capacitance	5	pf			

GENERAL NOTES:

V_{is} is the input voltage at nY or Z terminal, whichever is assigned as an input.
V_{OS} is the output voltage at nY or Z terminal, whichever is assigned as an output.

NOTES:

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

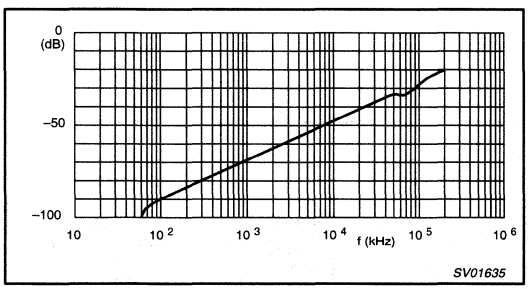


Figure 6. Typical switch "OFF" signal feed-through as a function of frequency.

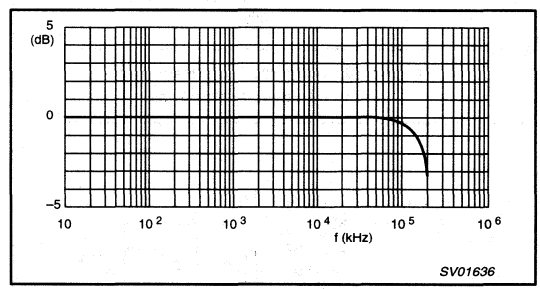


Figure 7. Typical frequency response.

NOTES TO FIGURES 6 AND 7:

Test conditions: V_{CC} = 3.0 V; GND = 0 V; V_{EE} = -3.0 V; R_L = 50 Ω; R_{SOURCE} = 1kΩ.

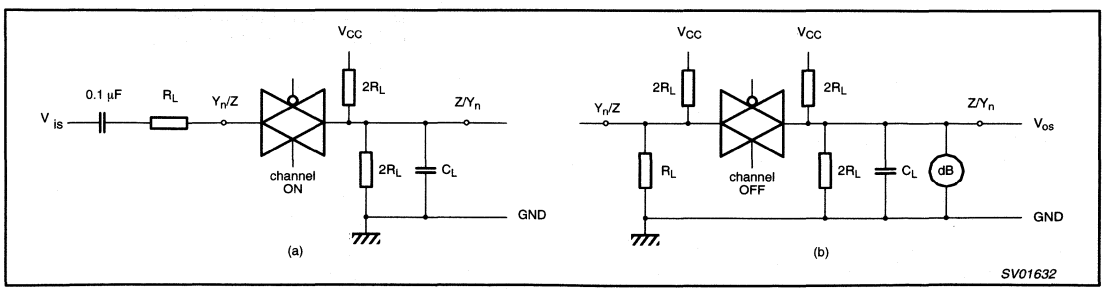


Figure 8. Test circuit for measuring crosstalk between any two switches. (a) channel ON condition; (b) channel OFF condition.

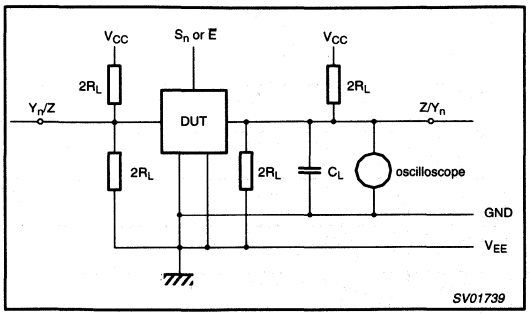
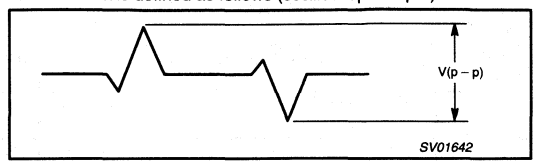


Figure 9. Test circuit for measuring crosstalk between control and any switch.

NOTE TO FIGURE 8:
The crosstalk is defined as follows (oscilloscope output):



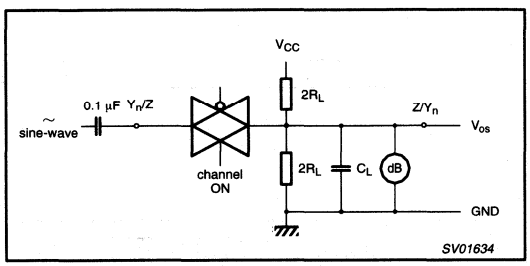


Figure 10. Test circuit for measuring minimum frequency response.

NOTE TO FIGURE 9:
Adjust input voltage to obtain 0 dBm at V_{OS} when F_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of –3 dB at V_{OS}.

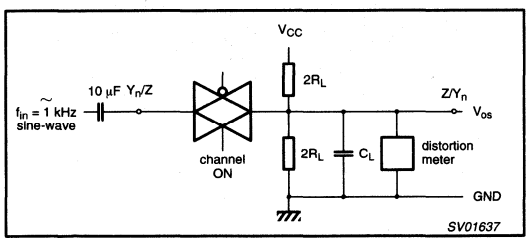


Figure 11. Test circuit for measuring sine-wave distortion.

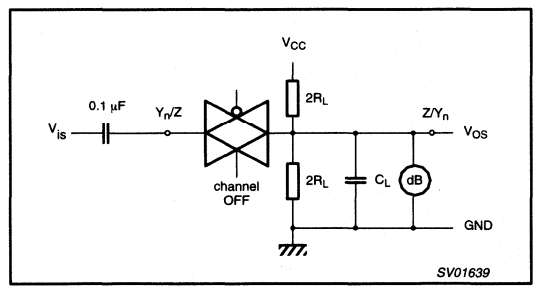


Figure 12. Test circuit for measuring switch "OFF" signal feed-through.

WAVEFORMS

V_M = 1.5 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_M = 0.5 × V_{CC} at 2.7 V > V_{CC} > 3.6 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
V_x = V_{OL} + 0.3 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_x = V_{OL} + 0.1 × V_{CC} at 2.7 V > V_{CC} > 3.6 V
V_Y = V_{OH} − 0.3 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_Y = V_{OH} − 0.1 × V_{CC} at 2.7 V > V_{CC} > 3.6 V

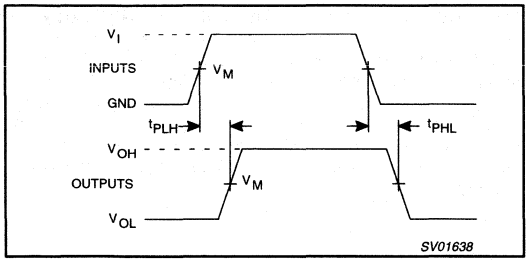


Figure 13. Input (V_{is}) to output (V_{os}) propagation delays.

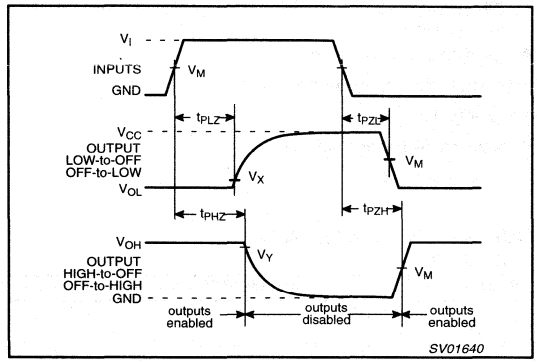
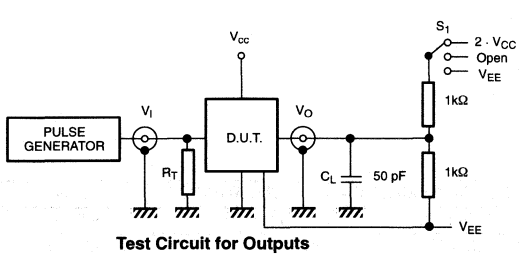
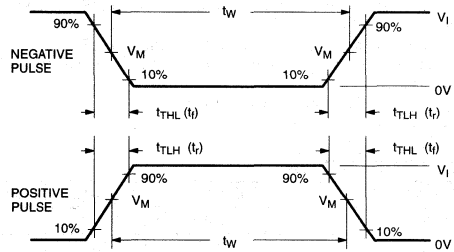


Figure 14. Turn-on and turn-off times for the inputs (S_n, $\overline{E}$) to the output (V_{os}).

TEST CIRCUIT



Test Circuit for Outputs



V_{CC}	V_I
< 2.7V	V_{CC}
2.7 - 3.6V	2.7V
> 3.6 V	V_{CC}

Test	S_1	V_{IS}
t_{PLH}/t_{PHL}	Open	Pulse
t_{PLZ}/t_{PZL}	2 · V_{CC}	V_{EE}
t_{PHZ}/t_{PZH}	V_{EE}	V_I

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

t_r = t_f =6ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

SY01738

Figure 15. Load circuitry for switching times.

Dual 4-channel analog multiplexer/demultiplexer — 74LV4052

FEATURES

- Optimized for low voltage applications: 1.0 to 6.0 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Low typ "ON" resistance:
  60 Ω at $V_{cc} - V_{EE}$ = 4.5 V
  90 Ω at $V_{cc} - V_{EE}$ = 3.0 V
  145 Ω at $V_{cc} - V_{EE}$ = 2.0 V
- Logic level translation: to enable 3 V logic to communicate with ± 3 V analog signals
- Typical "break before make" built in
- Analog/Digital multiplexing and demultiplexing
- Signal gating
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4052 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4052.

The 74LV4052 is a dual 4-channel analog multiplexer/demultiplexer with a common select logic. Each multiplexer has four independent inputs/outputs (nY_0 to nY_3) and a common input/output (nZ). The common channel select logics include two digital select inputs (S_0 and S_1) and an active LOW enable input ($\overline{E}$).

With $\overline{E}$ LOW, one of the four switches is selected (low impedance ON-state) by S_0 and S_1. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 and S_1. V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0, S_1 and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0 V. The analog inputs/outputs (nY_0, to nY_3, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} - V_{EE} may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn "ON" time $\overline{E}$ or V_{OS} S_n	C_L = 15 pF, R_L = 1KΩ, V_{CC} = 3.3 V	30	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time $\overline{E}$ or V_{OS} S_n		22	
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	See Notes 1 and 2	57	
C_S	Maximum switch capacitance independent (Y) common (Z)		5 12	

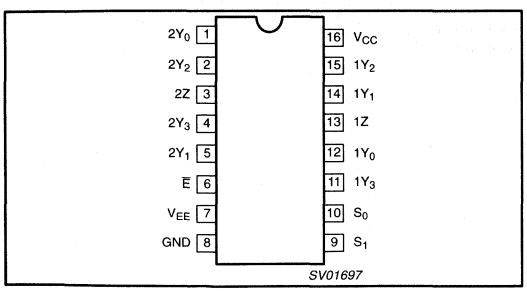
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = maximum switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	Code
16-Pin Plastic DIL	–40°C to +125°C	74LV4052 N	74LV4052 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV4052 D	74LV4052 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV4052 DB	74LV4052 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV4052 PW	74LV4052PW DH	SOT403-1

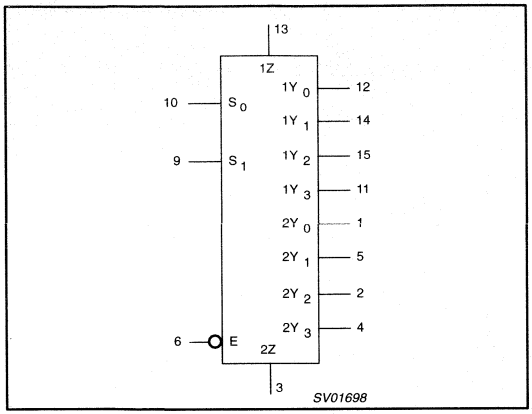
PIN CONFIGURATION



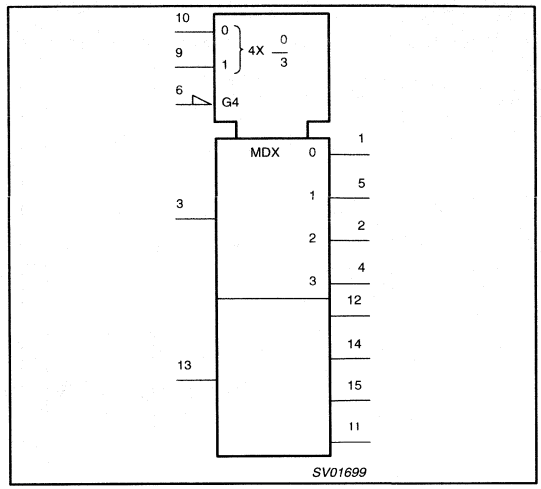
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 5, 2, 4	$2Y_0$, $2Y_3$	Independent inputs/outputs
6	$\overline{E}$	Enable input (active LOW)
7	V_{EE}	Negative supply voltage
8	GND	Ground (0 V)
10, 9	S_0, S_1	Select inputs
12, 14, 15, 11	$1Y_0$ to $1Y_3$	Independent inputs/outputs
13, 3	1Z, 2Z	Common inputs/outputs
16	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

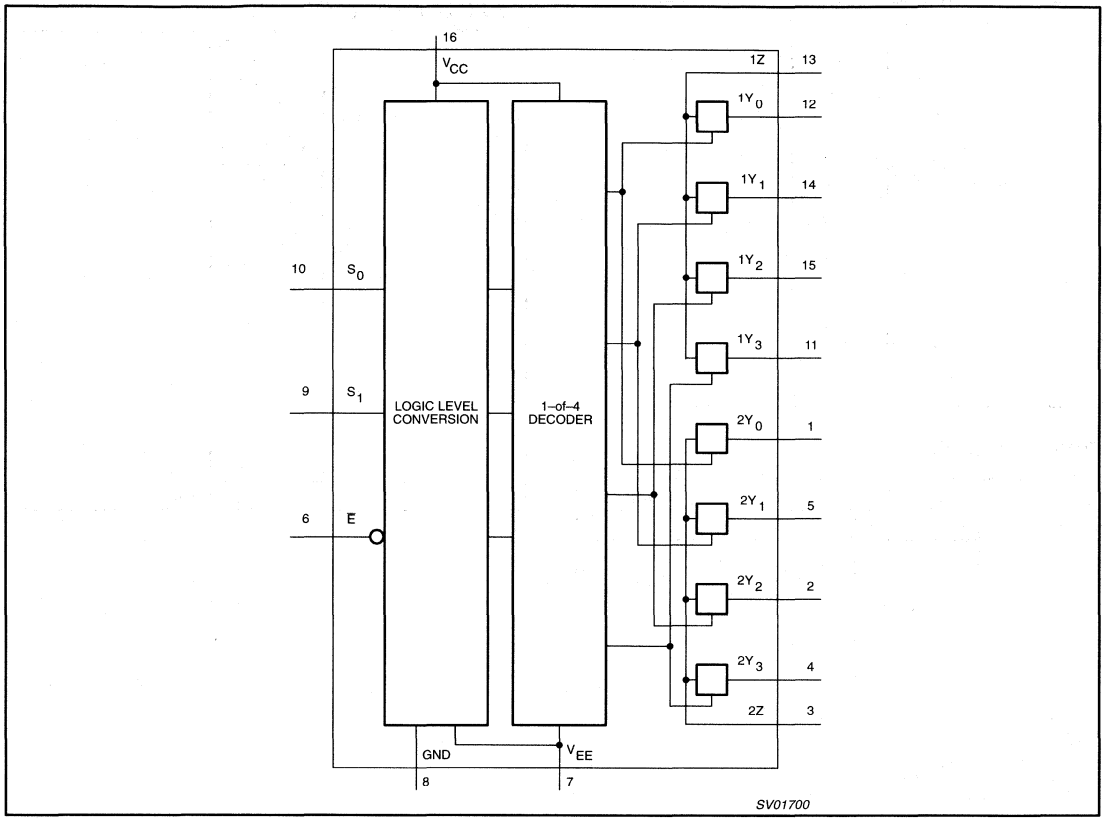


FUNCTION TABLE

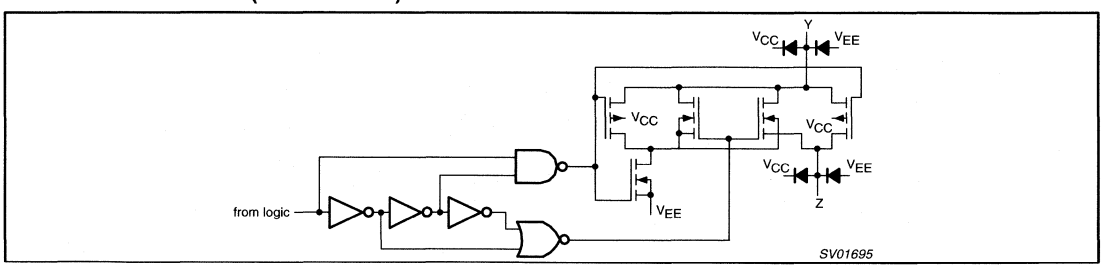
INPUTS			CHANNEL ON
$\overline{E}$	S_1	S_0	
L	L	L	$nY_0 - nZ$
L	L	H	$nY_1 - nZ$
L	H	L	$nY_2 - nZ$
L	H	H	$nY_3 - nZ$
H	X	X	None

NOTES:
1. H = HIGH voltage level
2. L = LOW voltage level
3. X = don't care

FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM (ONE SWITCH)



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V	20	mA
$\pm I_{SK}$	DC switch diode current	$V_S < -0.5$ or $V_S > V_{CC} + 0.5$ V	20	mA
$\pm I_S$	DC switch current	-0.5 V $< V_S < V_{CC} + 0.5$ V	25	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1 and Figure 5	1.0	3.3	6.0	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 6.0 V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 6.0 V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				-40°C to +85°C			-40°C to +125°C		
				MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V		0.9			0.9		V
		V_{CC} = 2.0 V		1.4			1.4		
		V_{CC} = 2.7 to 3.6 V		2.0			2.0		
		V_{CC} = 4.5 V		3.15			3.15		
		V_{CC} = 6.0 V		4.20			4.20		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V				0.3		0.3	V
		V_{CC} = 2.0 V				0.6		0.6	
		V_{CC} = 2.7 to 3.6 V				0.8		0.8	
		V_{CC} = 4.5 V				1.35		1.35	
		V_{CC} = 6.0 V				1.80		1.80	
$\pm I_I$	Input leakage current	V_{CC} = 3.6	V_I = V_{CC} or GND			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
$\pm I_S$	Analog switch OFF-state current per channel	V_{CC} = 3.6	V_I = V_{IH} or V_{IL}; $\lvert V_S \rvert$ = V_{CC} - GND (See Figure 2)			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
$\pm I_S$	Analog switch ON-state current	V_{CC} = 3.6	V_I = V_{IH} or V_{IL}; $\lvert V_S \rvert$ = V_{CC} - GND (See Figure 3)			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
I_{CC}	Quiescent supply current	V_{CC} = 3.6 V	V_I = V_{CC} or GND; V_{IS} = GND or V_{CC}; V_{OS} = V_{CC} or GND			20.0		40	µA
		V_{CC} = 6.0 V				40.0		80	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 to 3.6 V	V_I = V_{CC} – 0.6 V			500		850	µA
R_{ON}	ON-resistance (peak)	V_{CC} = 1.2 V	V_I = V_{IH} or V_{IL}; I_S = 100 µA; V_{IS} = V_{CC} to GND						Ω
		V_{CC} = 2.0 V	V_I = V_{IH} or V_{IL}; I_S = 1000 µA; V_{IS} = V_{CC} to GND		145	325		375	
		V_{CC} = 2.7 V			90	200		235	
		V_{CC} = 3.0 to 3.6 V			80	180		210	
		V_{CC} = 4.5 V			60	135		160	
		V_{CC} = 6.0 V			55	125		145	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V	V_I = V_{IH} or V_{IL}; I_S = 100 µA; V_{IS} = GND		225				Ω
		V_{CC} = 2.0 V	V_I = V_{IH} or V_{IL}; I_S = 1000 µA; V_{IS} = GND		110	235		270	
		V_{CC} = 2.7 V			70	145		165	
		V_{CC} = 3.0 to 3.6 V			60	130		150	
		V_{CC} = 4.5 V			45	100		115	
		V_{CC} = 6.0 V			40	85		100	

NOTES:

1. All typical values are measured at T_{amb} = 25°C.
2. At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
3. R_{ON} (MAX) data is preliminary.

DC ELECTRICAL CHARACTERISTICS (*Continued*)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				-40°C to +85°C			-40°C to +125°C		
				MIN	TYP[1]	MAX	MIN	MAX	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V	$V_I = V_{IH}$ or V_{IL}; I_S = 100 μA; $V_{IS} = V_{CC}$		250				Ω
		V_{CC} = 2.0 V	$V_I = V_{IH}$ or V_{IL}; I_S = 1000 μA; $V_{IS} = V_{CC}$		120	320		370	Ω
		V_{CC} = 2.7 V			75	195		225	
		V_{CC} = 3.0 to 3.6 V			70	175		205	
		V_{CC} = 4.5 V			50	130		150	
		V_{CC} = 6.0 V			45	120		135	
ΔR_{ON}	Maximum variation of ON-resistance between any two channels	V_{CC} = 1.2 V	$V_I = V_{IH}$ or V_{IL}; $V_{IS} = V_{CC}$ to GND						Ω
		V_{CC} = 2.0 V			5				
		V_{CC} = 2.7 V			4				
		V_{CC} = 3.0 to 3.6 V			4				
		V_{CC} = 4.5 V			3				
		V_{CC} = 6.0 V			2				

NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
3. R_{ON} (MAX) data is preliminary.

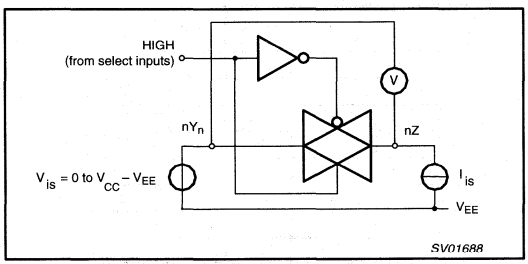


Figure 1. Test circuit for measuring ON-resistance (R_{ON}).

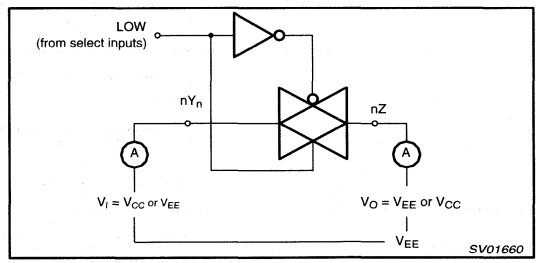


Figure 2. Test circuit for measuring OFF-state current.

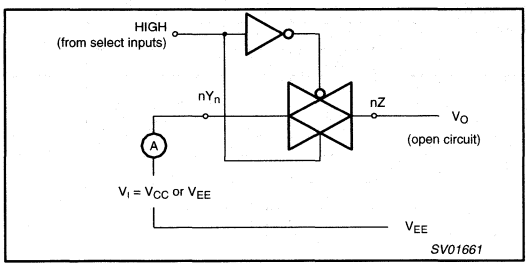


Figure 3. Test circuit for measuring ON-state current.

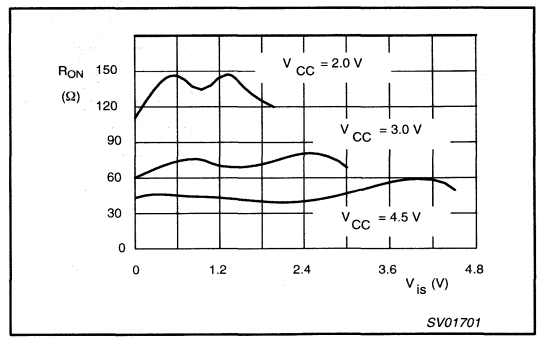


Figure 4. Typical ON-resistance (R_{on}) as a function of input voltage (V_{is}) for V_{is} = 0 to $V_{CC} - V_{EE}$.

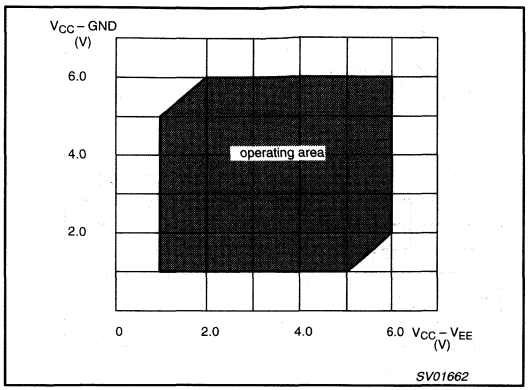


Figure 5. Guaranteed operating area as a function of the supply voltages.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	CONDITION		LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
		V_{CC} (V)	OTHER	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay V_{is} to V_{os}	1.2	$R_L = \infty$; C_L = 50 pF Figure 12		25				ns
		2.0			9	17		20	
		2.7			6	13		15	
		3.0 to 3.6			5[2]	10		12	
		4.5			4	9		10	
		6.0			3	7		8	
t_{PZH}/t_{PZL}	Turn-on time $\overline{E}$, S_n to V_{OS}	1.2	R_L = 1kΩ; C_L = 50 pF Figures 13 and 1		190				ns
		2.0			65	121		146	
		2.7			48	89		108	
		3.0 to 3.6			36[2]	71		86	
		4.5			32	60		73	
		6.0			25	46		56	
t_{PHZ}/t_{PLZ}	Turn-off time $\overline{E}$, Sn to V_{OS}	1.2	R_L = 1kΩ: C_L = 50 pF Figures 13 and 1		125				ns
		2.0			43	80		95	
		2.7			33	59		71	
		3.0 to 3.6			26[2]	48		57	
		4.5			23	41		49	
		6.0			18	32		38	

NOTES:
1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

ADDITIONAL AC CHARACTERISTICS

Recommended conditions and typical values
GND = 0 V; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	Sine-wave distortion f = 1 kHz	0.80 0.40	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pf Figure 9 and 10
	Sine-wave distortion f = 10 kHz	2.40 1.20	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pf Figure 9 and 10
	Switch "OFF" signal feed through	–50 –50	dB	3.0 6.0	Note 1	R_L = 600 Ω; C_L = 50 pf; f= 1 MHz Figures 5 and 11
	Crosstalk between any two switches/multiplexers	–60 –60	dB	3.0 6.0	Note 1	R_L = 600 Ω; C_L = 50 pf; f= 1 MHz Figure 8
$V_{(p-p)}$	Crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 120	mV	3.0 6.0		R_L = 600 Ω; C_L = 50 pf; f= 1 MHz (S_n or $\overline{E}$, square wave between V_{CC} and GND $t_r = t_f$ = 6 ns) Figure 8
f_{max}	Minimum frequency response (–3 dB)	180 200	MHz	3.0 6.0	Note 2	R_L = 50 Ω; C_L = 50 pF Figures 6, 8 and 9
C_S	Maximum switch capacitance	5	pf			

GENERAL NOTES:

1. V_{is} is the input voltage at nY or nZ terminal, whichever is assigned as an input.
2. V_{OS} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

NOTES:

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

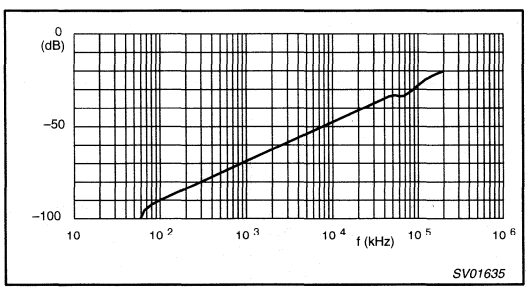


Figure 6. Typical switch "OFF" signal feed-through as a function of frequency.

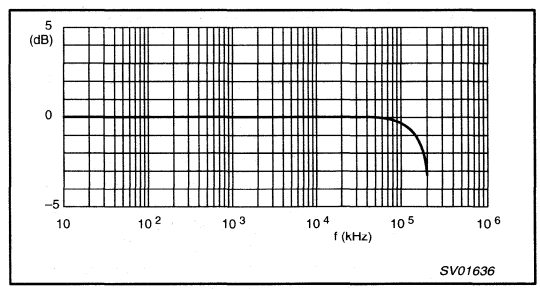


Figure 7. Typical frequency response.

NOTES TO FIGURES 6 AND 7:

Test conditions: V_{CC} = 3.0 V; GND = 0 V; V_{EE} = -3.0 V; R_L = 50 Ω; R_{SOURCE} = 1kΩ.

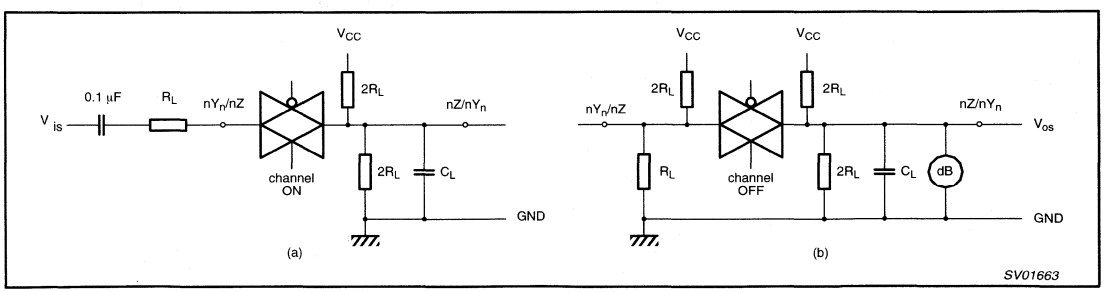
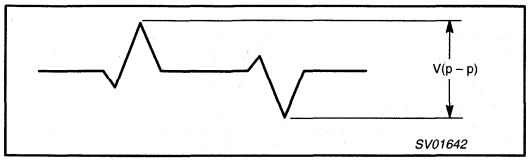


Figure 8. Test circuit for measuring crosstalk between any two switches. (a) channel ON condition; (b) channel OFF condition.

NOTE TO FIGURE 8:
The crosstalk is defined as follows (oscilloscope output):



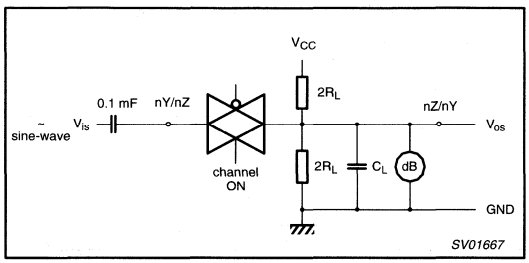


Figure 10. Test circuit for measuring minimum frequency response.

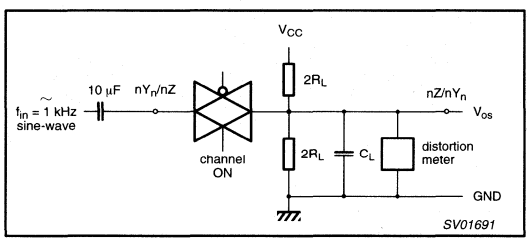


Figure 11. Test circuit for measuring sine-wave distortion.

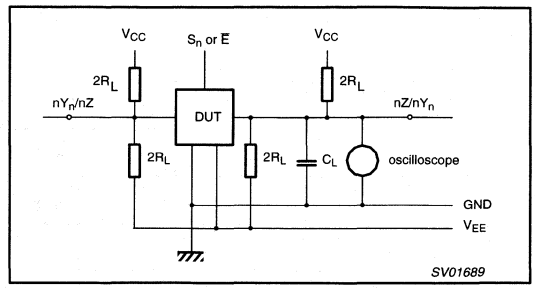


Figure 9. Test circuit for measuring crosstalk between control and any switch.

NOTE TO FIGURE 9:
Adjust input voltage to obtain 0 dBm at V_{OS} when F_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of –3 dB at V_{OS}.

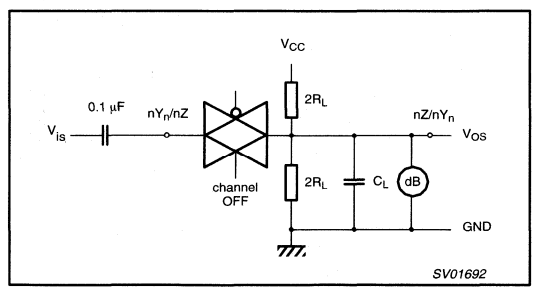


Figure 12. Test circuit for measuring switch "OFF" signal feed-through.

WAVEFORMS

NOTES:

1. $V_M = 1.5$ V at 2.7 V ≤ V_{CC} ≤ 3.6 V
   $V_M = 0.5 \times V_{CC}$ at 2.7 V > V_{CC} > 3.6 V
2. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
3. $V_x = V_{OL} + 0.3$ V at 2.7 V ≤ V_{CC} ≤ 3.6 V
   $V_X = V_{OL} + 0.1 \times V_{CC}$ at 2.7 V > V_{CC} > 3.6 V
   $V_Y = V_{OH} - 0.3$ V at 2.7 V ≤ V_{CC} ≤ 3.6 V
   $V_Y = V_{OH} - 0.1 \times V_{CC}$ at 2.7 V > V_{CC} > 3.6 V

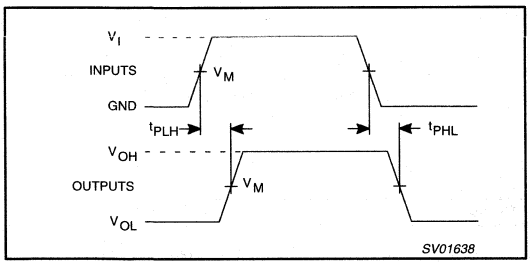


Figure 13. Input (V_{is}) to output (V_{os}) propagation delays.

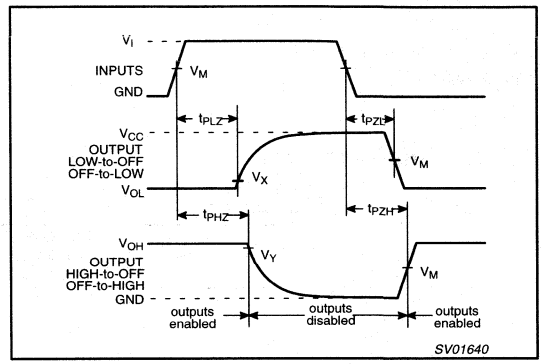
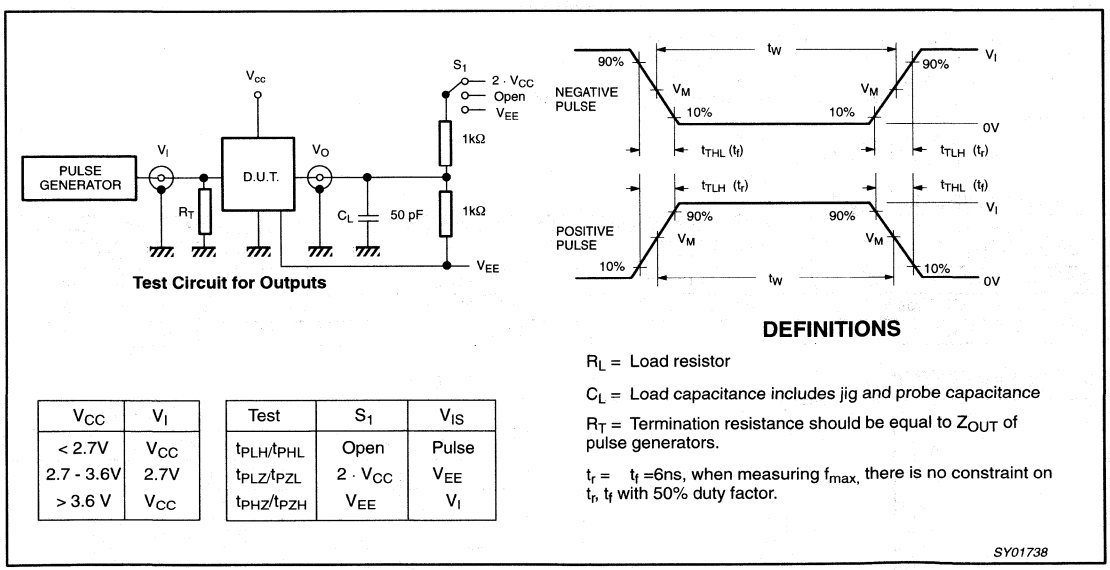


Figure 14. Turn-on and turn-off times for the inputs (S_n, E) to the output (V_{os}).

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7 - 3.6V	2.7V
> 3.6 V	V_{CC}

Test	S_1	V_{IS}
t_{PLH}/t_{PHL}	Open	Pulse
t_{PLZ}/t_{PZL}	2 · V_{CC}	V_{EE}
t_{PHZ}/t_{PZH}	V_{EE}	V_I

Figure 15. Load circuitry for switching times.

Triple 2-channel analog multiplexer/demultiplexer 74LV4053

FEATURES

- Optimized for low voltage applications: 1.0 to 6.0 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Low typ "ON" resistance:
  100 Ω at $V_{cc} - V_{EE}$ = 4.5 V
  150 Ω at $V_{cc} - V_{EE}$ = 3.0 V
  240 Ω at $V_{cc} - V_{EE}$ = 2.0 V
- Logic level translation: to enable 3 V logic to communicate with ± 3 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4053 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4053.

The 74LV4053 is a triple 2-channel analog multiplexer/demultiplexer with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (nY_0 to nY_1), a common input/output (nZ) and three digital select inputs (S_1 to S_3).

With $\overline{E}$ LOW, one of the two switches is selected (low impedance ON-state) by S_1 to S_3 With $\overline{E}$ HIGH, all switches are in the high impedance OFF-states, independent of S_1 and S_3.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_1, to S_3, and $\overline{E}$). The V_{CC} to GND ranges are 1.0 to 6.0 V. The analog inputs/outputs (nY_0, to nY_1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. V_{CC} - V_{EE} may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn "ON" time $\overline{E}$ to V_{OS} S_n to V_{OS}	C_L = 15 pF R_L = 1KΩ V_{CC} = 3.3 V	 16 20	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time $\overline{E}$ to V_{OS} S_n to V_{OS}		 17 16	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	See Notes 1 and 2	36	pF
C_S	Maximum switch capacitance independent (Y) common (Z)		5 8	pF

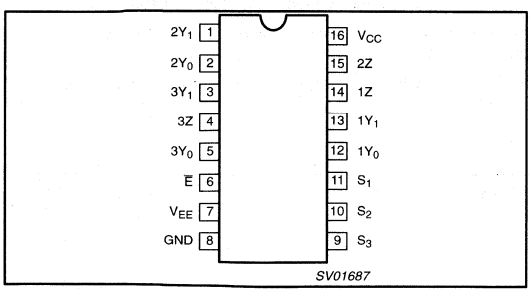
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = maximum switch capacitance in pF;
   V_{CC} = supply voltage in V;
   $\sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV4053 N	74LV4053 N	SOT38-1
16-Pin Plastic SO	–40°C to +125°C	74LV4053 D	74LV4053 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV4053 DB	74LV4053 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV4053 PW	74LV4053PW DH	SOT403-1

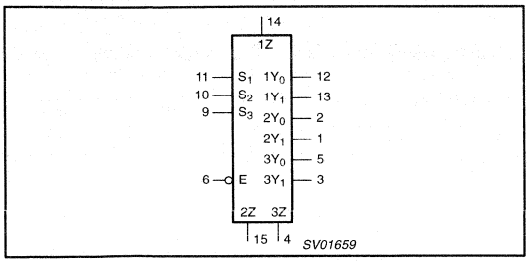
PIN CONFIGURATION



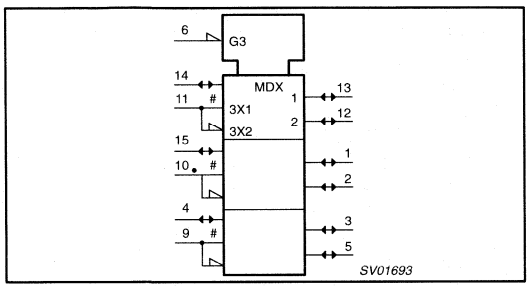
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 1	$2Y_0$, $2Y_1$	Independent inputs/outputs
5, 3	$3Y_0$, $3Y_1$	Independent inputs/outputs
6	$\overline{E}$	Enable input (active LOW)
7	V_{EE}	Negative supply voltage
8	GND	Ground (0 V)
11, 10, 9	S_1 to S_3	Select inputs
12, 13	$1Y_0$, $1Y_1$	Independent inputs/outputs
14, 15, 4	1Z to 3Z	Common inputs/outputs
16	V_{CC}	Positive supply voltage

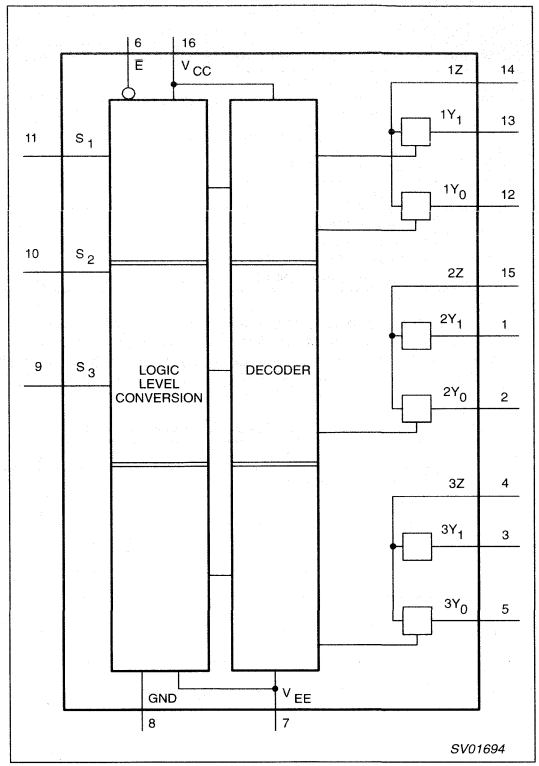
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM

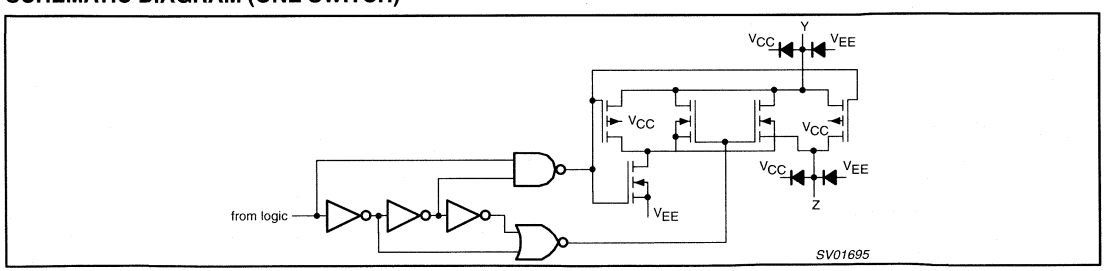


FUNCTION TABLE

INPUTS		CHANNEL ON
$\overline{E}$	Sn	
L	L	$nY_0 - nZ$
L	H	$nY_1 - nZ$
H	X	None

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

SCHEMATIC DIAGRAM (ONE SWITCH)



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V	20	mA
$\pm I_{SK}$	DC switch diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V	20	mA
$\pm I_S$	DC switch current	-0.5 V $< V_S < V_{CC} + 0.5$ V	25	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1 and Figure 5	1.0	3.3	6.0	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 6.0 V	– – –	– – –	500 200 100	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 6.0V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				-40°C to +85°C			-40°C to +125°C		
				MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V		0.9			0.9		V
		V_{CC} = 2.0 V		1.4			1.4		
		V_{CC} = 2.7 to 3.6 V		2.0			2.0		
		V_{CC} = 4.5 V		3.15			3.15		
		V_{CC} = 6.0 V		4.20			4.20		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V				0.3		0.3	V
		V_{CC} = 2.0 V				0.6		0.6	
		V_{CC} = 2.7 to 3.6 V				0.8		0.8	
		V_{CC} = 4.5 V				1.35		1.35	
		V_{CC} = 6.0 V				1.80		1.80	
$\pm I_I$	Input leakage current	V_{CC} = 3.6	V_I = V_{CC} or GND			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
$\pm I_S$	Analog switch OFF-state current per channel	V_{CC} = 3.6	V_I = V_{IH} or V_{IL}; $\lvert V_S \rvert$ = V_{CC} - GND (See Figure 2)			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
$\pm I_S$	Analog switch ON-state current	V_{CC} = 3.6	V_I = V_{IH} or V_{IL}; $\lvert V_S \rvert$ = V_{CC} - GND (See Figure 3)			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
I_{CC}	Quiescent supply current	V_{CC} = 3.6 V	V_I = V_{CC} or GND; V_{IS} = GND or V_{CC}; V_{OS} = V_{CC} or GND			20.0		40	µA
		V_{CC} = 6.0 V				40.0		80	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 to 3.6 V	V_I = V_{CC} – 0.6 V			500		850	µA
R_{ON}	ON-resistance (peak)	V_{CC} = 1.2 V	I_S = 100 µA; V_{IS} = V_{CC} to GND; V_I = V_{IH} or V_{IL}						Ω
		V_{CC} = 2.0 V	I_S = 1000 µA; V_{IS} = V_{CC} to GND; V_I = V_{IH} or V_{IL}		180	365		435	
		V_{CC} = 2.7 V			115	225		270	
		V_{CC} = 3.0 to 3.6 V			100	200		245	
		V_{CC} = 4.5 V			75	150		180	
		V_{CC} = 6.0 V			70	140		165	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V	I_S = 100 µA; V_{IS} = GND; V_I = V_{IH} or V_{IL}		250				Ω
		V_{CC} = 2.0 V	I_S = 1000 µA; V_{IS} = GND; V_I = V_{IH} or V_{IL}		120	280		325	
		V_{CC} = 2.7 V			75	170		195	
		V_{CC} = 3.0 to 3.6 V			70	155		180	
		V_{CC} = 4.5 V			50	120		135	
		V_{CC} = 6.0 V			45	105		120	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V	V_I = V_{IH} or V_{IL}; I_S = 100 µA; V_{IS} = V_{CC}		350				Ω
		V_{CC} = 2.0 V	V_I = V_{IH} or V_{IL}; I_S = 1000 µA; V_{IS} = V_{CC}		170	340		400	
		V_{CC} = 2.7 V			105	210		250	
		V_{CC} = 3.0 to 3.6 V			95	190		225	
		V_{CC} = 4.5 V			70	140		165	
		V_{CC} = 6.0 V			65	125		150	

DC ELECTRICAL CHARACTERISTICS (*Continued*)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				-40°C to +85°C			-40°C to +125°C		
				MIN	TYP[1]	MAX	MIN	MAX	
ΔR_{ON}	Maximum variation of ON-resistance between any two channels	V_{CC} = 1.2 V	$V_I = V_{IH}$ or V_{IL}; $V_{IS} = V_{CC}$ to GND						Ω
		V_{CC} = 2.0 V			5				
		V_{CC} = 2.7 V			4				
		V_{CC} = 3.0 to 3.6 V			4				
		V_{CC} = 4.5 V			3				
		V_{CC} = 6.0 V			2				

NOTES:

1. All typical values are measured at T_{amb} = 25°C.
2. At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

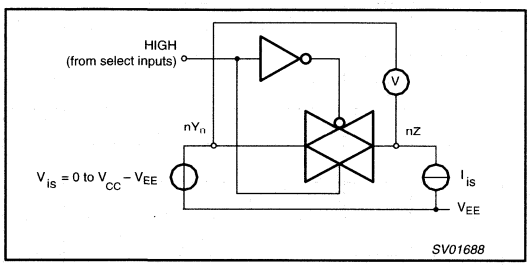


Figure 1. Test circuit for measuring ON-resistance (R_{ON}).

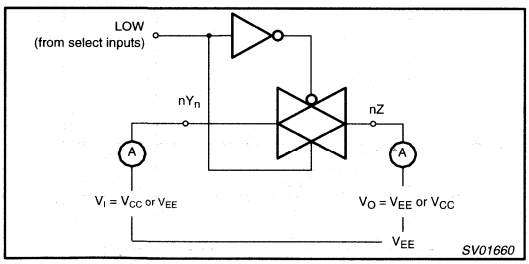


Figure 2. Test circuit for measuring OFF-state current.

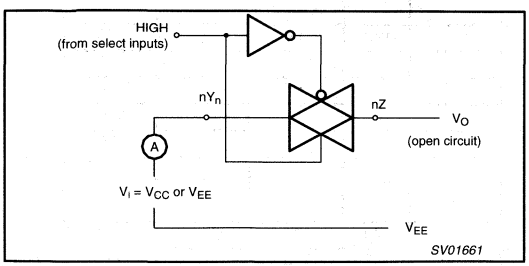


Figure 3. Test circuit for measuring ON-state current.

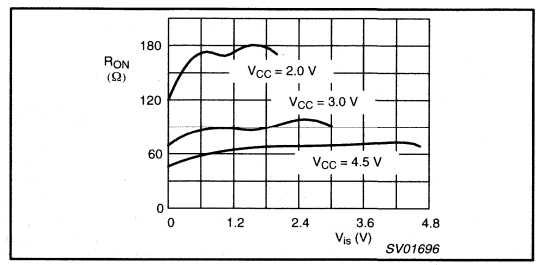


Figure 4. Typical ON-resistance (R_{on}) as a function of input voltage (V_{is}) for V_{is} = 0 to $V_{CC} - V_{EE}$.

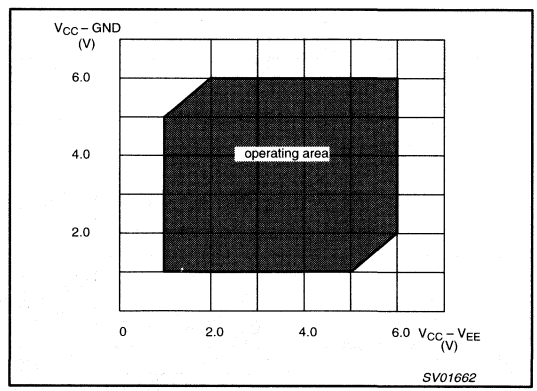


Figure 5. Guaranteed operating area as a function of the supply voltages.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	CONDITION		LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
		V_{CC} (V)	OTHER	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay V_{is} to V_{os}	1.2	$R_L = \infty$; C_L = 50 pF Figure 12		25				ns
		2.0			9	17		20	
		2.7			6	13		15	
		3.0 to 3.6			5[2]	10		12	
		4.5			4	9		10	
		6.0			3	7		8	
t_{PZH}/t_{PZL}	Turn-on time $\overline{E}$ to V_{os}	1.2	R_L = 1kΩ; C_L = 50 pF Figures 13 and 1		100				ns
		2.0			34	65		77	
		2.7			25	48		56	
		3.0 to 3.6			19[2]	38		45	
		4.5			17	32		38	
		6.0			13	25		29	
t_{PZH}/t_{PZL}	Turn-on time S_n to V_{os}	1.2	R_L = 1kΩ C_L = 50 pF Figures 13 and 1		125				ns
		2.0			43	82		97	
		2.7			31	60		71	
		3.0 to 3.6			24[2]	48		57	
		4.5			21	41		48	
		6.0			16	31		37	
t_{PHZ}/t_{PLZ}	Turn-off time $\overline{E}$ to V_{os}	1.2	R_L = 1kΩ C_L = 50 pF Figures 13 and 1		95				ns
		2.0			34	61		73	
		2.7			26	46		54	
		3.0 to 3.6			20[2]	37		44	
		4.5			18	32		38	
		6.0			15	25		30	
t_{PHZ}/t_{PLZ}	Turn-off time Sn to V_{os}	1.2	R_L = 1kΩ C_L = 50 pF Figures 13 and 1		90				ns
		2.0			32	59		70	
		2.7			24	44		52	
		3.0 to 3.6			19[2]	36		42	
		4.5			17	31		36	
		6.0			14	24		28	

NOTES:

1. Unless otherwise stated, all typical values are measured at T_{amb} = 25°C
2. Typical values are measured at V_{CC} = 3.3 V.

ADDITIONAL AC CHARACTERISTICS

Recommended conditions and typical values
GND = 0 V; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	Sine-wave distortion f = 1 kHz	0.80 0.40	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pf Figures 9 and 10
	Sine-wave distortion f = 10 kHz	2.40 1.20	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pf Figures 9 and 10
	Switch "OFF" signal feed through	−50 −50	dB	3.0 6.0	Note 1	R_L = 600 Ω; C_L = 50 pf; f= 1 MHz Figures 5 and 11
	Crosstalk between any two switches/multiplexers	−60 −60	dB	3.0 6.0	Note 1	R_L = 600 Ω; C_L = 50 pf; f= 1 MHz Figure 8
$V_{(p-p)}$	Crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 120	mV	3.0 6.0		R_L = 600 Ω; C_L = 50 pf; f= 1 MHz (S_n or $\overline{E}$, square wave between V_{CC} and GND $t_r = t_f$ = 6 ns) Figure 8
f_{max}	Minimum frequency response (−3 dB)	180 200	MHz	3.0 6.0	Note 2	R_L = 50 Ω; C_L = 50 pF Figures 6, 8 and 9
C_S	Maximum switch capacitance	5	pf			

GENERAL NOTES:

V_{is} is the input voltage at nY_n or nZ terminal, whichever is assigned as an input.
V_{OS} is the output voltage at nY_n or nZ terminal, whichever is assigned as an output.

NOTES:

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

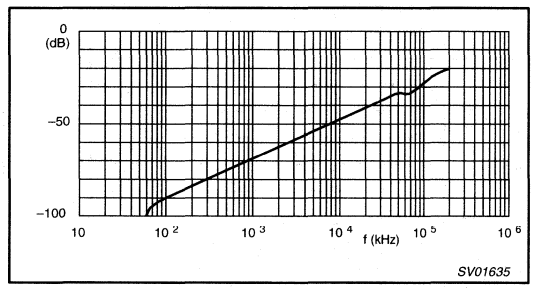


Figure 6. Typical switch "OFF" signal feed-through as a function of frequency.

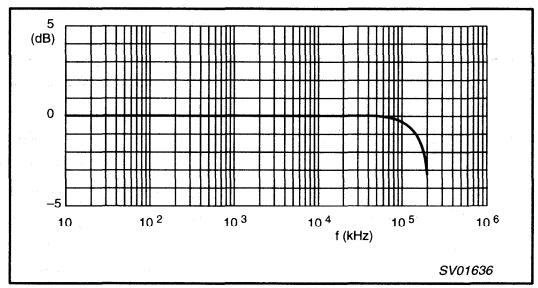


Figure 7. Typical frequency response.

NOTES TO FIGURES 6 AND 7:

Test conditions: V_{CC} = 3.0 V; GND = 0 V; V_{EE} = -3.0V; R_L = 50 Ω; R_{SOURCE} = 1kΩ.

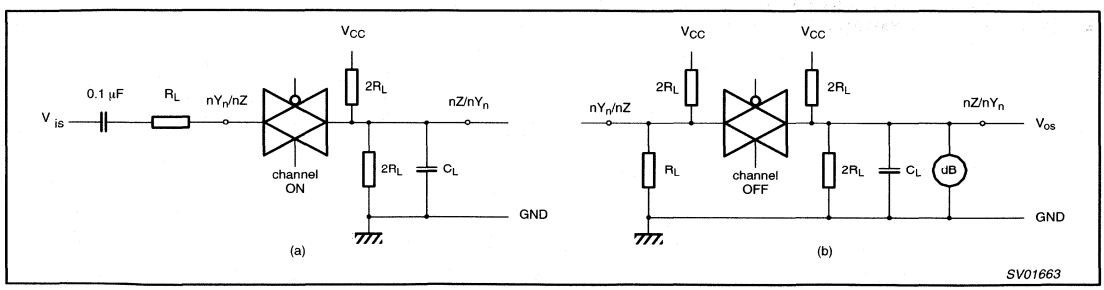
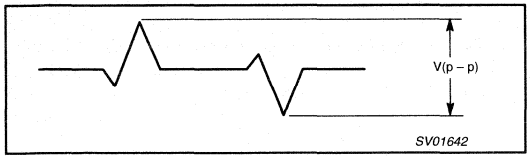


Figure 8. Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

NOTE TO FIGURE 8:
The crosstalk is defined as follows (oscilloscope output):



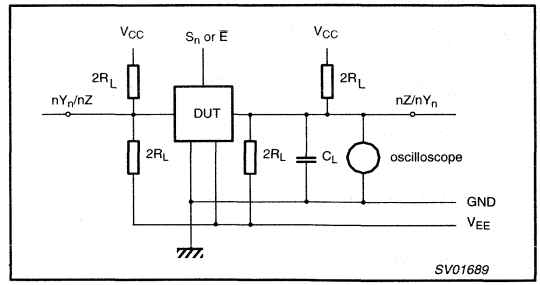


Figure 9. Test circuit for measuring crosstalk between control and any switch.

NOTE TO FIGURE 9:
Adjust input voltage to obtain 0 dBm at V_{OS} when F_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of –3 dB at V_{OS}.

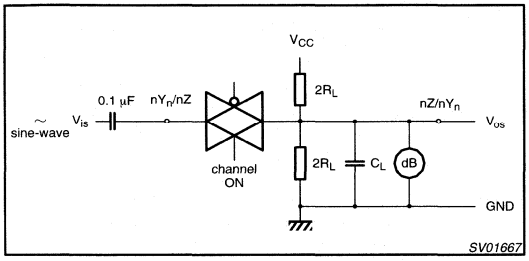


Figure 10. Test circuit for measuring minimum frequency response.

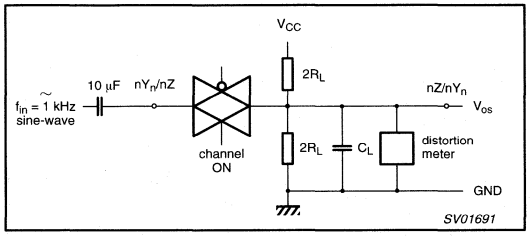


Figure 11. Test circuit for measuring sine-wave distortion.

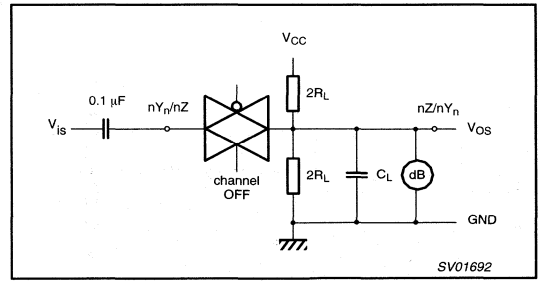


Figure 12. Test circuit for measuring switch "OFF" signal feed-through.

WAVEFORMS

V_M = 1.5 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_M = 0.5 × V_{CC} at 2.7 V > V_{CC} > 3.6 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
V_x = V_{OL} + 0.3 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_X = V_{OL} + 0.1 × V_{CC} at 2.7 V >V_{CC} > 3.6 V
V_Y = V_{OH} – 0.3 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_Y = V_{OH} – 0.1 × V_{CC} at 2.7 V >V_{CC} > 3.6 V

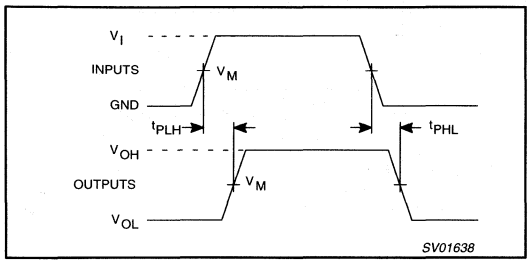


Figure 13. Input (V_{IS}) to output (V_{OS}) propagation delays.

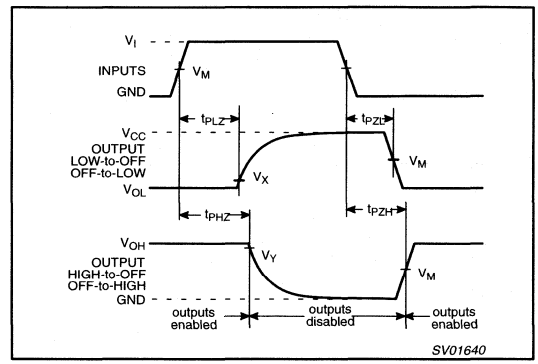
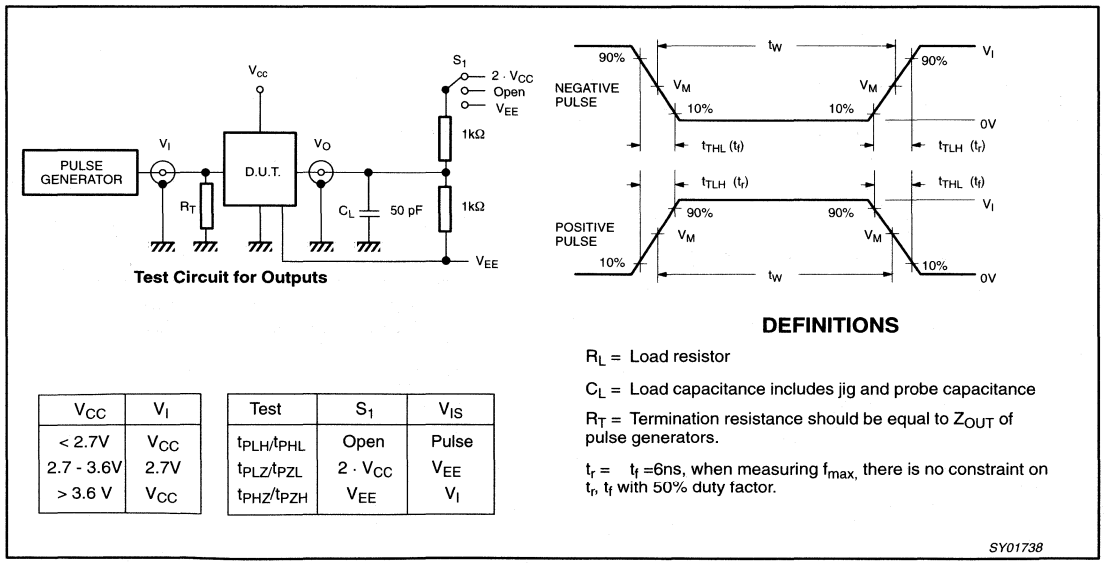


Figure 14. Turn-on and turn-off times for the inputs (S_n, $\overline{E}$) to the output (V_{OS}).

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7 - 3.6V	2.7V
> 3.6 V	V_{CC}

Test	S_1	V_{IS}
t_{PLH}/t_{PHL}	Open	Pulse
t_{PLZ}/t_{PZL}	2 · V_{CC}	V_{EE}
t_{PHZ}/t_{PZH}	V_{EE}	V_I

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

t_r = t_f =6ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

SY01738

Figure 15. Load circuitry for switching times.

14-stage binary ripple counter with oscillator 74LV4060

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C.
- All active components on chip
- RC or crystal oscillator configuration
- Output capability: standard (except for R_{TC} and C_{TC})
- I_{CC} category: MSI

APPLICATIONS

- Control Counters
- Timers
- Frequency Dividers
- Time-delay circuits

DESCRIPTION

The 74LV4060 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT4060.

The 74LV4060 is a 14-stage ripple-carry counter/divider and oscillator with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (Q_3 to Q_9 and Q_{11} to Q_{13}) and an overriding asynchronous master reset (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case, keep the oscillator pins (R_{TC} and C_{TC}) floating.

The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q_3 to Q_9 and Q_{11} to Q_{13} = LOW), independent of the other input conditions.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
	Propagation delay	C_L = 15 pF		
	RS to Q_3	V_{CC} = 3.3 V	29	
t_{PHL}/t_{PLH}	Q_n to Q_{n+1}		6	ns
t_{PHL}	MR to Q_n		16	
f_{max}	Maximum clock frequency		99	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per package	Notes 1, 2 and 3	40	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}
3. For formula on dynamic power dissipation, see the following pages.

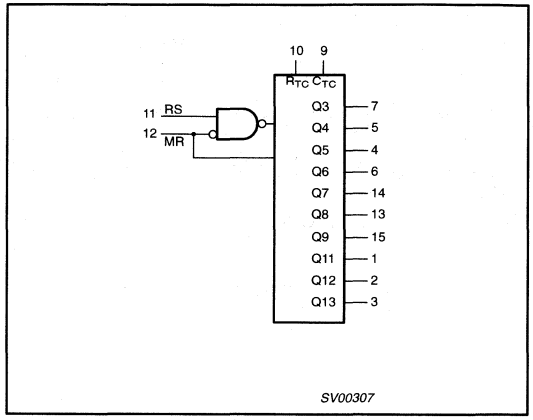
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV4060 N	74LV4060 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV4060 D	74LV4060 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV4060 DB	74LV4060 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV4060 PW	74LV4060PW DH	SOT403-1

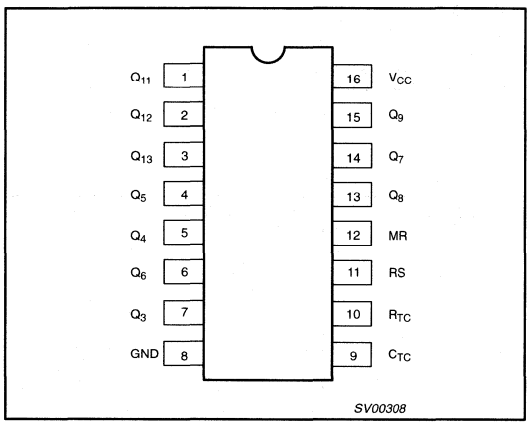
PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1, 2, 3	Q_{11} to Q13	Counter outputs
7, 5, 4, 6, 15, 13, 15	Q_3 to Q_9	Counter outputs
8	GND	Ground (0 V)
9	C_{TC}	External capacitor connection
10	R_{TC}	External resistor connection
11	RS	Clock input/oscillator pin
12	MR	Master reset
16	V_{CC}	Positive supply voltage

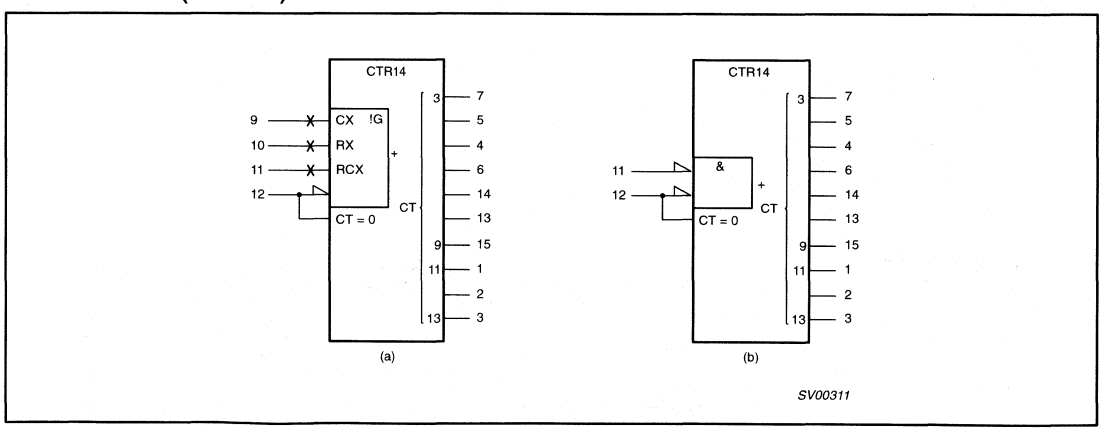
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



DYNAMIC POWER DISSIPATION

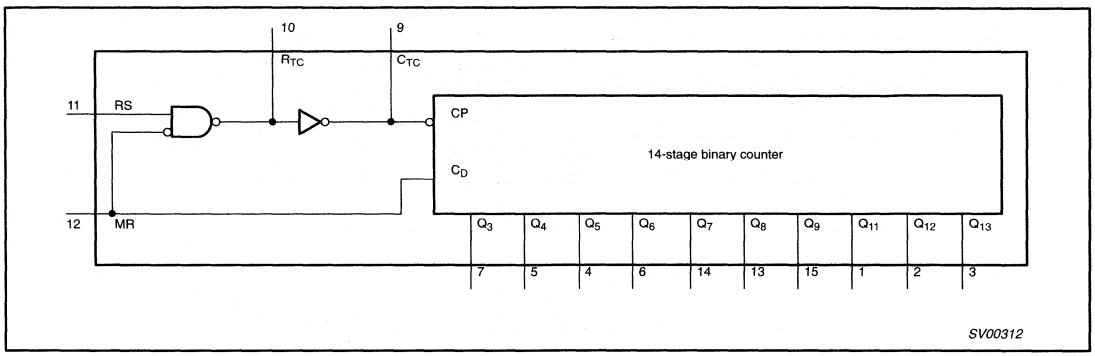
GND = 0 V; T_{amb} = 25 °C

PARAMETER	V_{CC} (V)	TYPICAL FORMULA FOR P_D (μW)[1]
Total dynamic power dissipation when using the on–chip oscillator (P_D)	1.2	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 16 \times V_{CC}$
	2.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 460 \times V_{CC}$
	3.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \Sigma (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1000 \times V_{CC}$

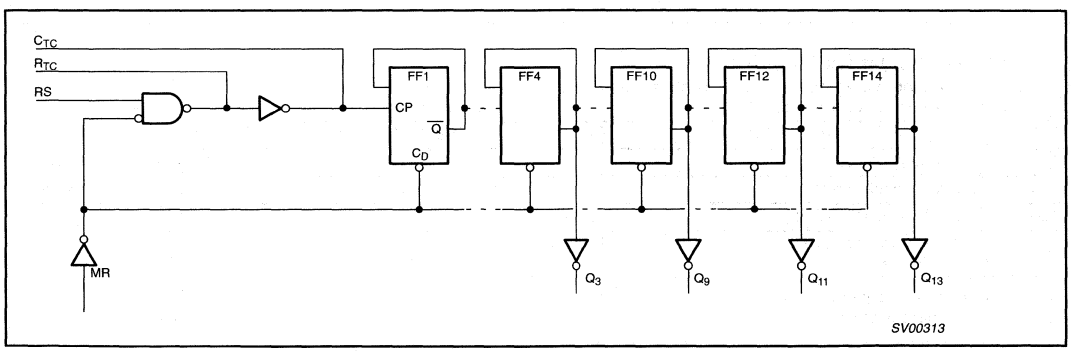
NOTE:

1. Where: f_o = output frequency in MHz; f_{osc} = oscillator frequency in MHz;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs; C_L = output load capacitance in pF;
   C_t = timing capacitance in pF; V_{CC} = supply voltage in V.

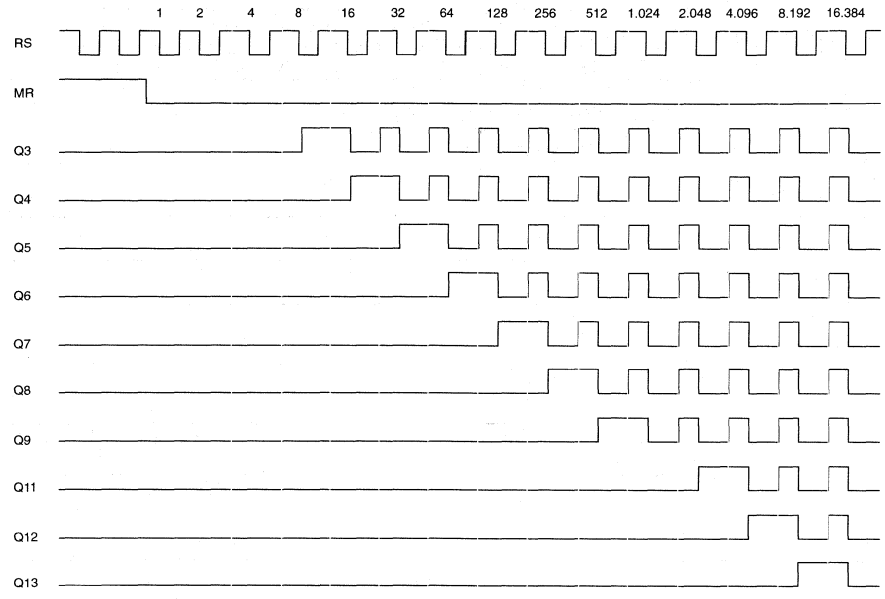
FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with –standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note[1]	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTES:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC CHARACTERISTICS

Over operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage MR input	V_{CC} = 1.2V	0.9	–	–	0.9	–	V
		V_{CC} = 2.0V	1.4	–	–	1.4	–	
		V_{CC} = 2.7 to 3.6V	2.0	–	–	2.0	–	
		V_{CC} = 4.5 to 5.5V	0.7 * V_{CC}	–	–	0.7 * V_{CC}	–	
V_{IL}	LOW level Input voltage MR input	V_{CC} = 1.2V	–	–	0.3	–	0.3	V
		V_{CC} = 2.0V	–	–	0.6	–	0.6	
		V_{CC} = 2.7 to 3.6V	–	–	0.8	–	0.8	
		V_{CC} = 4.5 to 5.5	–	–	0.3 * V_{CC}	–	0.3 * V_{CC}	
V_{IH}	HIGH level Input voltage RS input	V_{CC} = 1.2V	1.0	–	–	1.0	–	V
		V_{CC} = 2.0V	1.6	–	–	1.6	–	
		V_{CC} = 2.7 to 3.6V	2.4	–	–	2.4	–	
		V_{CC} = 4.5 to 5.5V	0.8 * V_{CC}	–	–	0.8 * V_{CC}	–	
V_{IL}	LOW level Input voltage RS input	V_{CC} = 1.2V	–	–	0.2	–	0.2	V
		V_{CC} = 2.0V	–	–	0.4	–	0.4	
		V_{CC} = 2.7 to 3.6V	–	–	0.5	–	0.5	
		V_{CC} = 4.5 to 5.5	–	–	0.2 * V_{CC}	–	0.2 * V_{CC}	
V_{OH}	HIGH level output voltage; R_{TC} output	V_{CC} = 1.2V; RS = GND and MR = GND; $-I_O$ = 3.4mA	–	–	–	–	–	V
		V_{CC} = 2.0V; RS = GND and MR = GND; $-I_O$ = 3.4mA	–	–	–	–	–	
		V_{CC} = 2.7V; RS = GND and MR = GND; $-I_O$ = 3.4mA	–	–	–	–	–	
		V_{CC} = 3.0V; RS = GND and MR = GND; $-I_O$ = 3.4mA	2.40	2.82	–	2.20	–	
		V_{CC} = 4.5V; RS = GND and MR = GND; $-I_O$ = 3.4mA	–	–	–	–	–	

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
V_{OH}	HIGH level output voltage; R_{TC} output	V_{CC} = 1.2V; RS = V_{CC} and MR = V_{CC}; $-I_O$ = 0.8mA	–	–	–	–	–	V
		V_{CC} = 2.0V; RS = V_{CC} and MR = V_{CC}; $-I_O$ = 0.8mA	–	–	–	–	–	
		V_{CC} = 2.7V; RS = V_{CC} and MR = V_{CC}; $-I_O$ = 0.8mA	–	–	–	–	–	
		V_{CC} = 3.0V; RS = V_{CC} and MR = V_{CC}; $-I_O$ = 0.8mA	2.40	2.82	–	2.20	–	
		V_{CC} = 4.5V; RS = V_{CC} and MR = V_{CC}; $-I_O$ = 0.8mA	–	–	–	–	–	
V_{OH}	HIGH level output voltage; R_{TC} output	V_{CC} = 1.2V; RS = GND and MR = GND; $-I_O$ = 100µA	1.0	1.2	–	1.0	–	V
		V_{CC} = 2.0V; RS = GND and MR = GND; $-I_O$ = 100µA	1.8	2.0	–	1.8	–	
		V_{CC} = 2.7V; RS = GND and MR = GND; $-I_O$ = 100µA	–	–	–	–	–	
		V_{CC} = 3.0V; RS = GND and MR = GND; $-I_O$ = 100µA	2.8	3.0	–	2.8	–	
		V_{CC} = 4.5V; RS = GND and MR = GND; $-I_O$ = 100µA	–	–	–	–	–	
V_{OH}	HIGH level output voltage; R_{TC} output	V_{CC} = 1.2V; RS = V_{CC} and MR = V_{CC}; $-I_O$ = 100µA	1.0	1.2	–	1.0	–	V
		V_{CC} = 2.0V; RS = V_{CC} and MR = V_{CC}; $-I_O$ = 100µA	1.8	2.0	–	1.8	–	
		V_{CC} = 2.7V; RS = V_{CC} and MR = V_{CC}; $-I_O$ = 100µA	–	–	–	–	–	
		V_{CC} = 3.0V; RS = V_{CC} and MR = V_{CC}; $-I_O$ = 100µA	2.8	3.0	–	2.8	–	
		V_{CC} = 4.5V; RS = V_{CC} and MR = V_{CC}; $-I_O$ = 100µA	–	–	–	–	–	
V_{OH}	HIGH level output voltage; C_{TC} output	V_{CC} = 1.2V; RS = V_{IH} and MR = V_{IL}; $-I_O$ = 3.8mA		1.2	–	–	–	V
		V_{CC} = 2.0V; RS = V_{IH} and MR = V_{IL}; $-I_O$ = 3.8mA	–	–	–	–	–	
		V_{CC} = 2.7V; RS = V_{IH} and MR = V_{IL}; $-I_O$ = 3.8mA	–	–	–	–	–	
		V_{CC} = 3.0V; RS = V_{IH} and MR = V_{IL}; $-I_O$ = 3.8mA	2.40	2.82	–	2.20	–	
		V_{CC} = 4.5V; RS = V_{IH} and MR = V_{IL}; $-I_O$ = 3.8mA	–	–	–	–	–	
V_{OH}	HIGH level output voltage; except R_{TC} output	V_{CC} = 1.2V; V_I = V_{IH} and V_I = V_{IL}; $-I_O$ = 100µA	1.0	1.2	–	1.0	–	V
		V_{CC} = 2.0V; V_I = V_{IH} and V_I = V_{IL}; $-I_O$ = 100µA	1.8	2.0	–	1.8	–	
		V_{CC} = 2.7V; V_I = V_{IH} and V_I = V_{IL}; $-I_O$ = 100µA	–	–	–	–	–	
		V_{CC} = 3.0V; V_I = V_{IH} and V_I = V_{IL}; $-I_O$ = 100µA	2.8	3.0	–	2.8	–	
		V_{CC} = 4.5V; V_I = V_{IH} and V_I = V_{IL}; $-I_O$ = 100µA	–	–	–	–	–	

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
V_{OH}	HIGH level output voltage; except R_{TC} and C_{TC} outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 6mA	–	–	–	–	–	V
		V_{CC} = 2.0V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 6mA	–	–	–	–	–	
		V_{CC} = 2.7V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 6mA	–	–	–	–	–	
		V_{CC} = 3.0V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 6mA	2.40	2.82	–	2.20	–	
		V_{CC} = 4.5V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 6mA	–	–	–	–	–	
V_{OL}	LOW level output voltage; R_{TC} output	V_{CC} = 1.2V; RS = V_{CC} and MR = GND; $-I_O$ = 3.4mA	–	–	–	–	–	V
		V_{CC} = 2.0V; RS = V_{CC} and MR = GND; $-I_O$ = 3.4mA	–	–	–	–	–	
		V_{CC} = 2.7V; RS = V_{CC} and MR = GND; $-I_O$ = 3.4mA	–	–	–	–	–	
		V_{CC} = 3.0V; RS = V_{CC} and MR = GND; $-I_O$ = 3.4mA	–	0.25	0.40	–	0.50	V
		V_{CC} = 4.5V; RS = V_{CC} and MR = GND; $-I_O$ = 3.4mA	–	–	–	–	–	V
V_{OL}	LOW level output voltage; R_{TC} output	V_{CC} = 1.2V; RS = V_{CC} and MR = GND; $-I_O$ = 100µA	–	0	0.2	–	0.2	V
		V_{CC} = 2.0V; RS = V_{CC} and MR = GND; $-I_O$ = 100µA	–	0	0.2	–	0.2	
		V_{CC} = 2.7V; RS = V_{CC} and MR = GND; $-I_O$ = 100µA	–	–	–	–	–	
		V_{CC} = 3.0V; RS = V_{CC} and MR = GND; $-I_O$ = 100µA	–	0	0.2	–	0.2	
		V_{CC} = 4.5V; RS = V_{CC} and MR = GND; $-I_O$ = 100µA	–	–	–	–	–	
V_{OL}	LOW level output voltage; C_{TC} output	V_{CC} = 1.2V; RS = V_{IH} and MR = V_{IL}; $-I_O$ = 3.8mA	–	–	–	–	–	V
		V_{CC} = 2.0V; RS = V_{IH} and MR = V_{IL}; $-I_O$ = 3.8mA	–	–	–	–	–	
		V_{CC} = 2.7V; RS = V_{IH} and MR = V_{IL}; $-I_O$ = 3.8mA	–	–	–	–	–	
		V_{CC} = 3.0V; RS = V_{IH} and MR = V_{IL}; $-I_O$ = 3.8mA	–	0.25	0.40	–	0.50	
		V_{CC} = 4.5V; RS = V_{IH} and MR = V_{IL}; $-I_O$ = 3.8mA	–	–	–	–	–	
V_{OL}	LOW level output voltage; except R_{TC} output	V_{CC} = 1.2V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 100µA	–	0	0.2	–	0.2	V
		V_{CC} = 2.0V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 100µA	–	0	0.2	–	0.2	
		V_{CC} = 2.7V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 100µA	–	–	–	–	–	
		V_{CC} = 3.0V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 100µA	–	0	0.2	–	0.2	
		V_{CC} = 4.5V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 100µA	–	–	–	–	–	

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
V_{OL}	HIGH level output voltage; except R_{TC} and C_{TC} outputs	V_{CC} = 1.2V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 6mA	–	–	–	–	–	V
		V_{CC} = 2.0V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 6mA	–	–	–	–	–	
		V_{CC} = 2.7V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 6mA	–	0.25	0.40	–	0.50	
		V_{CC} = 3.0V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 6mA	–	–	–	–	–	
		V_{CC} = 4.5V; $V_I = V_{IH}$ and $V_I = V_{IL}$; $-I_O$ = 6mA	–	–	–	–	–	
I_I	Input leakage current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND	–	–	1.0	–	1.0	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0	–	–	20	–	160	µA
	Quiescent supply current	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND; I_O = 0	–	–	–	–	80	
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0	–	–	500	–	850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay RS to Q_3	Figures, 6, 8	1.2	–	180	–	–	–	ns
			2.0	–	52	84	–	105	
			2.7	–	42	66	–	83	
			3.0 to 3.6	–	33[2]	53	–	66	
			4.5 to 5.5	–	24	39	–	49	
t_{PHL}/t_{PLH}	Propagation delay Q_n to Q_{n+1}	Figures 7, 8	1.2	–	40	–	–	–	ns
			2.0	–	14	23	–	29	
			2.7	–	10	16	–	20	
			3.0 to 3.6	–	8[2]	13	–	16	
			4.5 to 5.5	–	6	9	–	11	
t_{PHL}	Propagation delay MR to Q_n	Figures 7, 8	1.2	–	100	–	–	–	ns
			2.0	–	29	46	–	58	
			2.7	–	24	39	–	49	
			3.0 to 3.6	–	19[2]	31	–	39	
			4.5 to 5.5	–	14	23	–	29	
t_W	Clock pulse width RS; HIGH or LOW	Figure 6	2.0	34	9	–	38	–	ns
			2.7	25	6	–	30	–	
			3.0 to 3.6	20	5	–	24	–	
			4.5 to 5.5	16	4	–	20	–	
t_W	Master reset pulse width MR; HIGH	Figure 7	2.0	34	10	–	38	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	6	–	24	–	
			4.5 to 5.5	16	4	–	20	–	

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS –40 to +85 °C			LIMITS –40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{rem}	Removal time MR to RS	Figure 7	2.0	29	18	–	37	–	ns
			2.7	26	16	–	32	–	
			3.0 to 3.6	18	11	–	23	–	
			4.5 to 5.5	12	7	–	15	–	
f_{max}	Maximum clock pulse frequency	Figure 6	2.0	14	40	–	9	–	MHz
			2.7	19	70	–	12	–	
			3.0 to 3.6	24	90	–	15	–	
			4.5 to 5.5	30	100	–	19	–	

NOTE:
Unless otherwise stated, all typical values are at T_{amb} = 25°C.
1. Typical value measured at V_{CC} = 3.3V.
2. Typical value measured at V_{CC} = 5.0V.

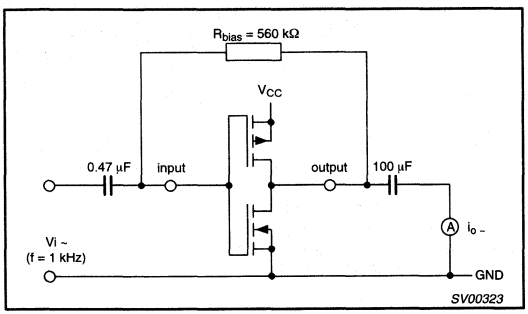


Figure 1.
Test set-up for measuring forward transconductance
$g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Figure 2); MR = LOW.

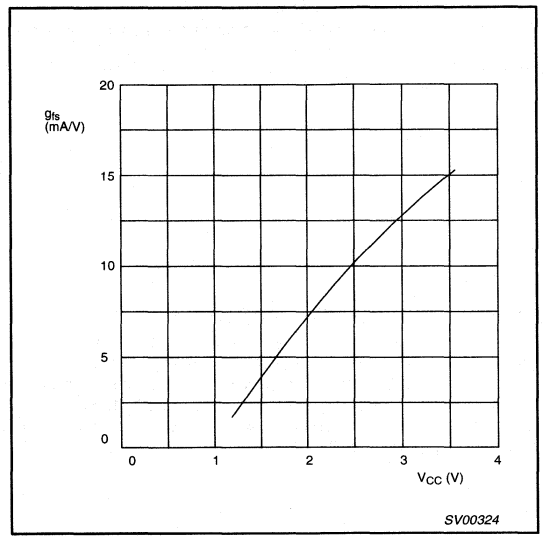


Figure 2.
Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25°C.

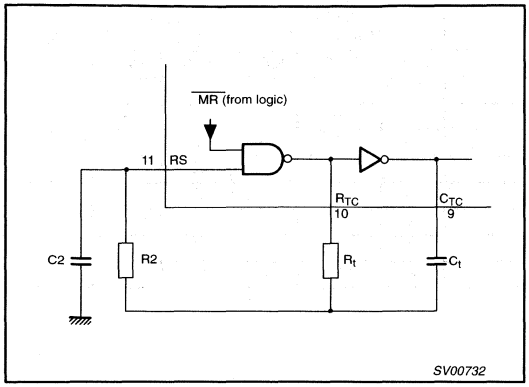


Figure 3.

Example of an RC oscillator. Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$$

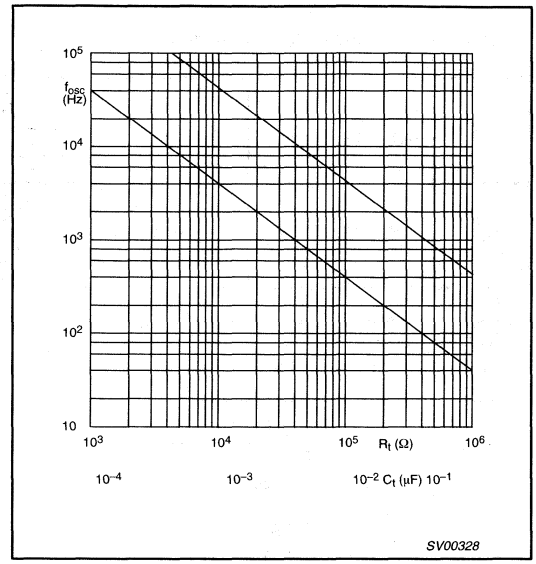


Figure 4.

RC oscillator frequency as a function of R_t and C_t at V_{CC} = 1.2 to 3.6 V; T_{amb} = 25°C.
C_t curve at R_t = 100 kΩ; R2 = 200 kΩ.
R_t curve at C_t = 1 nF; R2 = 2 x R_t.

TIMING COMPONENTS LIMITATIONS

The oscillator frequency is mainly determined by $R_t \cdot C_t$, provided R2 $\approx 2R_t$ and R2 · C2 $\ll R_t \cdot C_t$. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the 'ON' resistance in series with it, which typically is 280 Ω at V_{CC} = 1.2 V, 130 Ω at V_{CC} = 2.0 V and 100 Ω at V_{CC} 3.0 V. The recommended values for these components to maintain agreement with the typical oscillation formula are: C_t > 50pF, up to any practical value, 10 kΩ < R_t < 1 MΩ. In order to avoid start-up problems, $R_t \geq$ 1 kΩ.

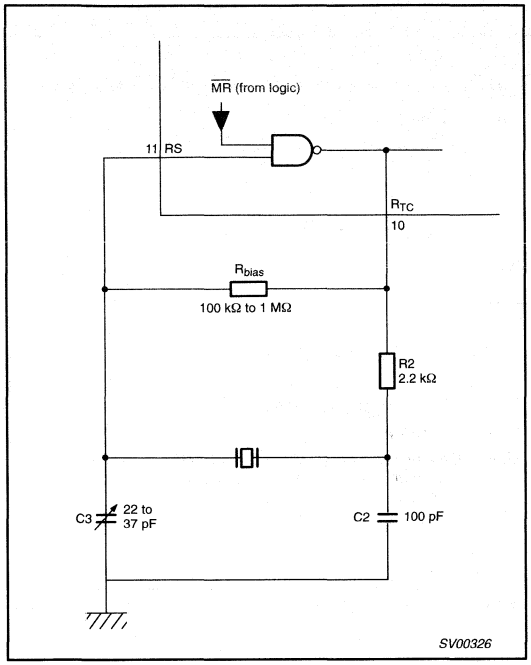


Figure 5. External components connection for a typical crystal oscillator

R2 is the power limiting resistor. For starting and maintaining oscillation, a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.

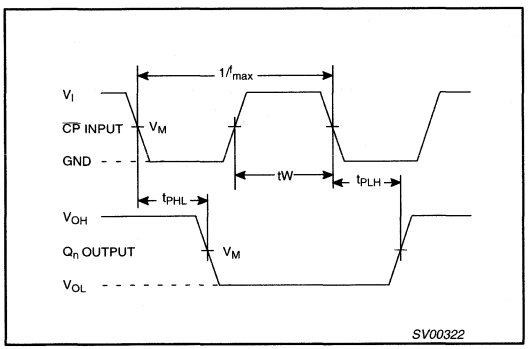


Figure 6.

Waveforms showing the clock (RS) to output (Q_3) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

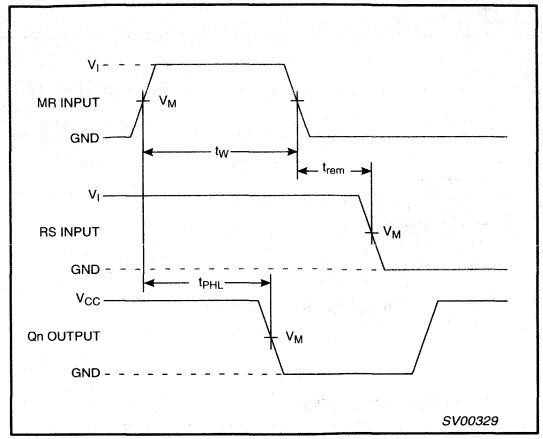


Figure 7.

Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (RS) removal time.

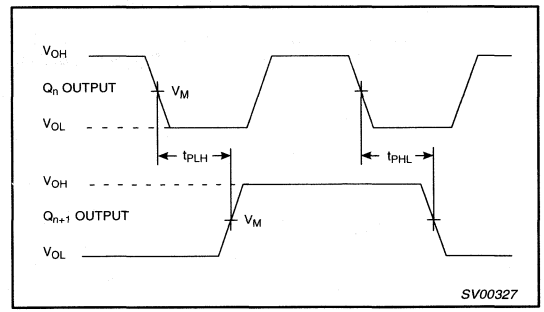


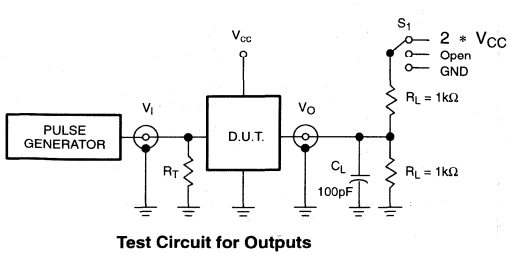
Figure 8.

Waveforms showing the output Q_n to output $_{n+1}$ propagation delays.

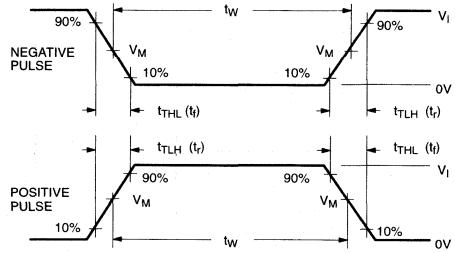
NOTES:

1. $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V and ≤ 3.6 V
   $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V and ≥ 4.5 V.
2. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

TEST CIRCUIT



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5 V	V_{CC}

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SV00910

Figure 9. Load circuitry for switching times.

Quad bilateral switches | 74LV4066

FEATURES

- Optimized for Low Voltage applications: 1.0V to 6.0V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C.
- Very low typ "ON" resistance:
  25Ω at V_{CC} – VEE = 4.5 V
  35Ω at V_{CC} – VEE = 3.0 V
  60Ω at V_{CC} – VEE = 2.0 V
- Output capability: non-standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV4066 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT4066.

The 74LV4066 has four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the corresponding analog switch is turned off.

The 74LV4066 has an on resistance which is dramatically reduced in comparison with 74HCT4066.

FUNCTION TABLE

INPUTS	SWITCH
nE	
L	off
H	on

NOTES:
H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq$ 2.5 ns

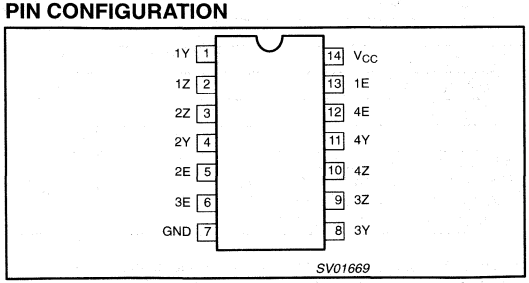
SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn "ON" time: nE to V_{OS}	C_L = 15pF R_L = 1KΩ V_{CC}= 3.3V	10	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time: nE to V_{OS}		13	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1, 2	11	pF
C_S	Maximum switch capacitances		8	pF

NOTES:
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_s = maximum switch capacitance in pF;
   $\sum \{(C_L + C_S) \times V_{CC}^2 \times F_o\}$ = sum of the outputs.
   V_{CC} = supply voltage in V.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4066N	16	DIL	Plastic	SOT27-1
74LV4066D	16	SO	Plastic	SOT108-1
74LV4066DB	16	SSOP	Plastic	SOT337-1
74LV4066PW	16	TSSOP	Plastic	SOT402-1

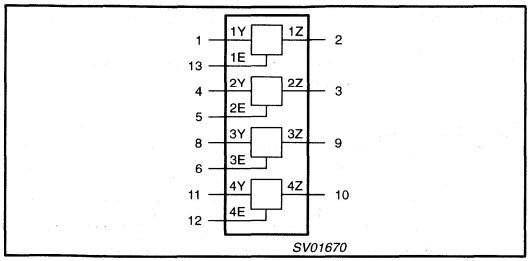
PIN CONFIGURATION



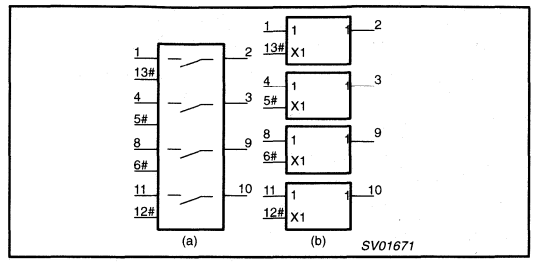
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 8, 11	1Y – 4Y	Independent inputs/outputs
2, 3, 9, 10	1Z – 4Z	Independent inputs/outputs
13, 5, 6, 12	1E to 4E	Enable input (active HIGH)
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

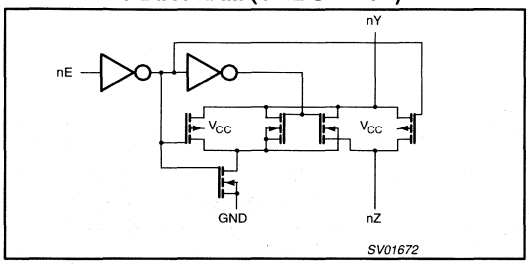
FUNCTIONAL DIAGRAM



IEC LOGIC SYMBOL



SCHEMATIC DIAGRAM (ONE SWITCH)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics –40 –40			+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC switch current	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.90			0.90		V
		V_{CC} = 2.0 V	1.40			1.4		
		V_{CC} = 2.7 to 3.6 V	2.00			2.0		
		V_{CC} = 4.5 V	3.15			3.15		
		V_{CC} = 6.0 V	4.20			4.20		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.30		0.30	V
		V_{CC} = 2.0 V			0.60		0.60	
		V_{CC} = 2.7 to 3.6 V			0.80		0.80	
		V_{CC} = 4.5 V			1.35		1.35	
		V_{CC} = 6.0 V			1.80		1.80	
$\pm I_I$	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND			1.0		1.0	µA
		V_{CC} = 6.0 V; V_I = V_{CC} or GND			2.0		2.0	
$\pm I_S$	Analog switch OFF-state current per channel	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}			1.0		1.0	µA
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}			2.0		2.0	
$\pm I_S$	Analog switch ON-state current per channel	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}			1.0		1.0	µA
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}			2.0		2.0	
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0			20		40	µA
		V_{CC} = 6.0V; V_I = V_{CC} or GND; I_O = 0			40		80	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} − 0.6 V			500		850	µA
R_{ON}	ON-resistance (peak)	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}		300	–		–	Ω
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}		60	130		150	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}		41	60		90	
		V_{CC} = 3.0 to 3.6 V; V_I = V_{IH} or V_{IL}		37	72		83	
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}		25	52		60	
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}		23	47		54	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}		75	–		–	Ω
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}		35	98		115	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}		26	60		68	
		V_{CC} = 3.0 to 3.6 V; V_I = V_{IH} or V_{IL}		24	52		60	
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}		15	40		45	
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}		13	35		40	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}		75	–		–	Ω
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}		40	110		130	
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}		35	72		85	
		V_{CC} = 3.0 to 3.6 V; V_I = V_{IH} or V_{IL}		30	65		75	
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}		22	47		55	
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}		20	40		47	
ΔR_{ON}	Maximum variation of ON-resistance between any two channels	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL}		–				Ω
		V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL}		5				
		V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL}		4				
		V_{CC} = 3.0 to 3.6 V; V_I = V_{IH} or V_{IL}		4				
		V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL}		3				
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}		2				

NOTE:

1. All typical values are measured at T_{amb} = 25°C.
2. At supply voltage approaching 1.2V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

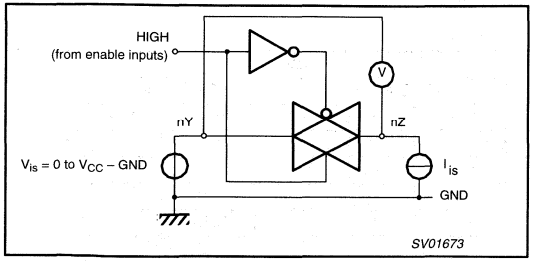


Figure 1. Test circuit for measuring ON-resistance (R_{on}).

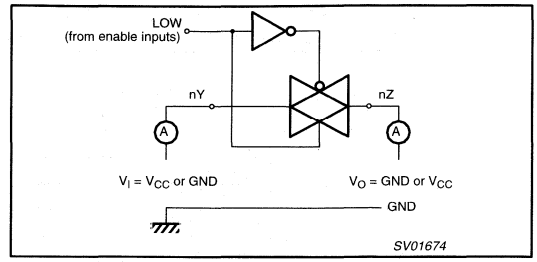


Figure 2. Test circuit for measuring OFF-state current.

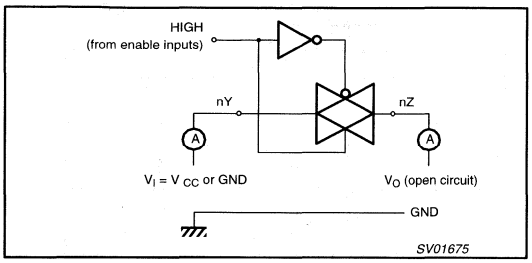


Figure 3. Test circuit for measuring ON-state current.

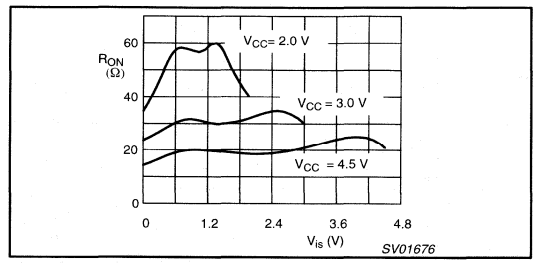


Figure 4. Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to V_{CC} – V_{EE}.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	LIMITS					UNIT	CONDITION	
		–40 to +85 °C			–40 to +125 °C				
		MIN	TYP[1]	MAX	MIN	MAX		V_{CC}(V)	OTHER
t_{PHL}/t_{PLH}	Propagation delay V_{is} to V_{os}		8				ns	1.2	R_L = ∞; C_L = 50 pF Figure 12
			5	26		31		2.0	
			3[2]	15		18		2.7 to 3.6	
			2	13		15		4.5	
			2	10		12		6.0	
t_{PZH}/t_{PZL}	Turn-on time nE to V_{os}		40				ns	1.2	R_L = 1 kΩ; C_L = 50 pF Figures 13 and 14
			22	43		51		2.0	
			12[2]	25		30		2.7 to 3.6	
			10	21		26		4.5	
			8	16		20		6.0	
t_{PHZ}/t_{PLZ}	Turn-off time nE to V_{os}		50				ns	1.2	R_L = 1 kΩ; C_L = 50 pF Figures 13 and 14
			27	65		81		2.0	
			15[2]	38		47		2.7 to 3.6	
			13	32		40		4.5	
			12	28		34		6.0	

NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. All typical values are measured at V_{CC} = 3.3V.

ADDITIONAL AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	TYP	UNIT	V_{CC} (V)	$V_{IS(P-P)}$ (V)	CONDITIONS
	Sine-wave distortion f = 1 kHz	0.04	%	3.0	2.75	R_L = 10 kΩ; C_L = 50 pF Figure 15
		0.02		6.0	5.50	
	Sine-wave distortion f = 10 kHz	0.12	%	3.0	2.75	R_L = 10 kΩ; C_L = 50 pF Figure 15
		0.06		6.0	5.50	
	Switch "OFF" signal feed through	–50	dB	3.0	Note 1	R_L = 600 kΩ; C_L = 50 pF; f=1 MHz Figures 10 and 16
		–50		6.0		
	Crosstalk between any two switches	–60	dB	3.0	Note 1	R_L = 600 kΩ; C_L = 50 pF; f=1 MHz Figure 12
		–60		6.0		
$V_{(p-p)}$	Crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110	mV	3.0		R_L = 600 kΩ; C_L = 50 pF; f=1 MHz (nE, square wave between V_{CC} and GND, $T_r = t_f$ = 6 ns) Figure 13
		220		6.0		
f_{max}	Minimum frequency response (–3 dB)	180	mHz	3.0	Note 2	R_L = 50 kΩ; C_L = 50 pF Figures 11 and 14
		200		6.0		
C_S	Maximum switch capacitance	8	pF			

GENERAL NOTES:

V_{is} is the input voltage at nY or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

NOTES:

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

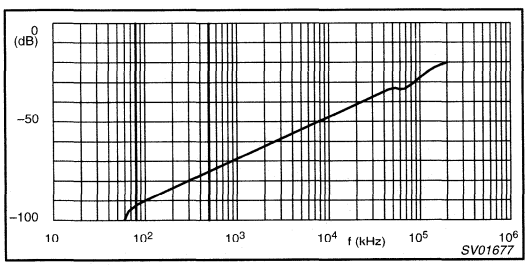


Figure 5. Typical switch "OFF" signal feed-through as a function of frequency.

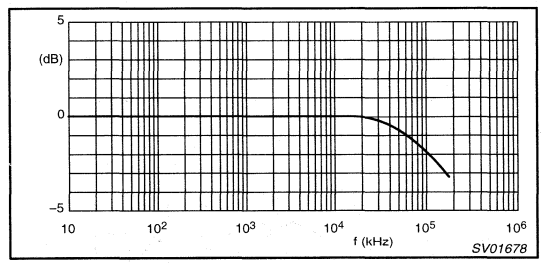


Figure 6. Typical frequency response.

NOTES TO FIGURES 5 AND 6:

Test conditions: V_{CC} = 3.0 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1kΩ.

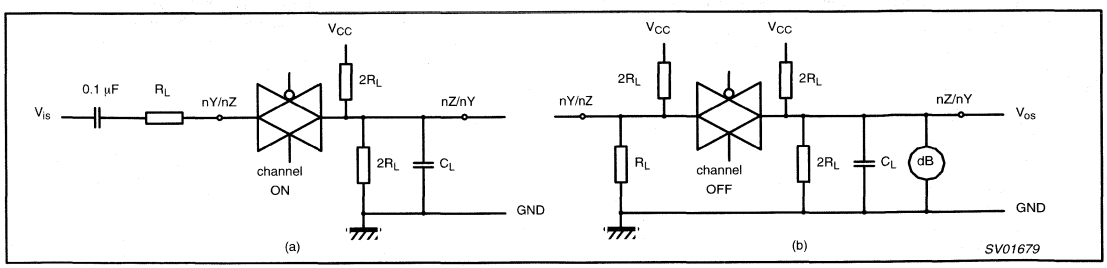


Figure 7. Test circuit for measuring crosstalk between any two switches. (a) channel ON condition; (b) channel OFF condition.

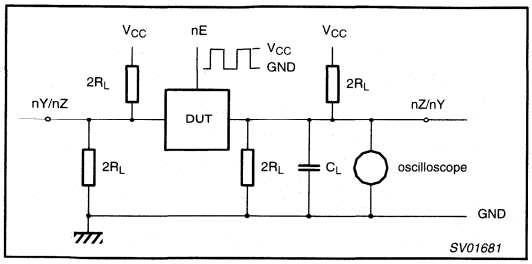


Figure 8. Test circuit for measuring crosstalk between control and any switch.

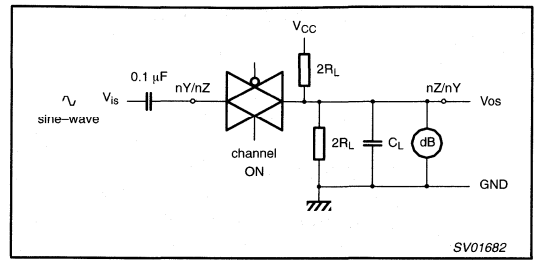
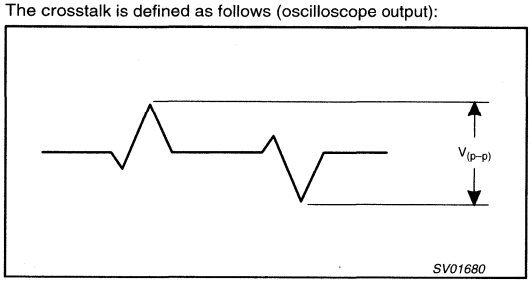


Figure 9. Test circuit for measuring minimum frequency response.

NOTE TO FIGURE 8:
The crosstalk is defined as follows (oscilloscope output):



NOTE TO FIGURE 9:
Adjust input voltage to obtain 0 dBm at V_{OS} when F_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of –3 dB at V_{OS}.

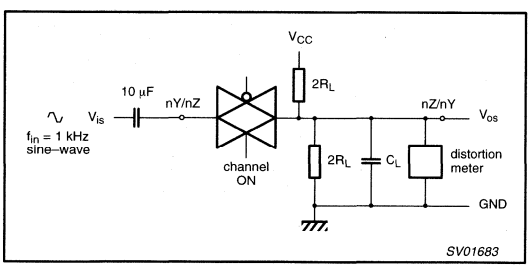


Figure 10. Test circuit for measuring sine-wave distortion.

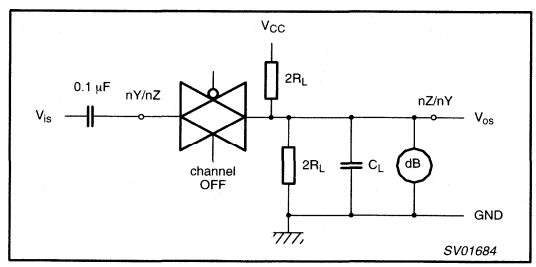


Figure 11. Test circuit for measuring switch "OFF" signal feed-through.

WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
$V_M = 0.5 \times V_{CC}$ at $V_{CC} \leq$ 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} <$ 2.7 V
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH} - 0.1 \times V_{CC}$ $V_{CC} <$ 2.7 V

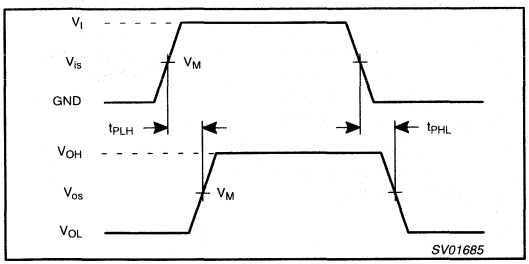


Figure 12. Input (V_{IS}) to output (V_{OS}) propagation delays.

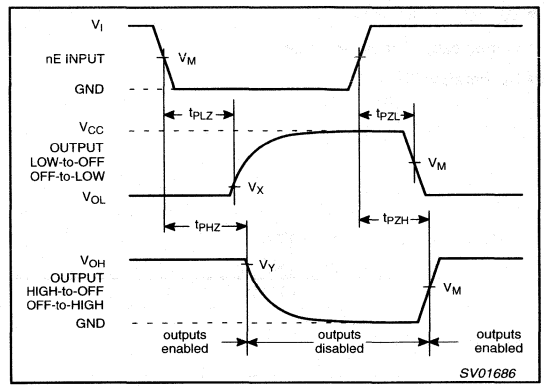
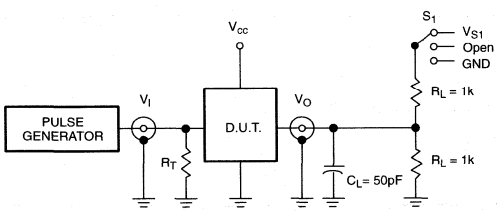
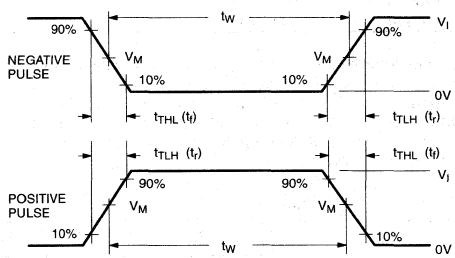


Figure 13. Turn-on and turn-off times for the inputs (nS, $\overline{E}$) to the output (V_{OS}).

TEST CIRCUIT



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{S1}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_{S1}
< 2.7V	V_{CC}	2 * V_{CC}
2.7–3.6V	2.7V	2 * V_{CC}
≥ 4.5 V	V_{CC}	2 * V_{CC}

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SY00044

Figure 14. Load circuitry for switching times.

16-channel analog multiplexer/demultiplexer 74LV4067

FEATURES

- Optimized for low voltage applications: 1.0 to 6.0 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Low typ "ON" resistance:
  60 Ω at V_{cc} – GND = 4.5 V
  90 Ω at V_{cc} – GND = 3.0 V
  145 Ω at V_{cc} – GND = 2.0 V
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4067 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT4067.

The 74LV4067 is an 16-channel analog multiplexer/demultiplexer with four address inputs (S_o to S_3), an active LOW enable input ($\overline{E}$), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

The 74LV4067 contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the sixteen switches is selected (low impedance ON–state) by S_0 to S_3. All unselected switches are in the high impedance OFF-state. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 to S_3.

The analog inputs/outputs (Y_0 to Y_{15}, and Z) can swing between V_{cc} as a positive limit and GND as a negative limit.
Vcc – GND may not exceed 6.0 V.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn "ON" time $\overline{E}$ to V_{OS} S_n to V_{OS}	C_L = 15 pF R_L = 1KΩ V_{CC} = 3.3 V	 25 27	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time $\overline{E}$ to V_{OS} S_n to V_{OS}		 25 27	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	See Notes 1 and 2	29	pF
C_S	Maximum switch capacitance independent (Y) common (Z)		5 45	pF

NOTE:

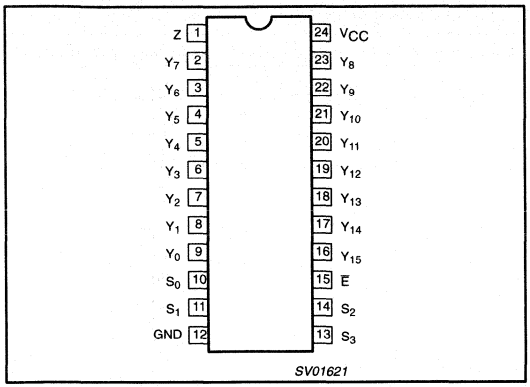
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; C_S = max. switch capacitance in pF; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic DIL	–40°C to +125°C	74LV4067 N	74LV4067 N	SOT101-1
24-Pin Plastic SO	–40°C to +125°C	74LV4067 D	74LV4067 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +125°C	74LV4067 DB	74LV4067 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV4067 PW	74LV4067PW DH	SOT355-1

16-channel analog multiplexer/demultiplexer 74LV4067

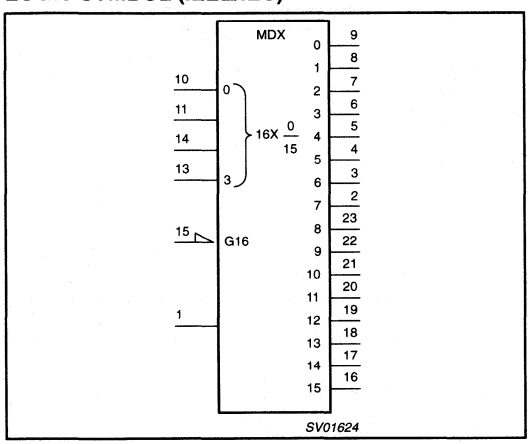
PIN CONFIGURATION



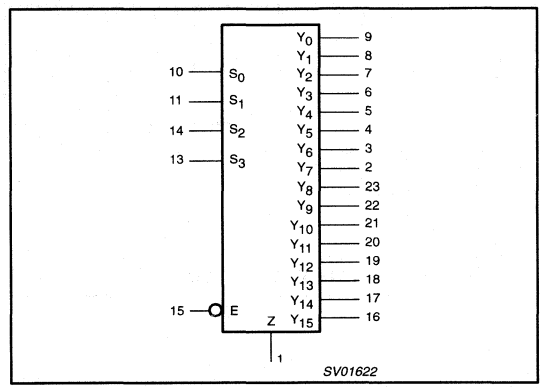
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	Z	Common input/output
9, 8, 7, 6, 5, 4, 3, 2, 23, 22, 21, 20, 19, 18, 17, 16	Y_0 to Y_{15}	Independent inputs/outputs
10, 11, 14, 13	S_0 to S_3	Select inputs
12	GND	Ground (0 V)
15	$\overline{E}$	Enable input (active LOW)
24	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL

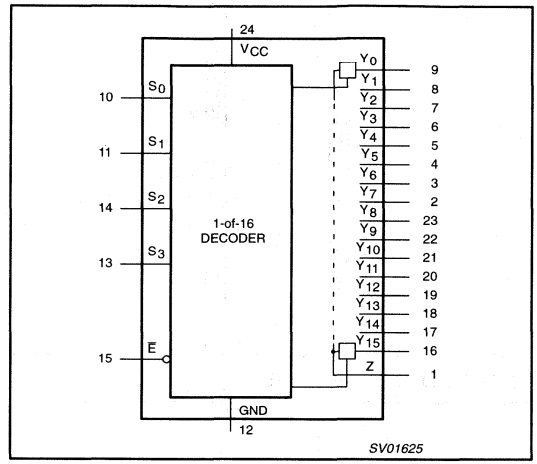


FUNCTION TABLE

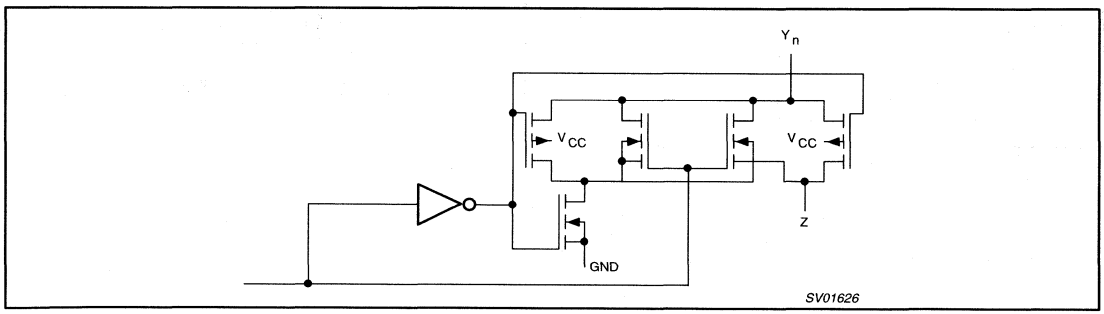
INPUTS					CHANNEL ON
$\overline{E}$	S_3	S_2	S_1	S_0	
L	L	L	L	L	$Y_0 - Z$
L	L	L	L	H	$Y_1 - Z$
L	L	L	H	L	$Y_2 - Z$
L	L	L	H	H	$Y_3 - Z$
L	L	H	L	L	$Y_4 - Z$
L	L	H	L	H	$Y_5 - Z$
L	L	H	H	L	$Y_6 - Z$
L	L	H	H	H	$Y_7 - Z$
L	H	L	L	L	$Y_8 - Z$
L	H	L	L	H	$Y_9 - Z$
L	H	L	H	L	$Y_{10} - Z$
L	H	L	H	H	$Y_{11} - Z$
L	H	H	L	L	$Y_{12} - Z$
L	H	H	L	H	$Y_{13} - Z$
L	H	H	H	L	$Y_{14} - Z$
L	H	H	H	H	$Y_{15} - Z$
H	X	X	X	X	None

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

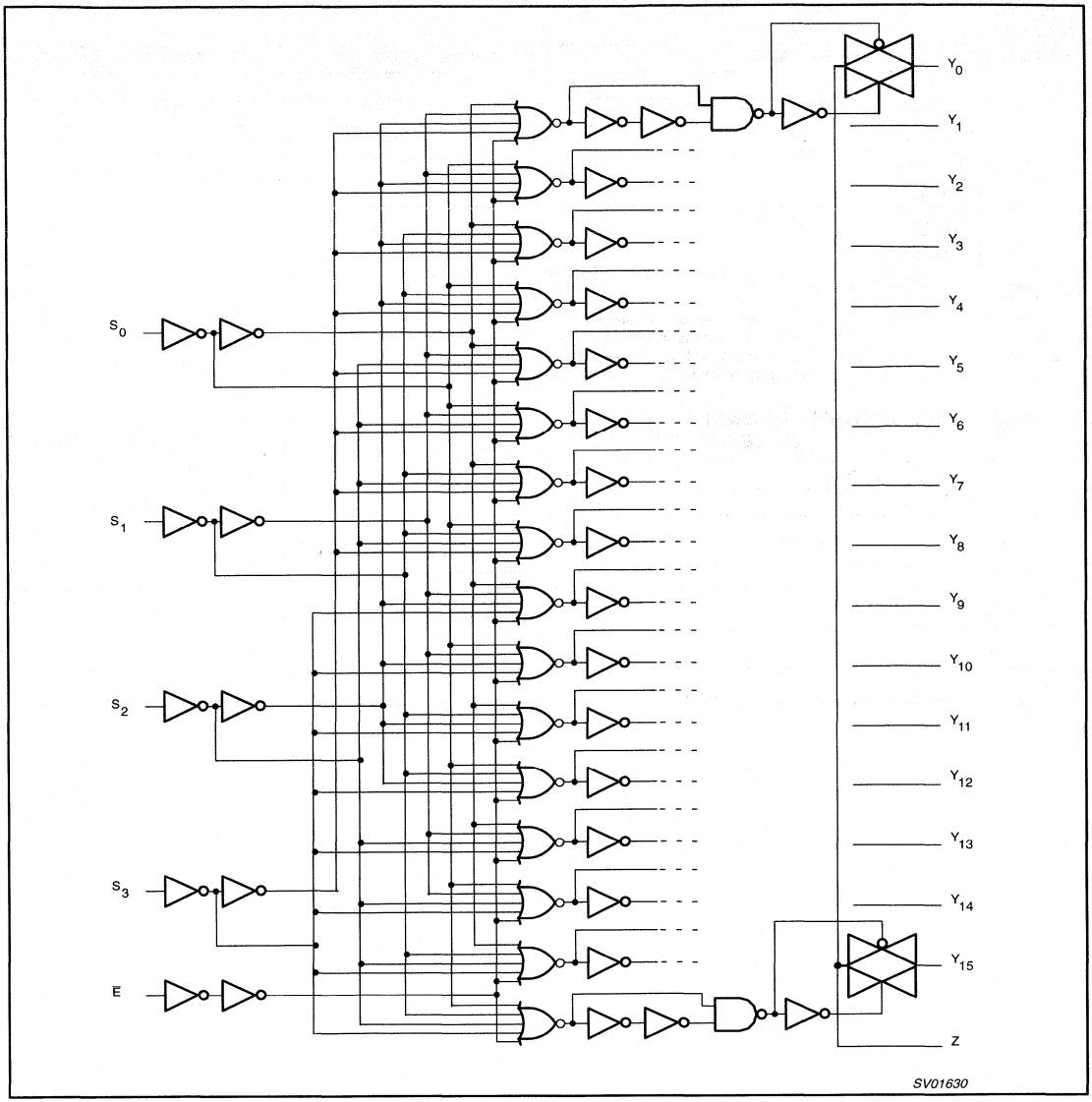
FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM (ONE SWITCH)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V	20	mA
$\pm I_{SK}$	DC switch diode current	$V_S < -0.5$ or $V_S > V_{CC} + 0.5$ V	20	mA
$\pm I_S$	DC switch current	-0.5 V $< V_S < V_{CC} + 0.5$ V	25	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1 and Figure 5	1.0	3.3	6.0	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0 V to 2.0 V V_{CC} = 2.0 V to 2.7 V V_{CC} = 2.7 V to 6.0 V	– – –	– – –	500 200 100	ns/V

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 6.0 V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				-40°C to +85°C			-40°C to +125°C		
				MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V		0.9			0.9		V
		V_{CC} = 2.0 V		1.4			1.4		
		V_{CC} = 2.7 to 3.6 V		2.0			2.0		
		V_{CC} = 4.5 V		3.15			3.15		
		V_{CC} = 6.0 V		4.20			4.20		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V				0.3		0.3	V
		V_{CC} = 2.0 V				0.6		0.6	
		V_{CC} = 2.7 to 3.6 V				0.8		0.8	
		V_{CC} = 4.5 V				1.35		1.35	
		V_{CC} = 6.0 V				1.80		1.80	
$\pm I_I$	Input leakage current	V_{CC} = 3.6	V_I = V_{CC} or GND			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
$\pm I_S$	Analog switch OFF-state current per channel	V_{CC} = 3.6	V_I = V_{IH} or V_{IL}; $\lvert V_S \rvert$ = V_{CC} - GND (See Figure 2)			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
$\pm I_S$	Analog switch ON-state current	V_{CC} = 3.6	V_I = V_{IH} or V_{IL}; $\lvert V_S \rvert$ = V_{CC} - GND (See Figure 3)			1.0		1.0	µA
		V_{CC} = 6.0				2.0		2.0	
I_{CC}	Quiescent supply current	V_{CC} = 3.6 V	V_I = V_{CC} or GND; V_{IS} = GND or V_{CC}; V_{OS} = V_{CC} or GND			20.0		40	µA
		V_{CC} = 6.0 V				40.0		80	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 to 3.6 V	V_I = V_{CC} – 0.6 V			500		850	µA
R_{ON}	ON-resistance (peak)	V_{CC} = 1.2 V	V_I = V_{IH} or V_{IL}; I_S = 100 µA; V_{IS} = V_{CC} to GND						Ω
		V_{CC} = 2.0 V	V_I = V_{IH} or V_{IL}; I_S = 1000 µA; V_{IS} = V_{CC} to GND		145	325		375	
		V_{CC} = 2.7 V			90	200		235	
		V_{CC} = 3.0 to 3.6 V			80	180		210	
		V_{CC} = 4.5 V			60	135		160	
		V_{CC} = 6.0 V			55	125		145	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V	V_I = V_{IH} or V_{IL}; I_S = 100 µA; V_{IS} = GND		225				Ω
		V_{CC} = 2.0 V	V_I = V_{IH} or V_{IL}; I_S = 1000 µA; V_{IS} = GND		110	235		270	
		V_{CC} = 2.7 V			70	145		165	
		V_{CC} = 3.0 to 3.6 V			60	130		150	
		V_{CC} = 4.5 V			45	100		115	
		V_{CC} = 6.0 V			40	85		100	

NOTES:

1. All typical values are measured at T_{amb} = 25°C.
2. At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
3. R_{ON} (MAX) data is preliminary.

DC ELECTRICAL CHARACTERISTICS (*Continued*)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				-40°C to +85°C			-40°C to +125°C		
				MIN	TYP[1]	MAX	MIN	MAX	
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V	$V_I = V_{IH}$ or V_{IL}; I_S = 100 μA; $V_{IS} = V_{CC}$		250				Ω
		V_{CC} = 2.0 V	$V_I = V_{IH}$ or V_{IL}; I_S = 1000 μA; $V_{IS} = V_{CC}$		120	320		370	Ω
		V_{CC} = 2.7 V			75	195		225	
		V_{CC} = 3.0 to 3.6 V			70	175		205	
		V_{CC} = 4.5 V			50	130		150	
		V_{CC} = 6.0 V			45	120		135	
ΔR_{ON}	Maximum variation of ON-resistance between any two channels	V_{CC} = 1.2 V	$V_I = V_{IH}$ or V_{IL}; $V_{IS} = V_{CC}$ to GND						Ω
		V_{CC} = 2.0 V			5				
		V_{CC} = 2.7 V			4				
		V_{CC} = 3.0 to 3.6 V			4				
		V_{CC} = 4.5 V			3				
		V_{CC} = 6.0 V			2				

NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
3. R_{ON} (MAX) data is preliminary.

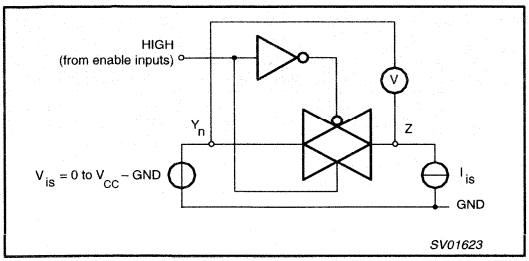


Figure 1. Test circuit for measuring ON-resistance (R_{ON}).

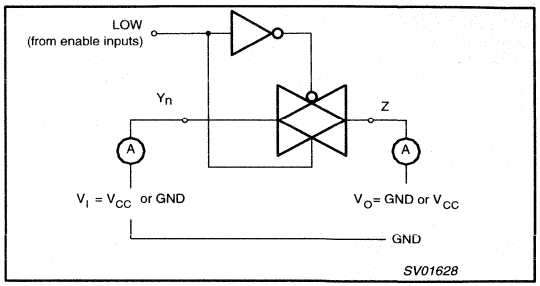


Figure 2. Test circuit for measuring OFF-state current.

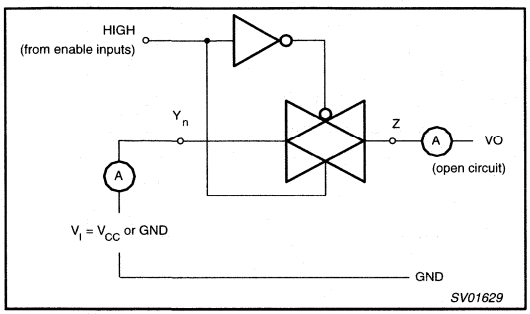


Figure 3. Test circuit for measuring ON-state current.

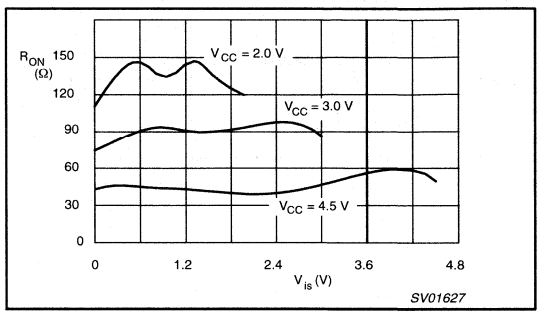


Figure 4. Typical ON-resistance (R_{on}) as a function of input voltage (V_{is} for V_{is} = 0 to V_{CC} – GND.

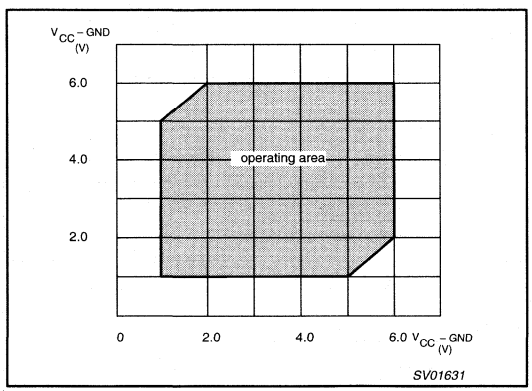


Figure 5. Guaranteed operating area as a function of the supply voltages.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF

SYMBOL	PARAMETER	CONDITION		LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
		V_{CC} (V)	OTHER	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay V_{is} to V_{os} Z to Y_n	1.2	$R_L = \infty$; $C_L = 50$ pF Figure 13		30				ns
		2.0			10	19		24	
		2.7			8	14		18	
		3.0 to 3.6			6[2]	11		14	
		4.5			5	9		12	
		6.0			4	7		9	
t_{PHL}/t_{PLH}	Propagation delay V_{is} to V_{os} Y_n to Z	1.2	$R_L = \infty$; $C_L = 50$ pF Figure 13		45				ns
		2.0			15	31		36	
		2.7			11	23		26	
		3.0 to 3.6			9[2]	18		21	
		4.5			8	15		18	
		6.0			6	12		14	
t_{PZH}/t_{PZL}	Turn-on time $\overline{E}$ to Y_n	1.2	$R_L = 1$kΩ $C_L = 50$ pF Figures 14 and 15		145				ns
		2.0			49	94		112	
		2.7			36	69		86	
		3.0 to 3.6			28[2]	55		66	
		4.5			25	47		56	
		6.0			19	38		43	
t_{PZH}/t_{PZL}	Turn-on time Z to Y_n	1.2	$R_L = 1$kΩ $C_L = 50$ pF Figures 14 and 15		160				ns
		2.0			54	102		122	
		2.7			40	75		94	
		3.0 to 3.6			30[2]	60		72	
		4.5			27	51		61	
		6.0			21	39		47	
t_{PHZ}/t_{PLZ}	Turn-off time $\overline{E}$ to Y_n	1.2	$R_L = 1$kΩ $C_L = 50$ pF Figures 14 and 15		125				ns
		2.0			43	80		95	
		2.7			33	59		71	
		3.0 to 3.6			26[2]	48		57	
		4.5			23	41		49	
		6.0			18	32		38	
t_{PHZ}/t_{PLZ}	Turn-off time Sn to Y_n	1.2	$R_L = 1$kΩ $C_L = 50$ pF Figures 14 and 15		140				ns
		2.0			49	90		109	
		2.7			37	67		81	
		3.0 to 3.6			29[2]	54		65	
		4.5			26	46		56	
		6.0			20	36		43	

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS (Continued)

GND = 0 V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF

SYMBOL	PARAMETER	CONDITION		–40 to +85 °C			–40 to +125 °C		UNIT
		V_{CC} (V)	OTHER	MIN	TYP[1]	MAX	MIN	MAX	
t_{PZH}/t_{PZL}	Turn-on time $\overline{E}$ to Z	1.2	$R_L = 1k\Omega$, $C_L = 50$ pF, Figures 14 and 15		145				ns
		2.0			51	93		110	
		2.7			39	70		83	
		3.0 to 3.6			29[2]	56		66	
		4.5			26	48		56	
		6.0			20	36		43	
t_{PZH}/t_{PZL}	Turn-on time S_n to Y_n	1.2	$R_L = 1k\Omega$, $C_L = 50$ pF, Figures 14 and 15		170				ns
		2.0			58	109		131	
		2.7			42	80		96	
		3.0 to 3.6			32[2]	64		77	
		4.5			29	54		65	
		6.0			21	42		50	
t_{PHZ}/t_{PLZ}	Turn-off time $\overline{E}$ to Z	1.2	$R_L = 1k\Omega$, $C_L = 50$ pF, Figures 14 and 15		145				ns
		2.0			51	93		110	
		2.7			38	69		82	
		3.0 to 3.6			30[2]	56		66	
		4.5			29	48		56	
		6.0			21	37		44	
t_{PHZ}/t_{PLZ}	Turn-off time S_n to Y_n	1.2	$R_L = 1k\Omega$, $C_L = 50$ pF, Figures 14 and 15		160				ns
		2.0			56	104		124	
		2.7			42	77		92	
		3.0 to 3.6			32[2]	62		74	
		4.5			29	53		61	
		6.0			23	41		49	

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

ADDITIONAL AC CHARACTERISTICS

Recommended conditions and typical values
GND = 0 V; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	TYP.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	Sine-wave distortion f = 1 kHz	0.80 0.40	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pf Figures 10 and 11
	Sine-wave distortion f = 10 kHz	2.40 1.20	%	3.0 6.0	2.75 5.50	R_L = 10 kΩ; C_L = 50 pf Figures 10 and 11
	Switch "OFF" signal feed through	–50 –50	dB	3.0 6.0	Note 1	R_L = 600 Ω; C_L = 50 pf; f= 1 MHz Figures 6 and 12
	Crosstalk between any two switches/multiplexers	–60 –60	dB	3.0 6.0	Note 1	R_L = 600 Ω; C_L = 50 pf; f= 1 MHz Figure 8
$V_{(p-p)}$	Crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 120	mV	3.0 6.0		R_L = 600 Ω; C_L = 50 pf; f= 1 MHz (S_n or $\overline{E}$, square wave between V_{CC} and GND $t_r = t_f$ = 6 ns) Figure 9
f_{max}	Minimum frequency response (–3 dB)	180 200	MHz	3.0 6.0	Note 2	R_L = 50 Ω; C_L = 50 pF Figures 7 and 10
C_S	Maximum switch capacitance	5	pf			

GENERAL NOTES:

V_{is} is the input voltage at nY or Z terminal, whichever is assigned as an input.
V_{OS} is the output voltage at nY or Z terminal, whichever is assigned as an output.

NOTES:

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50 Ω).

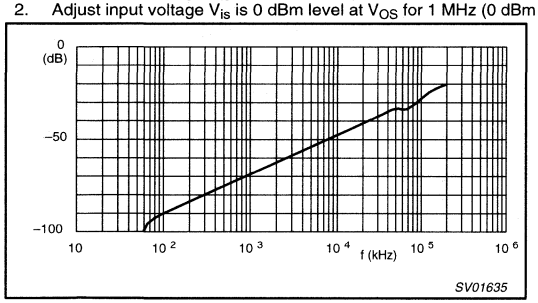


Figure 6. Typical switch "OFF" signal feed-through as a function of frequency.

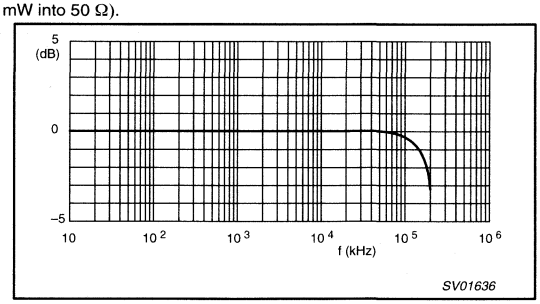


Figure 7. Typical frequency response.

NOTES TO FIGURES 6 AND 7:

Test conditions: V_{CC} = 3.0 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1kΩ.

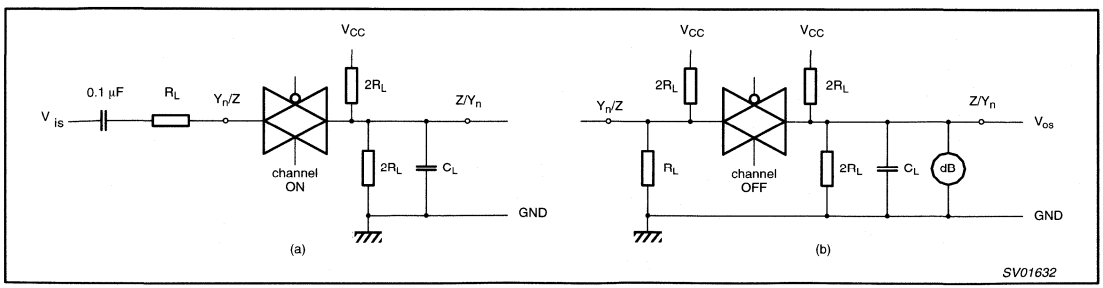
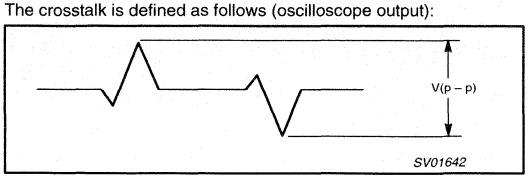


Figure 8. Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

NOTE TO FIGURE 9:
The crosstalk is defined as follows (oscilloscope output):



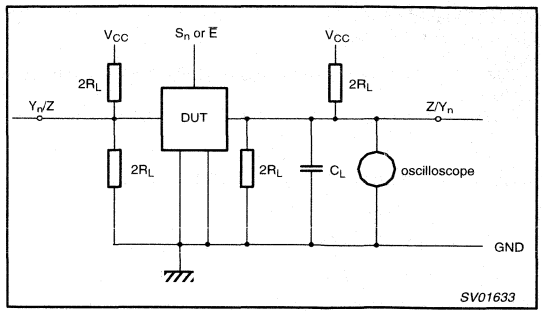


Figure 9. Test circuit for measuring crosstalk between control and any switch.

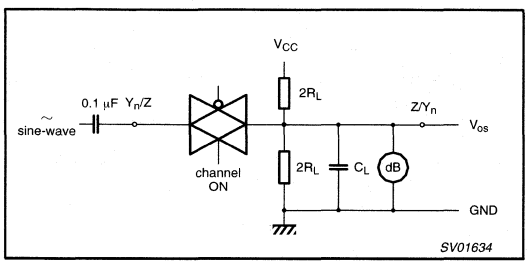


Figure 10. Test circuit for measuring minimum frequency response.

NOTE TO FIGURE 10:
Adjust input voltage to obtain 0 dBm at V_{OS} when F_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of –3 dB at V_{OS}.

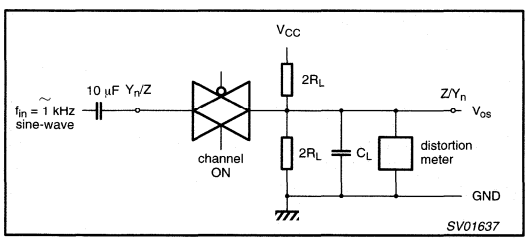


Figure 11. Test circuit for measuring sine-wave distortion.

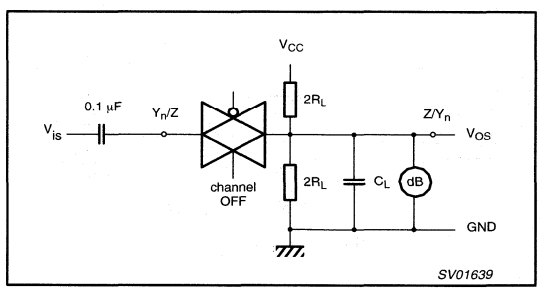


Figure 12. Test circuit for measuring switch "OFF" signal feed-through.

WAVEFORMS

V_M = 1.5 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_M = 0.5 × V_{CC} at 2.7 V > V_{CC} > 3.6 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
V_X = V_{OL} + 0.3 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_X = V_{OL} + 0.1 × V_{CC} at 2.7 V >V_{CC} > 3.6 V
V_Y = V_{OH} − 0.3 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_Y = V_{OH} − 0.1 × V_{CC} at 2.7 V >V_{CC} > 3.6 V

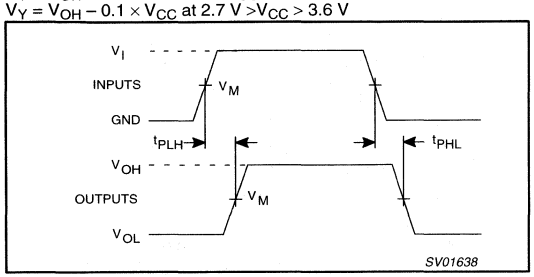


Figure 13. Input (V_{is}) to output (V_{os}) propagation delays.

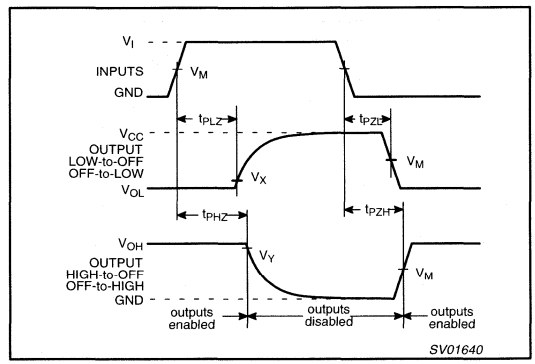
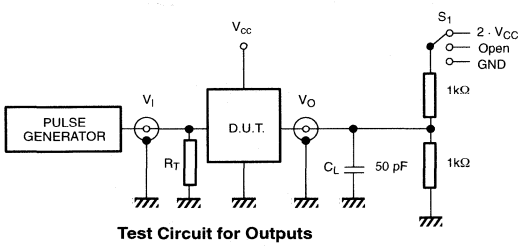
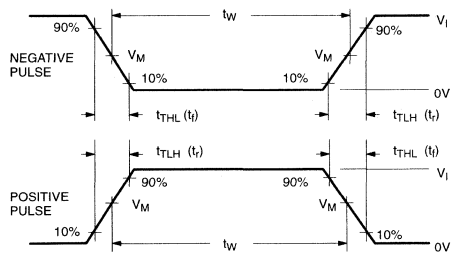


Figure 14. Turn-on and turn-off times for the inputs (S_n, $\overline{E}$) to the output (V_{os}).

TEST CIRCUIT



Test Circuit for Outputs



V_{CC}	V_I
< 2.7V	V_{CC}
2.7 - 3.6V	2.7V
> 3.6 V	V_{CC}

Test	S_1	V_{IS}
t_{PLH}/t_{PHL}	Open	Pulse
t_{PLZ}/t_{PZL}	2 · V_{CC}	GND
t_{PHZ}/t_{PZH}	GND	V_I

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance
R_L = load resistor

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

t_r = t_f =6ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

SY01740

Figure 15. Load circuitry for switching times.

8-stage shift-and-store bus register | 74LV4094

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Output capability: standard
- I_{CC} category: MSI

Applications:

- Serial-to-parallel data conversion
- Remote control holding register

DESCRIPTION

The 74LV4094 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT4094.

The 74LV4094 is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-State outputs (QP_0 to OP_7). The parallel outputs may be connected directly to the common bus lines. Data is shifted on the positive-going clock (CP) transitions. The data in each shift register is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH. Two serial outputs (QS_1 and QS_2) are available for cascading a number of 74LV4094 devices. Data is available at QS_1 on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at QS_2 on the next negative going clock edge and is for cascading 74LV4094 devices when the clock rise time is slow.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to QS_1 CP to QS_2 CP to QP_n STR to QP_n	C_L = 15 pF; V_{CC} = 3.3 V	 14 13 18 17	ns
f_{MAX}	Maximum clock frequency		95	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	83	pF

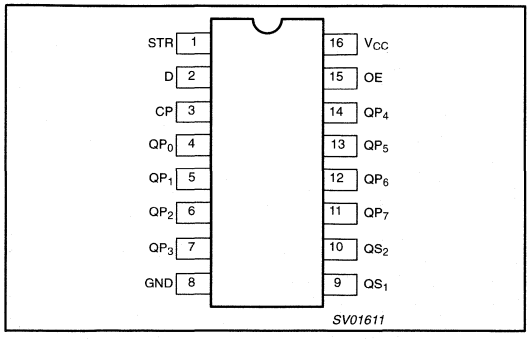
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV4094 N	74LV4094 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV4094 D	74LV4094 D	SOT109-1

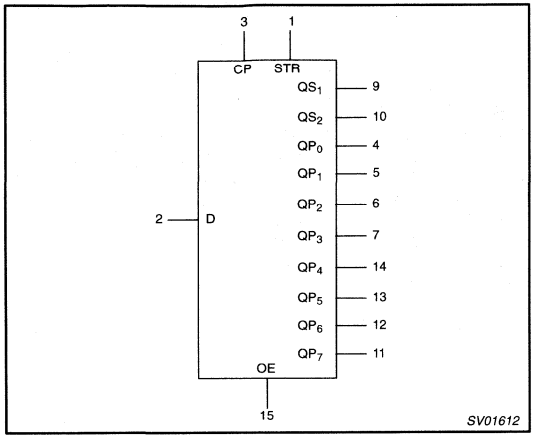
PIN CONFIGURATION



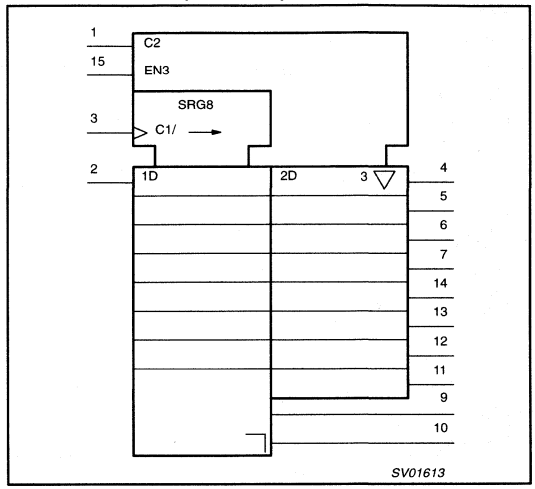
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	STR	Strobe input
2	D	Serial input
3	CP	Clock input
4, 5, 6, 7, 14, 13, 12, 11	QP_0 to QP_7	Parallel outputs
8	GND	Ground (0 V)
9, 10	QS_1, QS_2	Serial outputs
15	OE	Output enable input
16	V_{CC}	Positive supply voltage

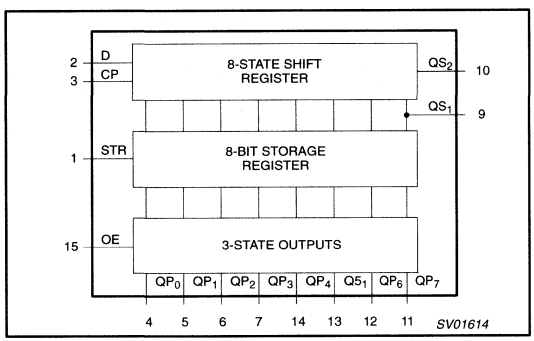
LOGIC SYMBOL



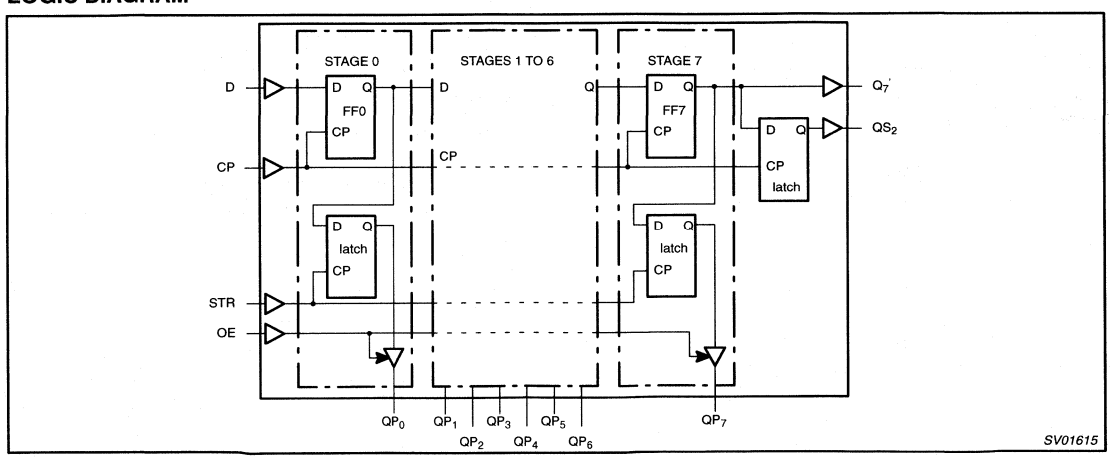
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



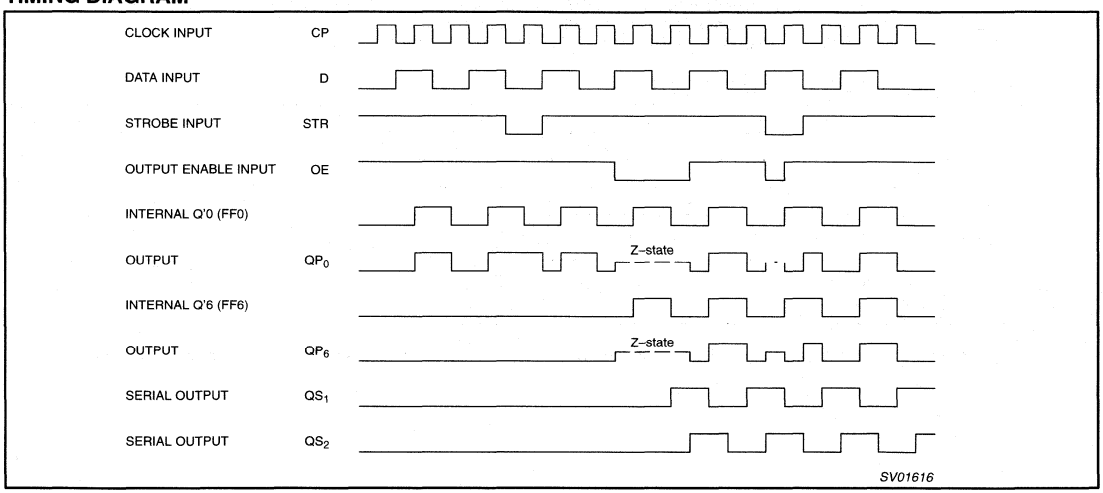
FUNCTION TABLE

INPUTS				PARALLEL OUTPUT		SERIAL OUTPUTS	
CP	OE	STR	D	QP_0	QP_n	QS_1	QS_2
↑	L	X	X	Z	Z	Q'_6	NC
↓	L	X	X	Z	Z	NC	QP_7
↑	H	L	X	NC	NC	Q'_6	NC
↑	H	H	L	L	QP_{n-1}	Q'_6	NC
↑	H	H	H	H	QP_{n-1}	Q'_6	NC
↓	H	H	H	NC	NC	NC	QP_7

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state
NC = no change

↑ = LOW-to–HIGH CP transition
↓ = HIGH-to-LOW CP transition
Q'_6 = the information in the 8^{th} register stage is transferred to the 8^{th} register stage and QS_n clock edge.

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	V_{CC}	0.6		V_{CC}		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V		0.4	GND		GND	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
I_I	Input leakage current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6 V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND			5		10	µA
I_{CC}	Quiescent supply current; SSI	V_{CC} = 3.6; $V_I = V_{CC}$ or GND; I_O = 0			20.0		40	µA
I_{CC}	Quiescent supply current; flip-flops	V_{CC} = 3.6; $V_I = V_{CC}$ or GND; I_O = 0			20.0		80	µA
	Quiescent supply current; MSI	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	µA
	Quiescent supply current; LSI	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0			500		1000	
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V			500		850	µA

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC} (V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay CP to QS_1		1.2		90				ns
			2.0		31	58		70	
			2.7		23	43		51	
			3.0 to 3.6		17[2]	34		41	
t_{PHL}/t_{PLH}	Propagation delay CP to QS_2		1.2		80				ns
			2.0		27	51		61	
			2.7		20	38		45	
			3.0 to 3.6		14[2]	30		36	
t_{PHL}/t_{PLH}	Propagation delay CP to QP_n		1.2		115				ns
			2.0		39	75		90	
			2.7		29	55		66	
			3.0 to 3.6		22[2]	44		53	
t_{PHL}/t_{PLH}	Propagation delay STR to QP_n		1.2		105				ns
			2.0		36	68		82	
			2.7		26	50		60	
			3.0 to 3.6		20[2]	40		48	
t_{PZH}/t_{PZL}	3-State Output enable time OE to QP_n		1.2		100				ns
			2.0		34	65		77	
			2.7		25	48		56	
			3.0 to 3.6		19[2]	38		45	
t_{PHZ}/t_{PLZ}	3-State Output disable time OE to QP_n		1.2		65				ns
			2.0		24	40		49	
			2.7		18	32		37	
			3.0 to 3.6		14[2]	26		30	
t_w	Clock pulse width HIGH or LOW		2.0	34	9		41		ns
			2.7	25	6		30		
			3.0 to 3.6	20	5[2]		24		
t_w	Strobe pulse width; HIGH		2.0	34	9		41		ns
			2.7	25	6		30		
			3.0 to 3.6	20	5[2]		24		
t_{su}	Set-up time D to CP		1.2		25				ns
			2.0	22	9		26		
			2.7	16	6		19		
			3.0 to 3.6	13	5[2]		15		
t_{su}	Set-up time CP to STR		1.2		50				ns
			2.0	43	17		51		
			2.7	31	13		38		
			3.0 to 3.6	25	10[2]		30		
T_h	Hold time D to CP		1.2		–10				ns
			2.0	5	–4		5		
			2.7	5	–3		5		
			3.0 to 3.6	5	–22		5		

NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC CHARACTERISTICS (Continued)

GND = 0 V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF

SYMBOL	PARAMETER	WAVEFORM	CONDITION	–40 to +85 °C			–40 to +125 °C		UNIT
			V_{CC} (V)	MIN	TYP[1]	MAX	MIN	MAX	
T_h	Hold time D to STR		1.2		–25				ns
			2.0	5	–9		5		
			2.7	5	–6		5		
			3.0 to 3.6	5	–5[2]		5		
f_{max}	Maximum clock pulse frequency		2.0	14	52		12		MHz
			2.7	19	70		16		
			3.0 to 3.6	24	87[2]		20		

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ ς
$V_Y = V_{OH} \pm 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} \pm 0.1 \times V_{CC}$ at $V_{CC} < 2.7$V

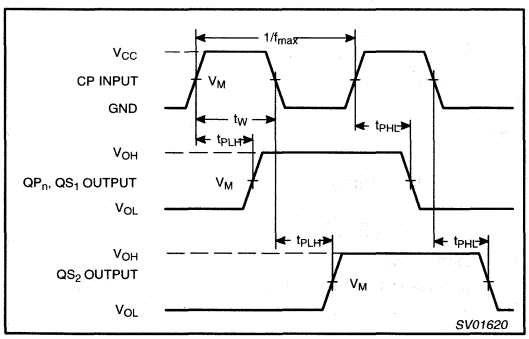


Figure 1. Clock (CP) to output (QP_n, QS_1, QS_2) propagation delays, the clock pulse width and the maximum clock frequency.

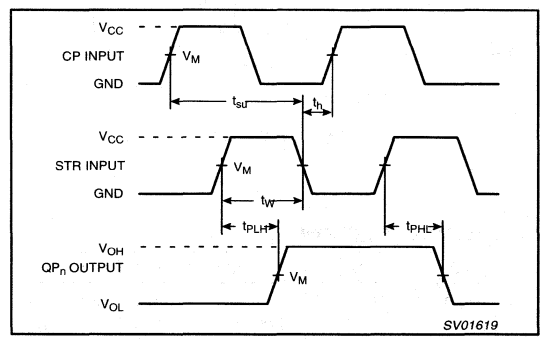


Figure 2. Strobe (STR) to output (QP_n) propagation delays and the strobe pulse width and the clock set-up and hold times for strobe input.

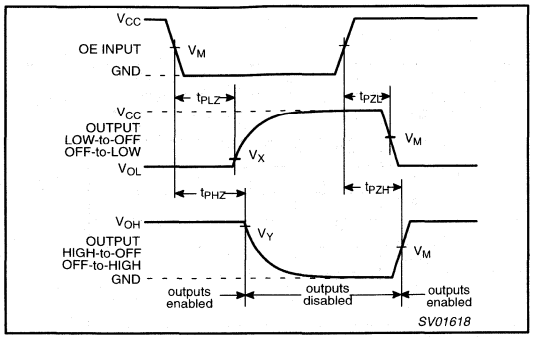


Figure 3. 3-State enable and disable times for input OE.

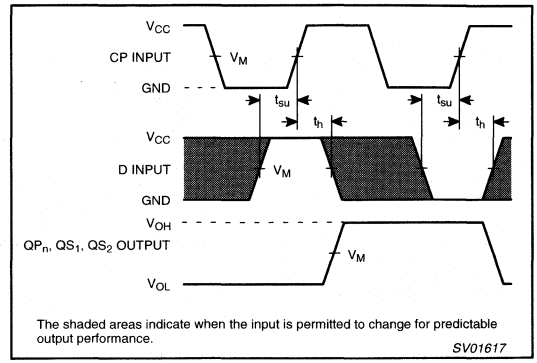
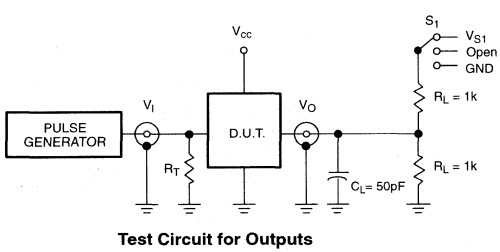
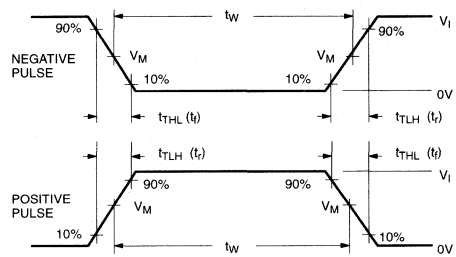


Figure 4. Data set-up and hold times for the data input (D).

TEST CIRCUIT



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{S1}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_{S1}
< 2.7V	V_{CC}	2 * V_{CC}
2.7–3.6V	2.7V	2 * V_{CC}
≥ 4.5 V	V_{CC}	2 * V_{CC}

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SY00044

Figure 5. Load circuitry for switching times.

Quad bilateral switches | 74LV4316

FEATURES

- Optimized for Low Voltage applications: 1.0V to 6.0V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Low typ "ON" resistance:
  80Ω at V_{CC} – VEE = 4.5V
  120Ω at V_{CC} – VEE = 3.0V
  295Ω at V_{CC} – VEE = 2.0V
- Logic level translation: to enable 3V logic to communicate with ±3V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4316 is a low-voltage CMOS device that is pin and function compatible with 74HC/HCT4316.

The 74LV4316 has four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (nS). When the enable input ($\overline{E}$) is HIGH, all four analog switches are turned off.

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{CC} > (V_Y, V_Z) > V_{EE}$. Inputs nY and nZ are electrically equivalent terminals. V_{CC} and GND are the supply voltage pins for the digital control inputs ($\overline{E}$ and nS). The V_{CC} to GND ranges are 1.0 to 6.0 V.

The analog inputs/outputs (nY and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit.

$V_{CC} - V_{EE}$ may not exceed 6.0 V.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq$ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	Turn "ON" time: $\overline{E}$ to V_{OS} nS to V_{OS}	C_L = 15pF R_L = 1KΩ V_{CC}= 3.3V	19	ns
t_{PHZ}/t_{PLZ}	Turn "OFF" time: $\overline{E}$ to V_{OS} nS to V_{OS}		20	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per switch	Notes 1, 2	13	pF
C_S	Maximum switch capacitance		5	pF

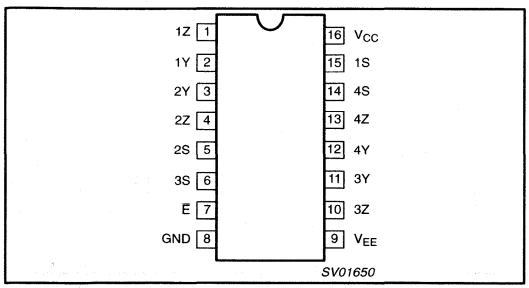
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   V_{CC} = supply voltage in V:
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV4316 N	74LV4316 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV4316 D	74LV4316 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV4316 DB	74LV4316 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV4316 PW	74LV4316PW DH	SOT403-1

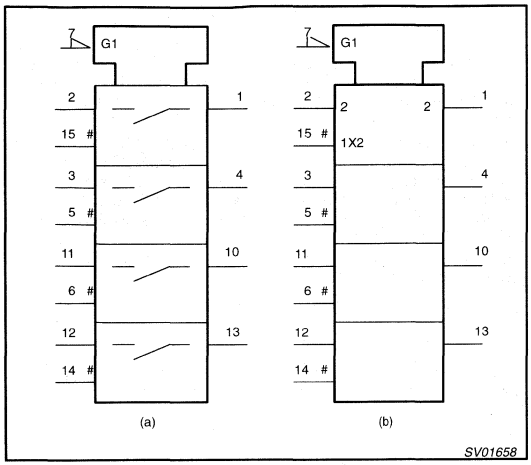
PIN CONFIGURATION



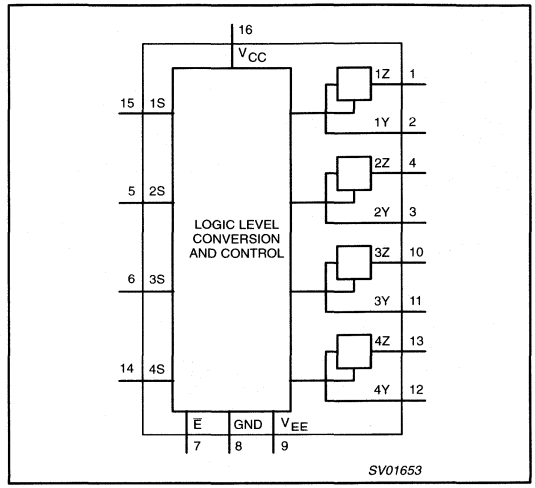
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 10, 13	1Z – 4Z	Independent inputs/outputs
2, 3, 11, 12	1Y – 4Y	Independent inputs/outputs
7	$\overline{E}$	Enable input (active LOW)
8	GND	Ground (0V)
9	V_{EE}	Negative supply voltage
15, 5, 6, 14	1S – 4S	Select inputs (active HIGH)
16	V_{CC}	Positive supply voltage

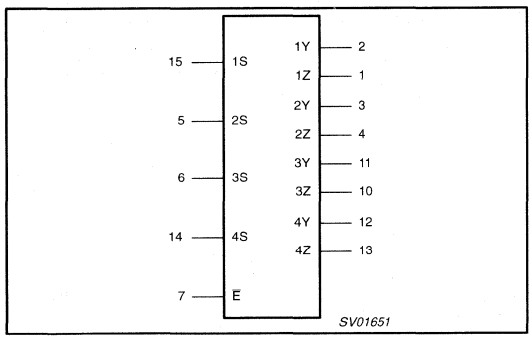
IEC LOGIC SYMBOL



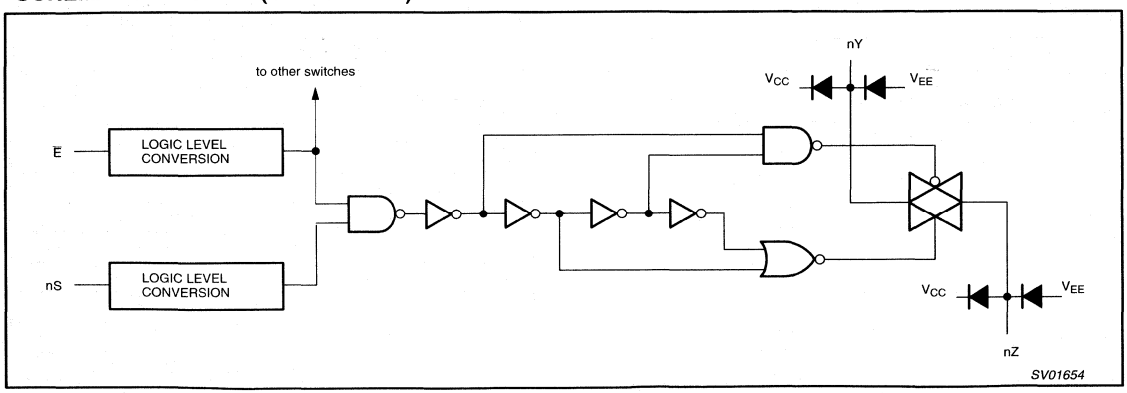
FUNCTIONAL DIAGRAM



LOGIC SYMBOL



SCHEMATIC DIAGRAM (ONE SWITCH)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	6.0	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	20	mA
$\pm I_O$	DC switch current	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.90			0.90		V
		V_{CC} = 2.0 V	1.40			1.4		
		V_{CC} = 2.7 to 3.6 V	2.00			2.0		
		V_{CC} = 4.5 V	3.15			3.15		
		V_{CC} = 6.0 V	4.20			4.20		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.30		0.30	V
		V_{CC} = 2.0 V			0.60		0.60	
		V_{CC} = 2.7 to 3.6 V			0.80		0.80	
		V_{CC} = 4.5 V			1.35		1.35	
		V_{CC} = 6.0 V			1.80		1.80	
$\pm I_I$	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND V_{CC} = 6.0 V; V_I = V_{CC} or GND			1.0 2.0		1.0 2.0	µA
$\pm I_S$	Analog switch OFF-state current per channel	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL} V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}			1.0 2.0		1.0 2.0	µA
$\pm I_S$	Analog switch ON-state current per channel	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL} V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}			1.0 2.0		1.0 2.0	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0 V_{CC} = 6.0V; V_I = V_{CC} or GND; I_O = 0			20 40		40 80	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA
R_{ON}	ON-resistance (peak)	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL} V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL} V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL} V_{CC} = 3.0 to 3.6 V; V_I = V_{IH} or V_{IL} V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL} V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}		295 120 110 80 70	– 860 300 270 200 180		– 990 360 325 240 215	Ω
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL} V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL} V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL} V_{CC} = 3.0 to 3.6 V; V_I = V_{IH} or V_{IL} V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL} V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}		225 110 85 55 40 35	– 240 150 135 100 90		– 290 180 180 120 110	Ω
R_{ON}	ON-resistance (rail)	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL} V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL} V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL} V_{CC} = 3.0 to 3.6 V; V_I = V_{IH} or V_{IL} V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL} V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}		250 120 75 60 45 40	– 270 170 155 115 105		– 325 205 180 135 120	Ω
ΔR_{ON}	Maximum variation of ON-resistance between any two channels	V_{CC} = 1.2 V; V_I = V_{IH} or V_{IL} V_{CC} = 2.0 V; V_I = V_{IH} or V_{IL} V_{CC} = 2.7 V; V_I = V_{IH} or V_{IL} V_{CC} = 3.0 to 3.6 V; V_I = V_{IH} or V_{IL} V_{CC} = 4.5 V; V_I = V_{IH} or V_{IL} V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}		– 5 4 4 3 2				Ω

NOTE:

1. All typical values are measured at T_{amb} = 25°C.
2. At supply voltage approaching 1.2V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

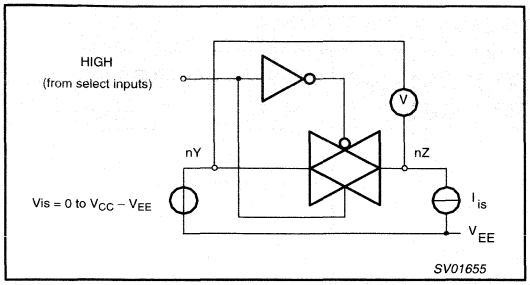


Figure 1. Test circuit for measuring ON-resistance (R_{on}).

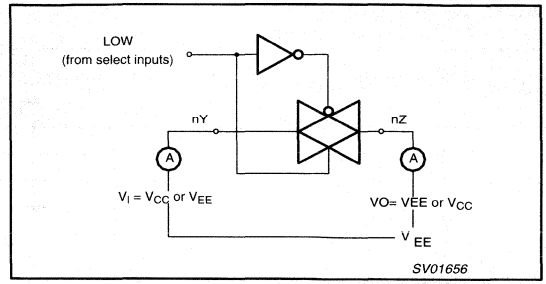


Figure 2. Test circuit for measuring OFF-state current.

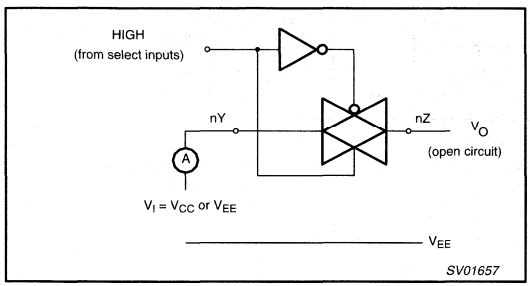


Figure 3. Test circuit for measuring ON-state current.

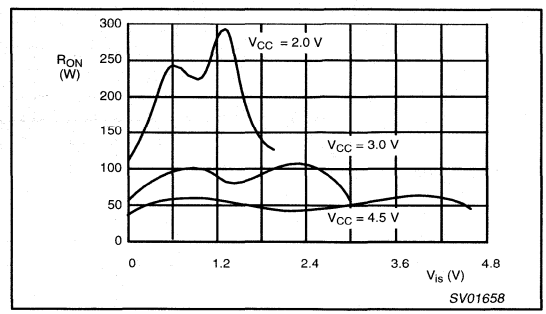


Figure 4. Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for V_{is} = 0 to $V_{CC} - V_{EE}$.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF

SYMBOL	PARAMETER	LIMITS					UNIT	CONDITION	
		−40 to +85 °C			−40 to +125 °C				
		MIN	TYP[1]	MAX	MIN	MAX		V_{CC}(V)	OTHER
t_{PHL}/t_{PLH}	Propagation delay V_{is} to V_{os}		30				ns	1.2	$R_L = \infty$; $C_L = 50$ pF Figure 12
			10	19		24		2.0	
			8	14		18		2.7	
			6*	11		14		3.0 to 3.6	
			5	9		12		4.5	
			4	7		9		6.0	
t_{PZH}/t_{PZL}	Turn-on time $\overline{E}$ to V_{os}		110				ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figures 13 and 14
			37	70		85		2.0	
			28	51		63		2.7	
			21[2]	41		50		3.0 to 3.6	
			19	35		43		4.5	
			15	27		33		6.0	
t_{PZH}/t_{PZL}	Turn-on time nS to V_{os}		95				ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figures 13 and 14
			32	61		75		2.0	
			24	45		55		2.7	
			18[2]	36		44		3.0 to 3.6	
			16	31		37		4.5	
			12	23		29		6.0	
t_{PHZ}/t_{PLZ}	Turn-off time $\overline{E}$ to V_{os}		105				ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figures 13 and 14
			37	68		80		2.0	
			28	51		59		2.7	
			22[2]	41		48		3.0 to 3.6	
			20	35		41		4.5	
			16	28		32		6.0	
t_{PHZ}/t_{PLZ}	Turn-off time nS to V_{os}		90				ns	1.2	$R_L = 1$ kΩ; $C_L = 50$ pF Figures 13 and 14
			32	59		70		2.0	
			24	44		52		2.7	
			19[2]	36		42		3.0 to 3.6	
			17	31		36		4.5	
			14	24		28		6.0	

NOTES:

1. All typical values are measured at $T_{amb} = 25°C$.
2. All typical values are measured at $V_{CC} = 3.3$V

ADDITIONAL AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	TYP	UNIT	V_{CC} (V)	$V_{IS(P-P)}$ (V)	CONDITIONS
	Sine-wave distortion f = 1 kHz	0.80	%	3.0	2.75	R_L = 10 kΩ; C_L = 50 pF Figure 10
		0.40		6.0	5.50	
	Sine-wave distortion f = 10 kHz	2.40	%	3.0	2.75	R_L = 10 kΩ; C_L = 50 pF Figure 10
		1.20		6.0	5.50	
	Switch "OFF" signal feed through	–50	dB	3.0	Note 1	R_L = 600 kΩ; C_L = 50 pF; f=1 MHz Figures 5 and 11
		–50		6.0		
	Crosstalk between any two switches	–60	dB	3.0	Note 1	R_L = 600 kΩ; C_L = 50 pF; f=1 MHz Figure 7
		–60		6.0		
$V_{(p-p)}$	Crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110	mV	3.0		R_L = 600 kΩ; C_L = 50 pF; f=1 MHz (nS or $\overline{E}$, square wave between V_{CC} and GND, $T_r = t_f$ = 6 ns) Figure 8
		220		6.0		
f_{max}	Minimum frequency response (–3 dB)	180	mHz	3.0	Note 2	R_L = 50 kΩ; C_L = 50 pF Figures 6 and 9
		200		6.0		
C_S	Maximum switch capacitance	5	pF			

GENERAL NOTES:

V_{is} is the input voltage at nY or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at nY or nZ terminal, whichever is assigned as an output.

NOTES:

1. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

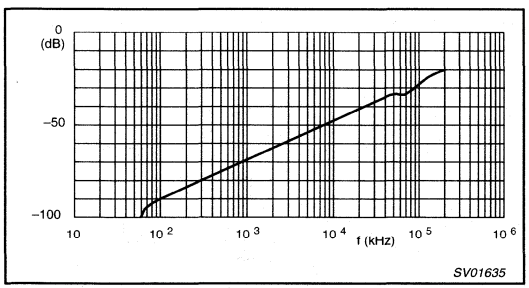


Figure 5. Typical switch "OFF" signal feed-through as a function of frequency.

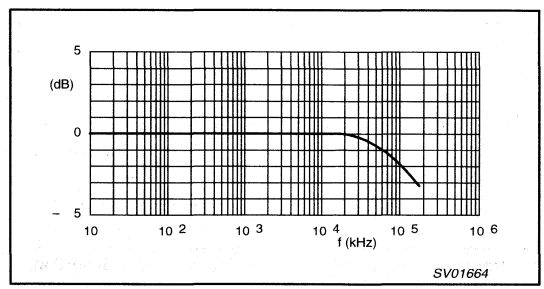


Figure 6. Typical frequency response.

NOTES TO FIGURES 5 AND 6:

Test conditions: V_{CC} = 3.0 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1kΩ.

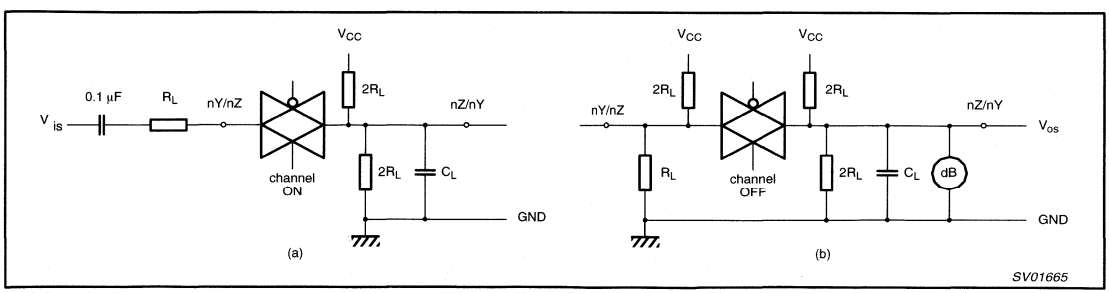


Figure 7. Test circuit for measuring crosstalk between any two switches. (a) channel ON condition; (b) channel OFF condition.

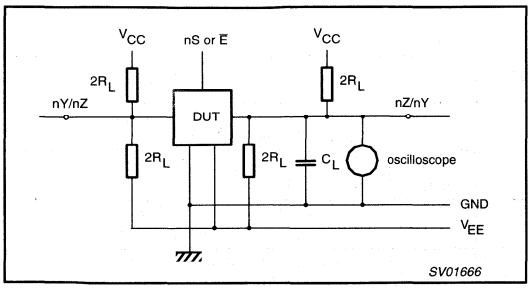
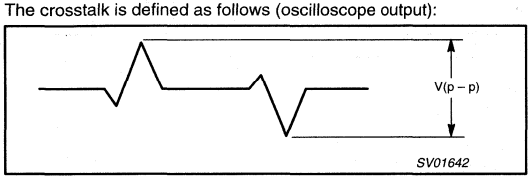


Figure 8. Test circuit for measuring crosstalk between control and any switch.

NOTE TO FIGURE 8:
The crosstalk is defined as follows (oscilloscope output):



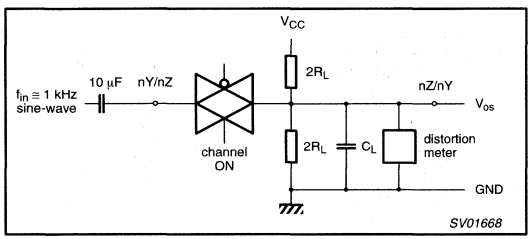


Figure 10. Test circuit for measuring sine-wave distortion.

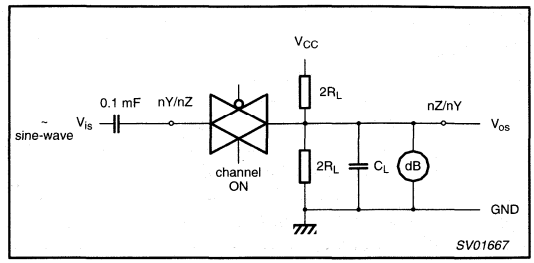


Figure 9. Test circuit for measuring minimum frequency response.

NOTE TO FIGURE 9:
Adjust input voltage to obtain 0 dBm at V_{OS} when F_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of –3 dB at V_{OS}.

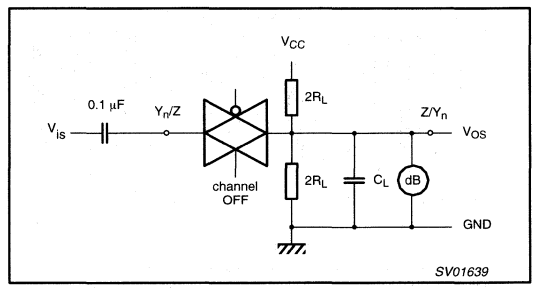


Figure 11. Test circuit for measuring switch "OFF" signal feed-through.

WAVEFORMS

V_M = 1.5 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_M = 0.5 × V_{CC} at 2.7 V > V_{CC} > 3.6 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load
V_x = V_{OL} + 0.3 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_X = V_{OL} + 0.1 × V_{CC} at 2.7 V > V_{CC} > 3.6 V
V_Y = V_{OH} − 0.3 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
V_Y = V_{OH} − 0.1 × V_{CC} at 2.7 V > V_{CC} > 3.6 V

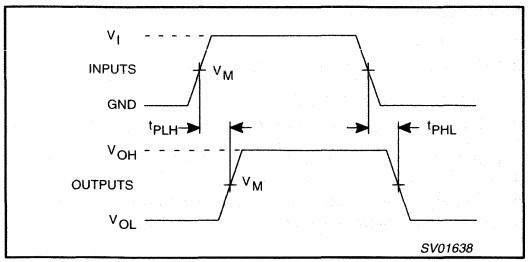


Figure 12. Input (V_{IS}) to output (V_{OS}) propagation delays.

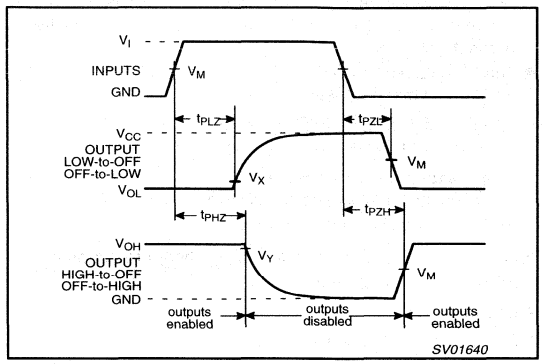
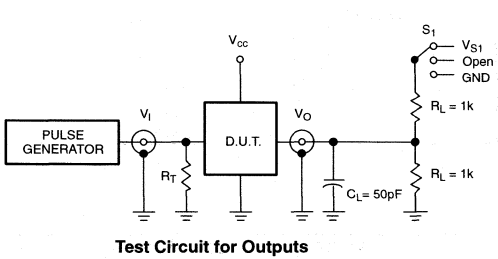
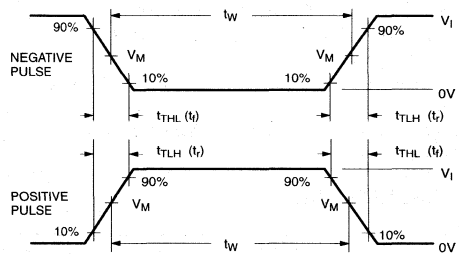


Figure 13. Turn-on and turn-off times for the inputs (nS, $\overline{E}$) to the output (V_{OS}).

TEST CIRCUIT



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{S1}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_{S1}
< 2.7V	V_{CC}	2 * V_{CC}
2.7–3.6V	2.7V	2 * V_{CC}
≥ 4.5 V	V_{CC}	2 * V_{CC}

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SY00044

Figure 14. Load circuitry for switching times.

Timer for NiCd and NiMH chargers | 74LV4799

FEATURES

- Wide supply voltage range of 0.9 V to 6 V allows 1 to 4-cell applications
- 10 V allowed on special inputs
- Supports virtually all battery chargers, including switched-mode power supplies
- On-chip timer calculates the actual capacity of the battery by measuring the charger time, discharge time and self-discharge time
- Automatic switch-over to trickle charge after completion of the charge time
- Can be adjusted for use with different types of batteries:
  - Charge time: 4 to 16 hours
  - Discharge time: 15 minutes to 4.7 hours
  - Self-discharge time: 50 to 100 days
- Battery status indication included:
  - $\overline{LED}$ output for charging/full indication
  - $\overline{MOLLI}$ output for battery-low indication
- LED mode select allows two different methods of indication
- Automatic power-ON reset
- Low-power consumption
- Requires only a few peripheral components
- Very accurate on-chip oscillator
- Scan test facilities included
- I_{CC} category: non-standard.

APPLICATIONS

- Time-controlled NiCd and NiMH low-current chargers
- Domestic appliances such as rechargeable battery shavers, electric toothbrushes etc.
- Portable equipment such as notebook PCs, laptop PCs, camera flash units etc.
- Personal communications like cordless telephones, personal mobile radios, pagers, etc.

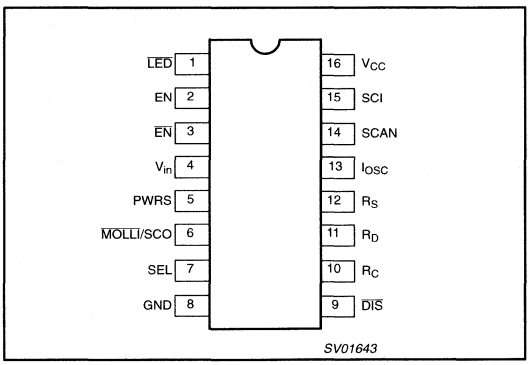
DESCRIPTION

The 74LV4799 is a low-voltage Si-gate CMOS control IC for battery management. It consists of:

- 17-stage divider
- 10-stage up/down counter
- Control logic
- Integrated precision oscillator (using external timing components)
- Automatic power-ON reset
- Scan test facilities
- Battery charging/full indication output ($\overline{LED}$)
- Battery-low indication output ($\overline{MOLLI}$)
- Open-drain-N outputs for driving the load transistor

Battery management with the 74LV4799 is based on the principle of time measurement. It measures the charge time, discharge time and self-discharge time by means of a very accurate on-chip oscillator, a divider and an up/down counter.

PIN CONFIGURATION



QUICK REFERENCE DATA

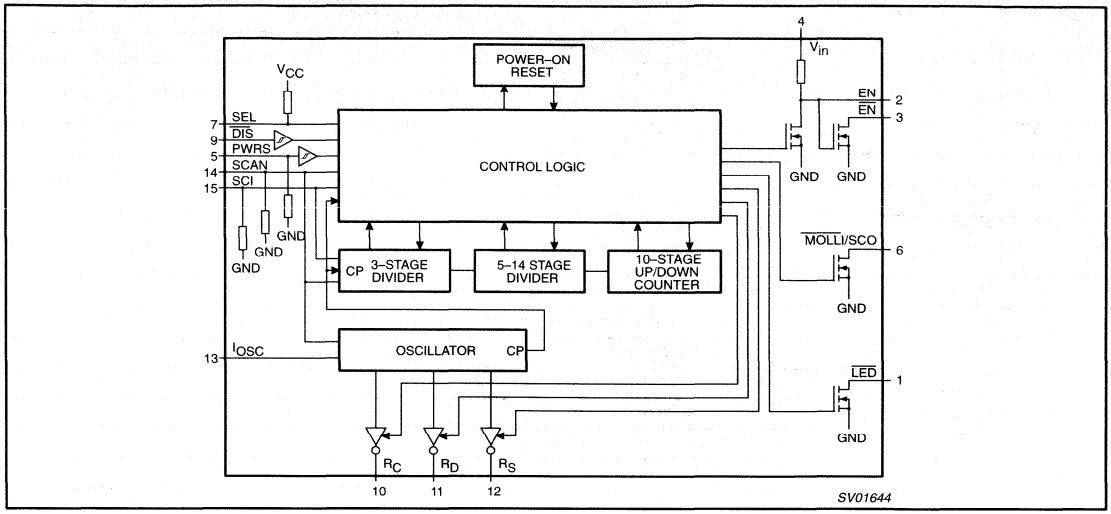
GND = 0V; T_{amb} = 25°C

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	TYPICAL	TYPICAL	UNIT
V_{CC}	DC supply voltage		0.9		6.0	V
I_{CC}	Operating supply current	V_{CC} = 3.3V; self-discharge mode; R_S = 100 kΩ; C_1 = 220nF		36		µA
Δf	Oscillator frequency tolerance	V_{CC} = 1 to 6 V			7	%

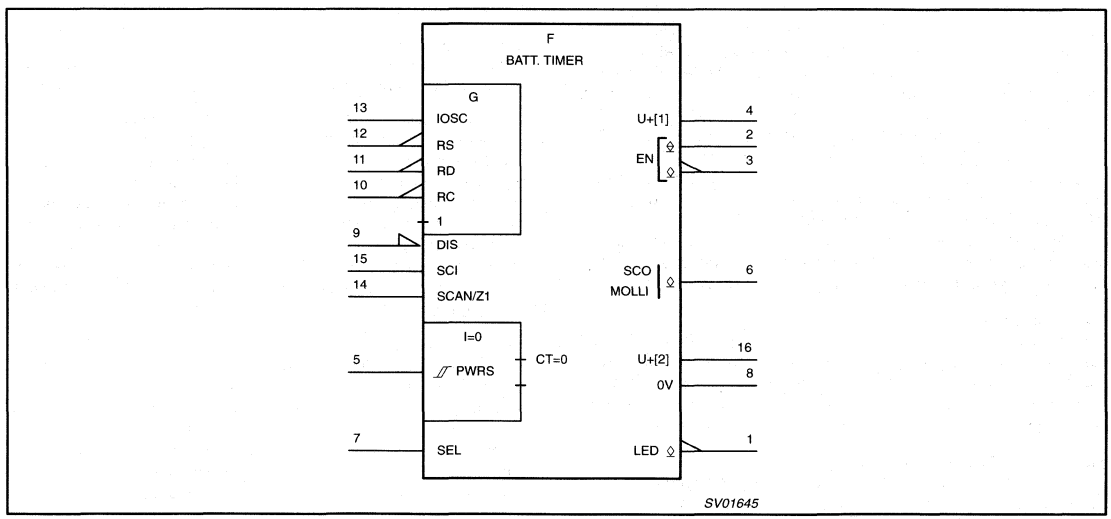
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	CODE
16-Pin Plastic DIL	0°C to +70°C	74LV4799 N	74LV4799 N	SOT38-4
16-Pin Plastic SO	0°C to +70°C	74LV4799 D	74LV4799 D	SOT109-1
16-Pin Plastic SSOP Type II	0°C to +70°C	74LV4799 DB	74LV4799 DB	SOT338-1
16-Pin Plastic TSSOP Type I	0°C to +70°C	74LV4799 PW	74LV4799PW DH	SOT403-1

FUNCTIONAL DIAGRAM



IEC LOGIC SYMBOL



PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{LED}$	LED driver output pin (active LOW)
2	EN	Enable output (active HIGH)
3	$\overline{EN}$	Enable output (active LOW)
4	V_{in}	External power input
5	PWRS	Power sense input
6	$\overline{MOLLI}$/SCO	More-or-less-low-indication output (active LOW)/scan test output
7	SEL	LED mode select input
8	GND	Ground (0 V)
9	$\overline{DIS}$	Discharge input (active LOW)
10	R_C	External resistor pin 3-State oscillator output (charge)
11	R_D	External resistor pin 3-State output (discharge)
12	R_S	External resistor pin 3-State output (self-discharge)
13	I_{OSC}	Oscillator input
14	SCAN	Scan test mode select input (active HIGH)
15	SCI	Scan test input
16	V_{CC}	Positive supply voltage

Power On Reset.
An automatic Power On Reset initiates the IC when the battery is discharged and power is connected to the circuit. The initial condition is the charge mode in which the counter is reset and counts from zero up to maximum. At start up, the battery therefore always receives a full charge cycle. When a partially charged battery is inserted, it may be over-charged during the first cycle. To guard against this, simply replace the resistor at the R_C pin with an NTC type which is in good thermal contact with the battery. If the temperature of the battery increases, the frequency of the oscillator also increases to quickly reach a counter full indication and switch-over to trickle charge. With a battery that is almost completely discharged, the POR input can also be activated during discharge or self-discharge. The counter will then be reset to zero. This is a correct action while returning to the initial condition.

Power-on sensing.
Because this IC supports virtually all battery chargers, the PWRS input has a broad input frequency spectrum (active HIGH to 100 kHz). A pull-down circuit at the PWRS input allows detection of the open state which corresponds to an inactive charger. A HIGH level on the PWRS input, or an AC signal up to 100 kHz, enables the charge mode.

Start-up with low battery voltage.
Good start-up, even with an un-charged battery, is assured by using the V_{IN} input. The voltage on the V_{IN} input biases the external bipolar transistors at the EN or $\overline{EN}$ output, even if the IC is not yet functioning. After the battery has received sufficient charge, the internal control logic takes over control of the EN and $\overline{EN}$ outputs.

Charge mode.
This mode is selected when PWRS is active (HIGH or pulsed) and the discharge input $\overline{DIS}$ is HIGH. The EN output is HIGH, and the $\overline{EN}$ output is LOW initiating continuous charge of the battery. The counter then counts from the zero state up to the maximum value. The clock frequency is determined by the external capacitor and resistor connected to the R_C output. The counter stops when it reaches its maximum value and the EN and $\overline{EN}$ outputs switch over from the continuous charge to the trickle charge mode.

Trickle charge mode.
At the maximum counter value, it is assumed that the battery is fully charged. The counter stops and remains on this maximum value.

The EN and $\overline{EN}$ outputs switch over from the continues charge to the trickle charge mode. In the trickle charge mode, the average charge current is reduced to only compensate the self-discharge of the battery by using the dedicated duty cycle control. The control is dedicated because it adjusts the duty cycle in inverse proportion to the load current, resulting in a fixed charger current irrespective of the kind of charger (e.g. 4-hour or 16-hour charger). In the trickle charge mode, the oscillator circuitry alternately generates 4 periods of R_C -C1 time-constant, and 3 periods of the R_S -C1 time-constant (See Figure 1).

Discharge mode.
The discharge input ($\overline{DIS}$) is used to detect the discharge of the battery. If $\overline{DIS}$ is LOW, the counter counts down. The clock frequency is determined by the external capacitor and resistor at the R_D output. If PWRS is inactive (LOW or open), the EN output is LOW, and the $\overline{EN}$ output is in the high impedance OFF-state (no charge of the battery). This is called the discharge mode. If PWRS is active, the circuit is in the charge/discharge mode.

Charge/Discharge mode.
If $\overline{DIS}$ is LOW and PWRS is active (HIGH or pulsed), the circuit is in the charge/discharge mode. The counter counts down. The clock frequency is determined by the external capacitor and resistor tied at the R_D output. The EN output is HIGH, and the $\overline{EN}$ output is LOW initiating continuous charge of the battery. The battery is therefore charged and discharged at the same instant, thereby maintaining a better load condition of the battery.

Self-discharge mode.
If $\overline{DIS}$ is HIGH and PWRS is inactive (LOW or open), the battery is being neither charged nor discharged. The circuit is in the self-discharge mode. This mode represents the battery leakage (self-discharge). The counter counts down. The clock frequency is determined by the external capacitor and resistor at the R_S output. When the counter reaches the zero state, it stops.

LED mode select.
The $\overline{LED}$ output drives a battery status LED which indicates the charge/full status of the battery. For optimum flexibility, two modes of operation are built-in.

- Mode 1: If SEL is LOW, the $\overline{LED}$ output is active LOW in the charge mode, and the LED blinks with a frequency of about 1 Hz during trickle charge.
- Mode 2: If SEL is HIGH or open, the LED output blinks with a frequency of about 0.25 Hz in the charge mode, and is active LOW during trickle charge. In the discharge or self-discharge mode, the $\overline{LED}$ output is open except when PWRS is active (HIGH or pulsed). Then, the battery is charging and discharging simultaneously. Although the discharge mode is dominant, the LED output is active when PWRS is also active.

NOTE: The blink frequency depends on the oscillator frequency. (See application information)

Low indication.
As part of the user interface, the $\overline{MOLLI}$ output shows when the battery needs to be charged. $\overline{MOLLI}$ stands for More Or Less Low Indication (active LOW). The function is as follows: In the discharge mode, ($\overline{DIS}$ is active LOW), the counter counts down and, when it reaches the zero state, it stops. If $\overline{DIS}$ is switched HIGH, the $\overline{MOLLI}$ output gives an output signal of four periods of about one second, with a 50% duty cycle. This can be used to activate a buzzer. The $\overline{MOLLI}$ output signal of four periods will be interrupted as soon as PWRS is activated.

Alarm indication.
If an almost completely discharged battery is connected to the charger, it may not be noticed by the user if the load switch is still on. To prevent damaging the battery, an alarm signal on the $\overline{LED}$ output will alert the user to switch off the load. The alarm signal is easily recognized, because the $\overline{LED}$ output will blink at a higher frequency than normal (about 5 Hz instead of 1 Hz). This alarm indication is only active if the SEL input is HIGH or open. If the SEL input is LOW, no alarm indication is present, because in many applications simultaneous charging and discharging is quite acceptable. (See charge/discharge mode)

Scan test mode.
If the SCAN input (pin 14) is made active HIGH, the circuit is in the test mode. The tester clock is connected to the I_{OSC} pin (pin 13). In the scan mode, the on–chip oscillator is bypassed to allow rapid testing of the divider/counter. The scan test patterns are available on request. The scan test data is entered serially through the SCI input (pin 15). The scan out data is present on the $\overline{MOLLI}$/SCO output (pin 6), which then acts as a scan output.

Remaining energy indication.
The scan test facility can be used as a remaining energy indication because the value of the counter can be read out at the scan output ($\overline{MOLLI}$/SCO). This is done by briefly interrupting the normal mode of operation, putting the circuit in the scan mode, and reading out the counter value. The circuit then reverts to the normal mode. This only works correctly with the $\overline{MOLLI}$/SCO output and SCI input linked (round coupled loop) and with exactly 49 clock pulses applied to the I_{OSC} input.

The serial scan-out data is available on the $\overline{MOLLI}$/SCO output. The value of the counter can be decoded by reading the correct bits. Details are given later in the section "Application information".

Output drivers EN and $\overline{EN}$.
In one-cell battery (low-voltage) applications, the drive from the ENABLE output ($\overline{EN}$) is insufficient to provide the base current directly for the external bipolar PNP regulator transistor. The inverse signal has therefore been made available at the ENABLE output (EN) to drive an extra bipolar NPN transistor that can provide the base current for the bipolar PNP regulator transistor as shown in Figure 2.

FUNCTION TABLE 1

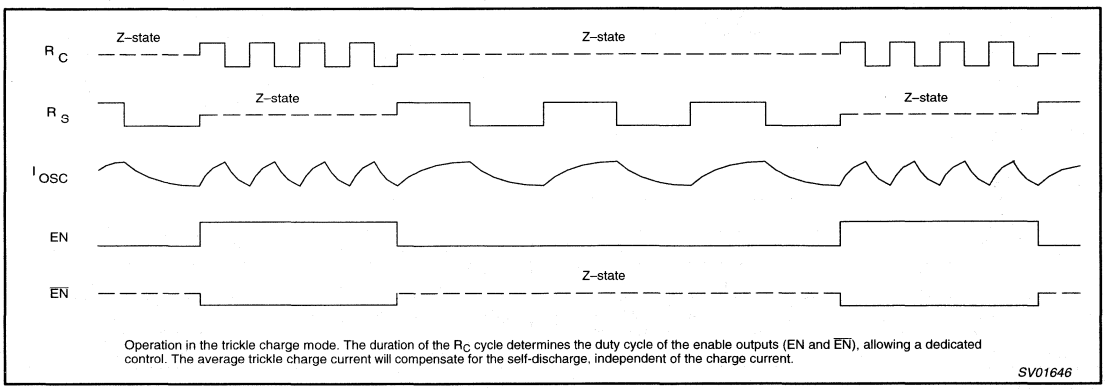
OPERATING MODES	INPUTS			OUTPUTS					DIVIDER/COUNTER	
	PWRS	V_{IN}	$\overline{DIS}$	EN	$\overline{EN}$	R_C	R_D	R_S	MODE	VALUE
Charge	H or ⎍⎍	H	H	H	L	⎍⎍	Z	Z	Count up 22 sections	< max
Trickle charge	H or ⎍⎍	H	H	⎍⎍	⏉⏉	⎍⎍	Z	⎍⎍	Stop	max
Charge/discharge	H or ⎍⎍	H	L	H	L	Z	⎍⎍	Z	Count down 18 sections	≥ min
Discharge	L or open	X	L	L	Z	Z	⎍⎍	Z	Count down 18 sections	≥ min
Self-discharge	L or open	X	H	L	Z	Z	Z	⎍⎍	Count down 27 sections	≥ min

FUNCTION TABLE 2

STATUS INDICATION	INPUTS			OUTPUTS		COUNTER	
	PWRS	$\overline{DIS}$	SEL[1]	$\overline{LED}$	$\overline{MOLLI}$	MODE	VALUE
Charge	H or ⎍⎍	H	L	L	Z	Count up	< max
	H or ⎍⎍	H	H or open	⎍⎍	Z	Count up	< max
Charge/discharge	H or ⎍⎍	L	L	L	Z	Count down	≥ min
Trickle charge	H or ⎍⎍	H	L	⎍⎍	Z	Stop	max
	H or	H	H or open	L	Z	Stop	max
Discharge	L or open	L	X	Z	Z	Count down	> min
Self-discharge	L or open	H	X	Z	Z	Count down	> min
Low	L or open	↑	X	Z	⎍	Stop	min
Low	↑	↑	X	Z	Z[2]	Count up	≥ min
Alarm	H or	L	H or open	⎍⎍	Z	Count down	≥ min

NOTES:
1. Don't change SEL during operation.
2. The $\overline{MOLLI}$ function will be interrupted as soon as PWRS is activated.

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state
X = don't care
⎍⎍ = pulsed (H/L)
⎍⎍ = pulsed (Z/L)
⎍ = 4 periods of about one second (Z/L)
↑ = LOW-to-HIGH level transition



Operation in the trickle charge mode. The duration of the R_C cycle determines the duty cycle of the enable outputs (EN and $\overline{EN}$), allowing a dedicated control. The average trickle charge current will compensate for the self-discharge, independent of the charge current.

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Figure 1. Trickle charge mode characteristics.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	0.9	1.2	6	V
V_I	Input voltage pins 4, 5, and 9 Input voltage pins 7, 13, 14, and 15		0 0	– –	10 V_{CC}	V
V_O	Output voltage pins 10, 11, and 12 Output voltage pins 1, 2, 3, and 6		0 0	– –	V_{CC} 10	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics per device	0		+70	°C
t_r, t_f	Input rise and fall times pin 5		–	–	10	ms
	Input rise and fall times pins 7, 14 and 15	V_{CC} = 1.0V; V_I = 1.0V V_{CC} = 2.0V; V_I = 2.0V V_{CC} = 3.0V; V_I = 4.5V V_{CC} = 3.6V; V_I = 6.0V	– – – –	– – – –	500 200 100 50	ns
	Input rise and fall times pin 9		–	–	2	µs

NOTE:
1. Single sided input protection applied on pins 4, 5, and 9.

ABSOLUTE MAXIMUM RATINGS[2, 3]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage		–0.5	+7.0	V
I_{IK}	DC input diode current pins 4, 5 and 9	$V_I < -0.5$ or $V_I > 12$ V		±20	mA
	DC input diode current pins 7, 13, 14 and 15	$V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V		+20	
	NON repetitive peak DC input diode current pin 9	$V_I > 10$ V and $t < 10$ µs; see note 1		10	
V_I	DC input voltage range pins 4, 5 and 9		–0.5	+12	V
	DC input voltage range pins 7, 13, 14 and 15		–0.5	V_{CC} + 0.5	V
I_{OK}	DC output diode current pins 1, 2, 3 and 6	$V_O < -0.5$ V		–20	mA
I_O	DC output sink current pins 1, 2, 3 and 6	$V_O > 0$ V		–25	mA
I_{OK}	DC output diode current pins 10, 11 and 12	$V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	DC output sink or source current pins 10, 11 and 12	-0.5 V $< V_O < V_{CC} + 0.5$ V		±25	mA
I_{GND}, I_{CC}	DC GND or V_{CC} current			±50	mA
T_{stg}	Storage temperature range		–65	+150	°C
P_{tot}	Power dissipation per package Plastic DIL Plastic mini-pack (SO) Plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125 °C above + 70 °C derate linearly with 12 mW/K above + 70 °C derate linearly with 8 mW/K above + 60 °C derate linearly with 5.5 mW/K		 750 500 400	mW

NOTES:
1. In applications where a motor is present, the input voltage may exceed the maximum V_I, level of 10 V at the $\overline{DIS}$ input for a very short period when the motor is switched off.
2. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions.
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			+25°C			0°C to +70°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.0 V	0.8	0.5	–	0.8	–	V
		V_{CC} = 4.5 V	3.6	2.4	–	3.6	–	
		V_{CC} = 6.0 V	4.8	3.2	–	4.8	–	
V_{IL}	LOW level Input voltage	V_{CC} = 1.0 V	–	0.5	0.2	–	0.2	V
		V_{CC} = 4.5 V	–	2.1	0.9	–	0.9	
		V_{CC} = 6.0 V	–	2.8	1.2	–	1.2	
V_{OH}	HIGH level output voltage; R_C, R_D outputs	V_{CC} = 1.0 V; V_I = V_{IH} or V_{IL}; I_O = –190µA	0.90	0.96	–	0.89	–	V
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}; I_O = –6.1mA	5.73	5.84	–	5.66	–	
	HIGH level output voltage; R_S output	V_{CC} = 1.0 V; V_I = V_{IH} or V_{IL}; I_O =–24µA	0.90	0.96	–	0.89	–	
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}; I_O =–760µA	5.73	5.84	–	5.66	–	
V_{OL}	LOW level output voltage; R_C, R_D outputs	V_{CC} = 1.0 V; V_I = V_{IH} or V_{IL}; I_O = 190µA	–	0.04	0.10	–	0.11	V
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}; I_O = 6.1mA	–	0.16	0.26	–	0.33	
	LOW level output voltage; R_S output	V_{CC} = 1.0 V; V_I = V_{IH} or V_{IL}; I_O =24µA	–	0.04	0.10	–	0.11	
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}; I_O =760µA	–	0.16	0.26	–	0.33	
	LOW level output voltage; $\overline{MOLLI}$, $\overline{LED}$ outputs	V_{CC} = 1.0 V; V_I = V_{IH} or V_{IL}; I_O = 220µA	–	0.04	0.10	–	0.11	
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}; I_O = 7.4mA	–	0.17	0.26	–	0.33	
	LOW level output voltage; EN output	V_{CC} = 1.0 V; V_I = V_{IH} or V_{IL}; I_O =360µA; pin 4 open	–	0.04	0.10	–	0.11	
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}; I_O =13.0mA; pin 4 open	–	0.17	0.26	–	0.33	
	LOW level output voltage; EN output	V_{CC} = 1.3 V; V_I = V_{IH} or V_{IL}; pin 4 = 10 V[1]	–	0.12	0.35	–	0.40	
	LOW level output voltage; $\overline{EN}$ output	V_{CC} = 1.0 V; V_I = V_{IH} or V_{IL}; I_O =140µA; pin 4 HIGH	–	0.04	0.10	–	0.11	
		V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}; I_O =5.0mA; pin 4 HIGH	–	0.17	0.26	–	0.33	
V_{CC}	POR level active inactive		0.25 –	– –	0.65 0.9	– –	– –	V
I_{CC}	Quiescent supply current	V_{CC} = 6.0 V; V_I = V_{CC} or GND; pins 5, 14, and 15 at GND; pins 7 and 9 at V_{CC}[2]	–	34	50	–	400	µA
I_I	Input leakage current pins 4 and 9	V_{CC} = 1.0 V; V_I = 10 V	–	–	500	–	–	nA
	Input leakage current pins 14 and15	V_{CC} = 6.0 V; V_I = V_{CC} or GND	–	–	100	–	–	
	Pull-up current pin 7	V_{CC} = 1.0 V; V_I = GND	–0.5	–2.4	–10	–	–	µA
		V_{CC} = 6.0 V; V_I = GND	–0.5	–2.4	–10	–	–	
	Pull-down current pin 5	V_{CC} = 1.0 V; V_I = V_{CC}	0.5	2.4	10	–	–	
		V_{CC} = 6.0 V; V_I = V_{CC}	0.5	2.4	10	–	–	
I_{OZH}	OFF-state current pin 1, 3, and 6	V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}; V_O = 10 V	–	–	500	–	–	nA
	OFF-state current pin 2	V_{CC} = 6.0 V; V_O = 6 V; V_{in} = open	–	–	100	–	–	
	OFF-state current pin 3	V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}; V_O = 6 V	–	–	100	–	–	
I_{OZ}	OFF-state current pins 10, 11, and 12	V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	–	–	±100	–	–	nA

NOTE:
1. This item guarantees that an external bipolar NPN-transistor can be switched off by the EN output.
2. Oscillator disabled. This can be done by I_{OC} = HIGH or LOW.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
				+25			0 to +70		
		V_{CC}(V)		MIN	TYP	MAX	MIN	MAX	
Δf	Oscillator frequency spread	1.0	Any resistor or capacitor according to the application information, see note 1	−11	−4	+3			%
		6.0		−9	−2	+5			
δ_{LED}	Duty factor at pin 1	1.0	See Note 2	–	50				%
		6.0		–	50				
δ_{MOLLI}	Duty factor at pin 6	1.0	See Note 3	–	50				%
		6.0		–	50				
t_{deb}	Debounce suppression at pin 9	1.0		–	67				ms
		6.0		–	65				
$f_{i(max)}$	Maximum frequency at power sense input	1.0		100					kHz
		6.0		100					
$f_{i(min)}$	Minimum frequency at power sense input	1.0				50			Hz
		6.0				50			

NOTES:

1. The oscillator frequency can be calculated by: $f = \frac{0.36}{R \times C1}$
2. During blinking.
3. An output signal of four periods will appear in case of discharged batteries and $\overline{DIS}$ is switched HIGH.

APPLICATION INFORMATION

Oscillator.

The frequency will be determined by the external components R_C, R_D, R_S, and C_1. The frequencies can be calculated by the following expressions: $f = \frac{0.36}{R_C \times C1}$; $f = \frac{0.36}{R_D \times C1}$; $f = \frac{0.36}{R_S \times C1}$.

R_C and C1 determine the charge time.
R_D and C1 determine the discharge time.
R_S and C1 determine the self-charge time.

The charge, discharge and self-discharge times can be calculated as follows:

Charge time $= \frac{2^{22}}{f_C}$; Discharge time $= \frac{2^{18}}{f_D}$; Self-discharge time $= \frac{2^{27}}{f_S}$

In the trickle charge mode, the average charge current will be reduced by a factor: $\frac{1}{1 + \frac{3 \times R_S}{4 \times R_C}}$

External components range

SYMBOL	PARAMETER	TEST CONDITIONS			T_{amb} (°C)			UNIT
					+25			
		V_{CC}(V)	V_1	OTHER	MIN	TYP	MAX	
R_C/R_D	Resistor range	1.0		C1 = 0.22 µF	5.360		100	kΩ
		2.0			1.150		100	
		4.5			0.562		100	kΩ
		6.0			0.511		100	
R_S	Resistor range	1.0		C1 = 0.22 µF	42.20		825	kΩ
		2.0			9.09		825	
		4.5			4.22		825	kΩ
		6.0			3.32		825	
C1	Capacitor range	1.0					no limit	pF
		2.0					no limit	
		4.5					no limit	pF
		6.0					no limit	

Charge discharge times

PARAMETER	TIME RANGE	CONDITIONS
Charge time	4 hours to 16 hours	Components ranges are within the values given in Section "External components range"
Discharge time	15 minutes to to 4.7 hours	
Self-discharge time	50 days to 100 days	

LED frequency

The frequency of the $\overline{LED}$ output (pin1) is determined by the oscillator frequency.
Three modes of operation, each with its own frequency, are possible.

Mode	SEL	$\overline{LED}$ frequency
Charge	H or open	$\frac{f_C}{256}$
Trickle charge	L	$\frac{1}{\frac{8}{f_C} + \frac{6}{f_S}}$
Alarm	H	$\frac{f_D}{32}$

$\overline{MOLLI}$ pulse duration

The MOLLI output gives an output signal of four periods with a 50% duty cycle. The duration of one period is determined by: $16/f_s$

Timing accuracy.

The timing accuracy depends on the accuracy of the on–chip oscillator and on the external R and C components. The inaccuracy of the on–chip oscillator is specified as maximum +/–7%. In most cases the actual inaccuracy will be significantly lower. This depends on the supply voltage as well as the value of the external components.

Influence of Resistor value.

Low resistor values cause some spread because the RC combination is biased by a 3–State push–pull output. The spread of the R_{on} of the push–pull stage will contribute to the frequency spread. When high–value resistors are used, any possible output leakage of the not–selected 3–State outputs will cause a frequency deviation. For these reasons, the resistor values must be within the specified ranges.

Influence of supply voltage

The trip levels of the oscillator are fixed at 20% and 80% of V_{cc}. At higher supply voltages the spread of the trip levels decreases in greater proportion because the offset voltage remains constant, and the propagation delay decreases. Furthermore, the R_{on} values of the push–pull driving stage decrease at higher voltages.

SPREAD-CAUSING FACTORS

SYMBOL	PARAMETER	V_{CC} (V)	T_{amb} (°C)			UNIT
			MIN	TYP	MAX	
V_{off}	Offset voltage	1.0		7		mV
		6.0		7		mV
t_P	Propagation delay	1.0		22		µs
		6.0		5.5		µs
R_{ON}	P-channel resistance R_C, R_D outputs	1.0		170		Ω
		6.0		25		Ω
R_{ON}	N-channel resistance R_C, R_D outputs	1.0		250		Ω
		6.0		35		Ω
R_{ON}	P-channel resistance R_S output	1.0		1300		Ω
		6.0		180		Ω
R_{ON}	N-channel resistance R_S output	1.0		1300		Ω
		6.0		180		Ω

Error free operation, even under extreme conditions.
Several measures are taken in the circuit design to ensure error–free operation, even with very low supply voltages. Moreover, the circuit has been made very insensitive to the effects of external fields. The measures taken during the design are:

- Use of synchronous logic
- Bistable POR instead of monostable POR
- Data retention assured below a supply voltage of 0.9 V.
- Debounce circuitry on $\overline{DIS}$ input (maximum expected debounce time = 10 ms)
- Schmitt trigger on PWRS (power sense) input and on $\overline{DIS}$ input
- Special oscillator security to prevent any malfunction.

Synchronous logic and bistable POR.
Use of synchronous logic results in much lower sensitivity to spikes on input pins. The POR is adapted to fit well into a synchronous environment. An increasing supply voltage sets the POR. The POR output signal is routed to the control logic and divider/counter. it is synchronized with the on–chip clock. After all flip–flops are reset, a reset acknowledge signal is generated which resets the POR. This method ensures that the POR signal is acknowledged in all cases, even at very low voltages.

Data retention.
The circuit may be used in an application where an electric motor is present. When the motor is switched on, it will disturb the supply voltage for a short period. The POR level is set at such a level that, even with very low supply voltages, the POR will not respond during motor switch on. The flip–flops will retain their data during the supply voltage disturbance because of the inherent data retention of any CMOS gate. However, when the battery is almost completely discharged and the motor switch is activated, the dip on the supply voltage line can be too large. The retention of the POR is therefore made deliberately worse than that of the internal flip–fops. The POR will therefore respond long before the flip–flops will loose their data. This results in a proper start condition for a new charge cycle.

Debounce circuitry on $\overline{DIS}$ input.
A discharge cycle is activated by a switch. To protect the circuit from any bounce of the switch contacts, de–bounce circuitry is provided at the $\overline{DIS}$ input. The circuitry allows a switch de–bounce time of max. 10 ms.

Schmitt trigger on PWRS (power sense) input.
The PWRS input can be corrupted by high transients due to disturbances on the mains supply. To suppress any false triggering, the PWRS input is provided with a Schmitt–trigger. However, for some applications, it is advisable to connect a low–value capacitor (150 pF min.) between the PWRS input and GND.

Special oscillator security to prevent any malfunction.
The excellent performance of the oscillator is achieved by using linear op–amp techniques. The oscillator consists of an internal reference, two comparators and a latch. Care was taken to design a very reliable oscillator even with a supply voltage below 0.9 V. If one of the comparators ceases to operate with a supply voltage below 0.9 V, the latch will not be corrupted. Priority was given to stop the oscillator rather than allow uncontrolled oscillation.

All these measures result in reliable 1-cell to 4-cell battery charge management.

Remaining energy indication:
The scan test facility can be used as a remaining energy indication because the value of the counter can be read–out at the scan output ($\overline{MOLLI}$/SCO). This is achieved by briefly interrupting the normal mode of operation, putting the circuit in the scan mode (pin 14 = HIGH), and reading–out of the counter value. The circuit is then returned to the normal mode (pin 14 = LOW or open).

Read–out procedure: The contents of the counter flip–flops can be read–out in the scan mode. To ensure that there is no disturbance of the circuit function, it is essential to either create a round coupled loop by linking the $\overline{MOLLI}$/SCO output (pin 6) directly to the SCI input pin 15), or to shift–in the serial data of the scan line at the SCI input after completion of the read out cycle. 49 clock pulses are needed on the losc input (pin 13) to shift–out the contents of the whole scan line. The most–significant bit of the counter will appear at the $\overline{MOLLI}$/SCO output after the last clock pulse. The least–significant bit after the penultimate clock pulse, etc. Selecting the last three or four bits will yield sufficiently high accuracy to obtain the counter value which represents the remaining energy of the battery.

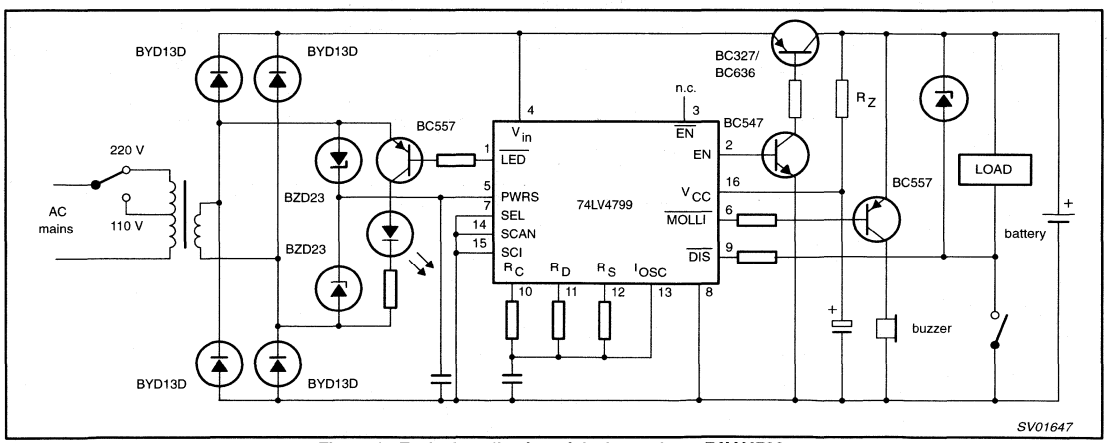


Figure 2. Typical application of the low-voltage 74LV4799.

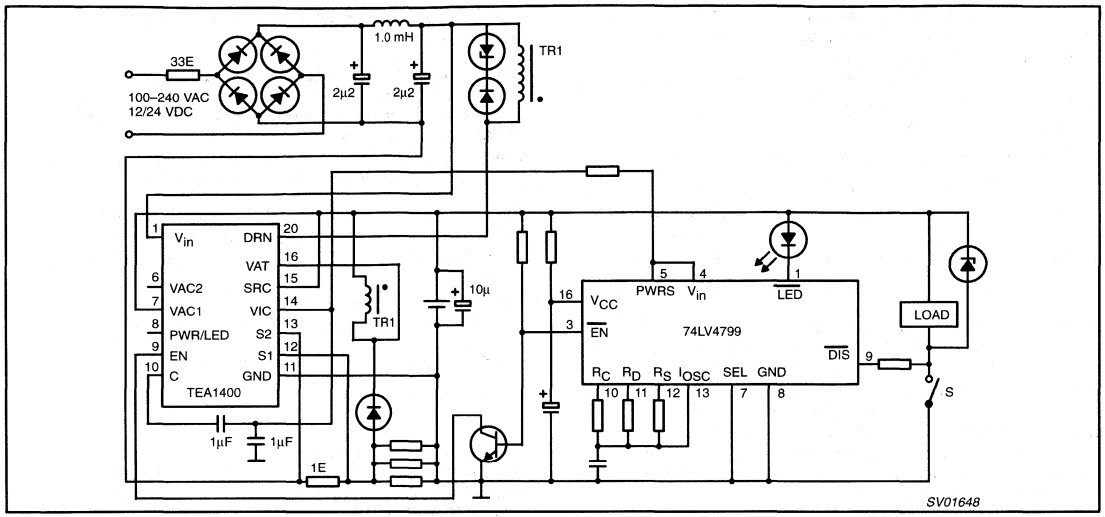


Figure 3. Application diagram of the 74LV4799 in combination with the high-voltage IC TEA1400.

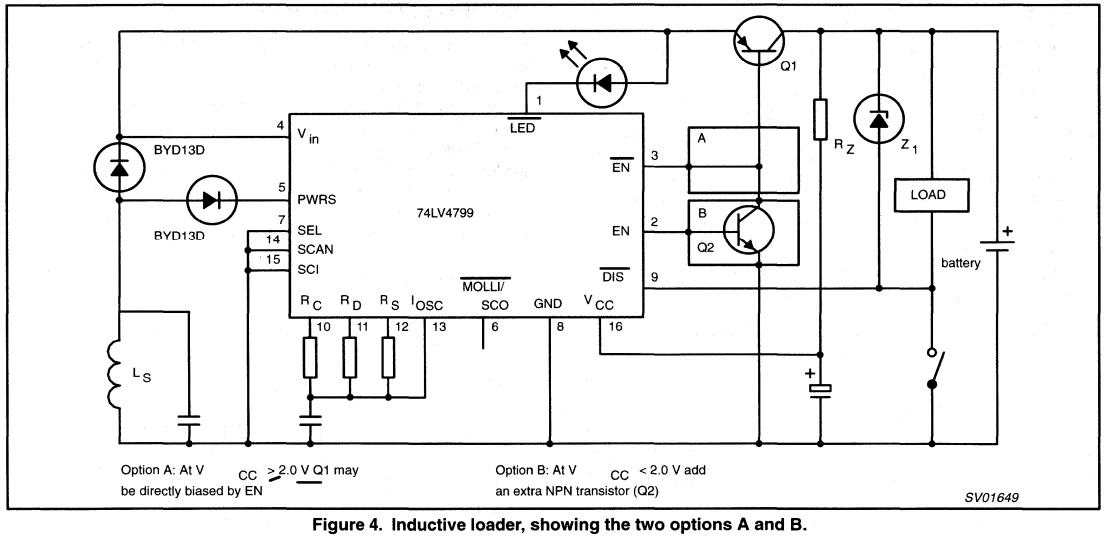


Figure 4. Inductive loader, showing the two options A and B.

Section 3
Low Voltage CMOS (LVC)

Advanced Low Voltage CMOS Logic

CONTENTS

Quad 2-input NAND gate — 74LVC00A

FEATURES

- Wide supply range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 5-volt tolerant inputs, for interfacing with 5-volt logic

DESCRIPTION

The 74LVC00A is a high-performance, low power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall times.

The 74LVC00A provides the 2-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nY	C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	28	pF

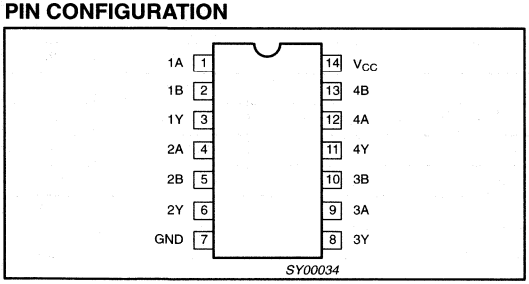
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

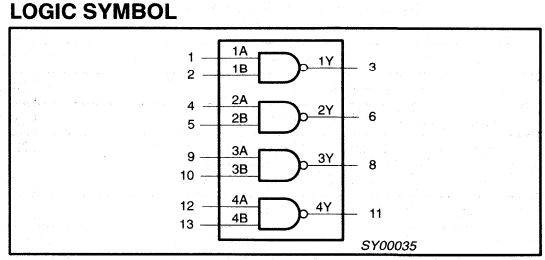
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVC00A D	74LVC00A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC00A DB	74LVC00A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC00A PW	74LVC00APW DH	SOT402-1

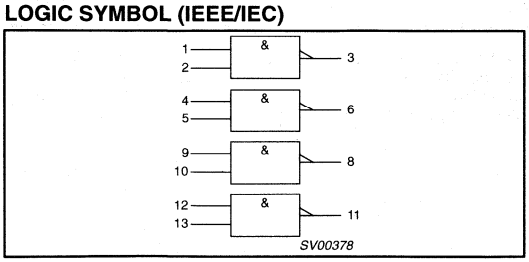
PIN CONFIGURATION



LOGIC SYMBOL



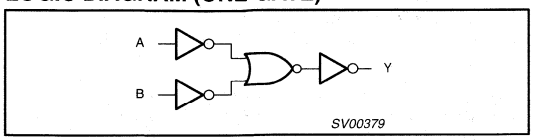
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage (for max. speed performance)		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} + 0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF

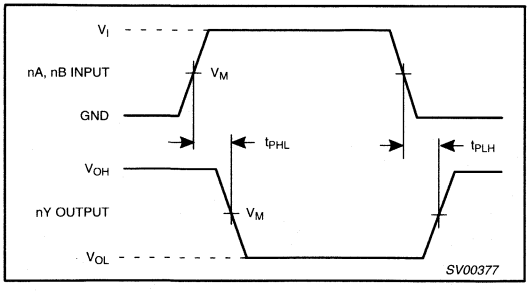
SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	TYP	MAX	TYP	
t_{PHL}/ t_{PLH}	Propagation delay nA, nB to nY	1, 2	1.5	3.0	5.0	1.5	3.4	5.8	11	ns

NOTE:

1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

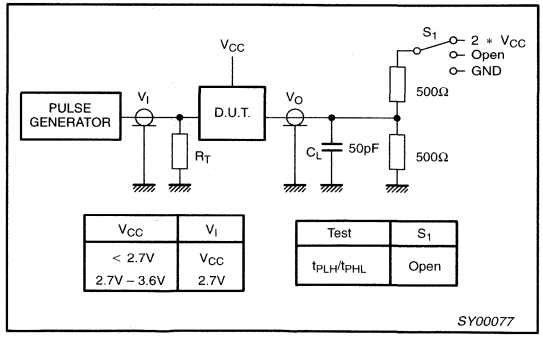
AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA) to output (nY) propagation delays.

TEST CIRCUIT



Waveform 2. Load circuitry for switching times.

Quad 2-input NOR gate — 74LVC02A

FEATURES

- Wide supply range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 5-volt tolerant inputs, for interfacing with 5-volt logic

DESCRIPTION

The 74LVC02A is a high performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC02A provides the 2-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nY	C_L = 50 pF; V_{CC} = 3.3 V	2.8	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	28	pF

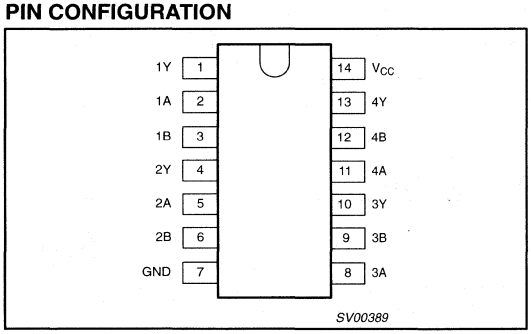
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVC02A D	74LVC02A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC02A DB	74LVC02A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC02A PW	74LVC02APW DH	SOT402-1

PIN CONFIGURATION

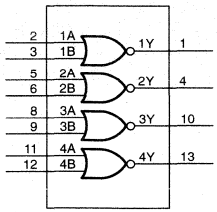


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y – 4Y	Data outputs
2, 5, 8, 11	1A – 4A	Data inputs
3, 6, 9, 12	1B – 4B	
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

Quad 2-input NOR gate 74LVC02A

LOGIC SYMBOL



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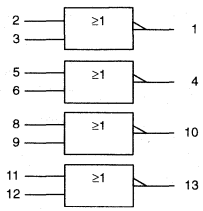
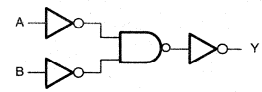
LOGIC SYMBOL (IEEE/IEC)



SV00391

LOGIC DIAGRAM (ONE GATE)



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FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage (for max. speed performance)		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	−0.5 to V_{CC} + 0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

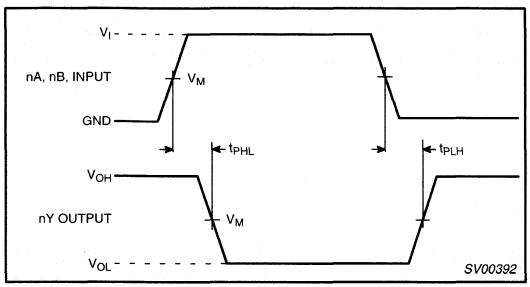
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	Figures 1, 2	1.5	2.8	4.6	1.5	3.2	5.6	11	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

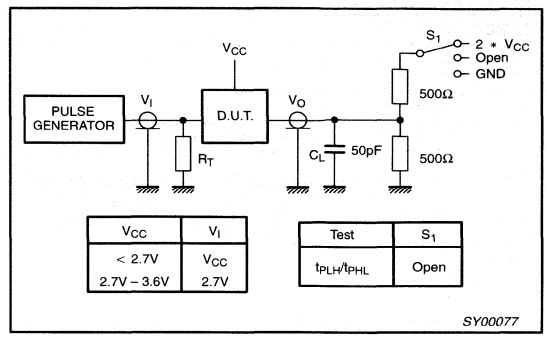
AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT



Waveform 2. Load circuitry for switching times.

Hex inverter | 74LVC04A

FEATURES

- Wide supply range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 5-volt tolerant inputs, for interfacing with 5-volt logic

DESCRIPTION

The 74LVC04A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC04A provides six inverting buffers.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 50 pF; V_{CC} = 3.3 V	2.5	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	25	pF

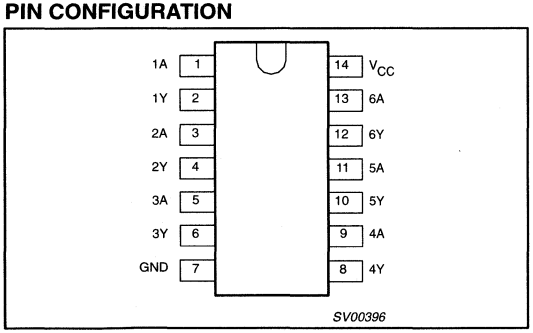
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVC04A D	74LVC04A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC04A DB	74LVC04A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC04A PW	74LVC04APW DH	SOT402-1

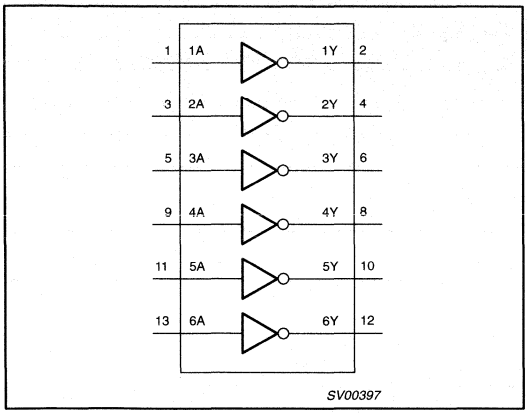
PIN CONFIGURATION



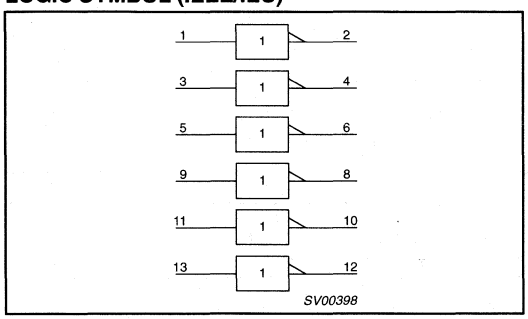
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

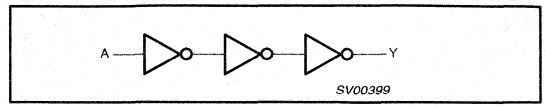
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

INPUTS	OUTPUTS
nA	nY
L	H
H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	V_{CC} + 0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		± 0.1	± 5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF

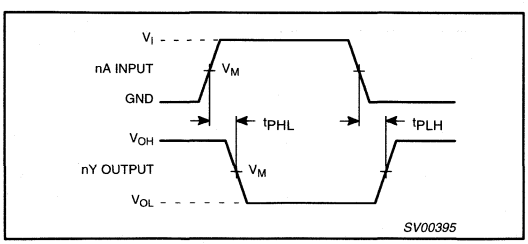
SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	TYP	MAX	TYP	
t_{PHL}/ t_{PLH}	Propagation delay nA to nY	1	1.5	2.5	4.5	1.5	3.2	5.5	16.0	ns

NOTE:

1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

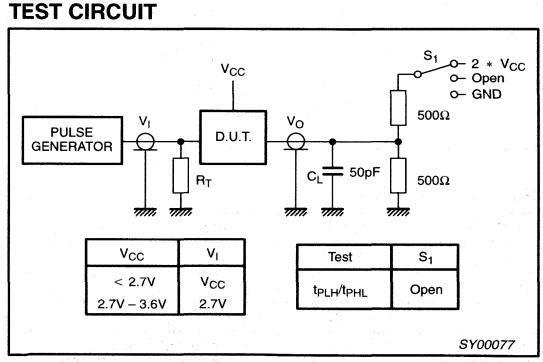
AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA) to output (nY) propagation delays.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open

Waveform 2. Load circuitry for switching times.

Hex inverter | 74LVCU04A

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVCU04A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVCU04A is a general purpose hex inverter. Each of the six inverters is a single stage with unbuffered outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 50 pF; V_{CC} = 3.3 V	4.3	ns
C_I	Input capacitance		7.8	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	16.8	pF

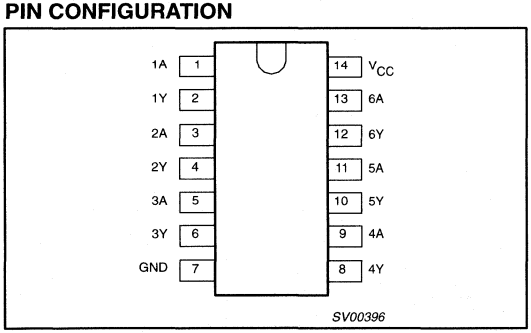
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation(P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

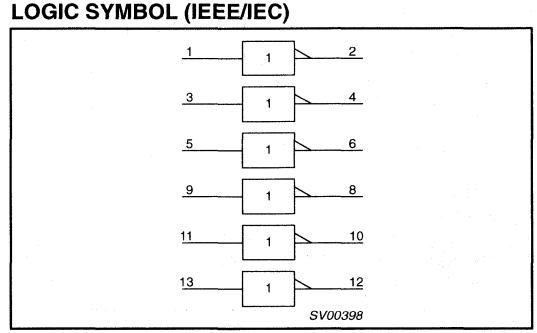
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic SO	–40°C to +85°C	74LVCU04A D	74LVCU04A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVCU04A DB	74LVCU04A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVCU04A PW	74LVCU04APW DH	SOT402-1

PIN CONFIGURATION



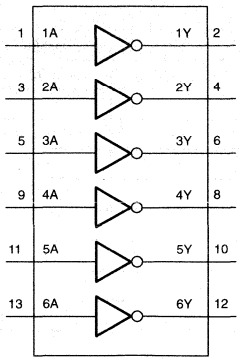
LOGIC SYMBOL (IEEE/IEC)



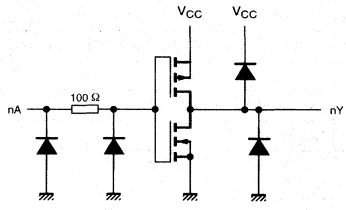
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A – 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y – 6Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC DIAGRAM (ONE INVERTER)



FUNCTION TABLE

INPUTS	OUTPUTS
nA	nY
L	H
H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC input voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V;V_{OL}(max) = 0.5 V; I_O = -100 µA	V_{CC}			V
		V_{CC} = 2.0 V; V_{OL}(max) = 0.5 V; I_O = -100 µA	1.2			
		V_{CC} = 2.7 V; V_{OL}(max) = 0.5 V; I_O = -100 µA	1.8			
		V_{CC} = 3.0 V; V_{OL}(max) = 0.5 V; I_O = -100 µA	2.0			
		V_{CC} = 3.6 V; V_{OL}(max) = 0.5 V; I_O = -100 µA	2.4			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V; V_{OH}(min) = V_{CC} – 0.5 V; I_O = 100 µA			GND	V
		V_{CC} = 2.0 V; V_{OH}(min) = V_{CC} – 0.5 V; I_O = 100 µA			0.6	
		V_{CC} = 2.7 V; V_{OH}(min) = V_{CC} – 0.5 V; I_O = 100 µA			0.6	
		V_{CC} = 3.0 V; V_{OH}(min) = V_{CC} – 0.5 V; I_O = 100 µA			1.0	
		V_{CC} = 3.6 V; V_{OH}(min) = V_{CC} – 0.5 V; I_O = 100 µA			1.2	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7 V; V_{CC} or GND; I_O = -12 mA	V_{CC} – 0.5			V
		V_{CC} = 3.0 V; V_{CC} or GND; I_O = -100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0 V; V_{CC} or GND; I_O = -12 mA	V_{CC} – 0.6			
		V_{CC} = 3.0 V; V_{CC} or GND; I_O = -24 mA	V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7 V; V_{CC} or GND; I_O = 12 mA			0.40	V
		V_{CC} = 3.0 V; V_{CC} or GND; 12mA; I_O = 100µA			0.20	
		V_{CC} = 3.0 V; V_{CC} or GND; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6 V; 5.5 V or GND; Not for I/O pins		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6 V; V_{CC} or GND; I_O = 0		0.1	10	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		$V_{CC} = 1.2V$	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay nA to nY	Figure 1	–	2.7	4.3	–	5.3	–	ns

NOTE:
1. These typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25°C$.

AC WAVEFORM

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \bullet V_{CC}$ at $V_{CC} < 2.7$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

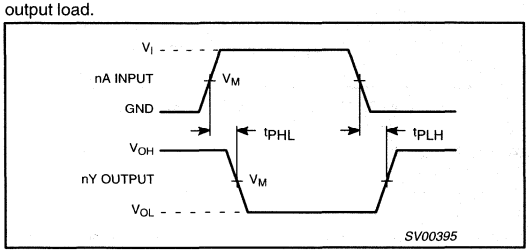


Figure 1. Input (nA) to output (nY) propagation delays.

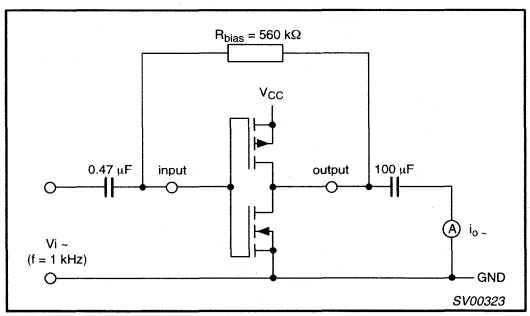


Figure 2. Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Figure 3).

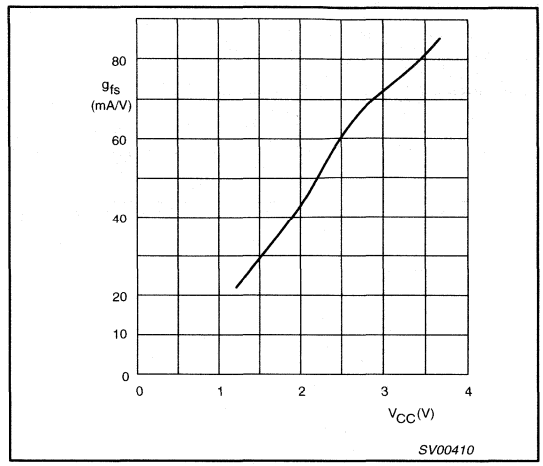
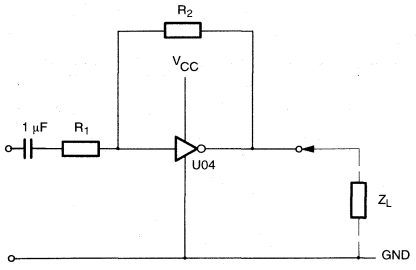


Figure 3. Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at $T_{amb} = 25°C$.

APPLICATION INFORMATION

Some applications for the 74LVU04 are:

- Linear amplifier (see Figure 4)
- In crystal oscillator designs (see Figure 5)
- Astable multivibrator (see Figure 6)



Note:

Z_L > 10kΩ; A_{OL} = 20 (typical)

$$A_u = -\frac{A_{OL}}{1 + \frac{R_1}{R_2}(1 + A_{OL})}; V_{OMax(P-P)} \approx V_{CC} - 1.5\ V \text{ centered at } {}^1/_2 V_{CC}$$

3 kΩ ≤ R1, R2 ≤ 1 MΩ

Typical unity gain bandwidth product is 5 MHz.

C_l, see Figure10

A_{OL} = open loop amplification

A_u = voltage amplification

SV00404

Figure 4. LVU04 used as a linear amplifier.

Note to Figure 4

Z_L > 10 kΩ; A_{OL} = 20 (typical)

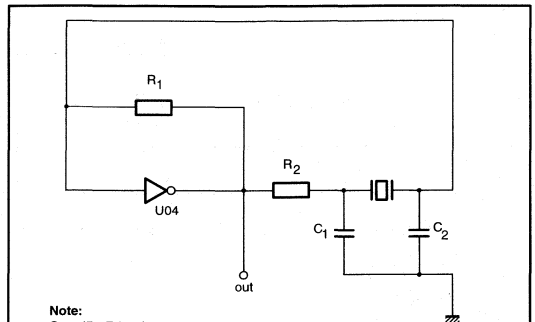
$$A_u = -\frac{A_{OL}}{1 + \frac{R_1}{R_2}(1 + A_{OL})}; V_{O\ Max\ (P-P)} \approx V_{CC} - 1.5\ V \text{ centered at } {}^1/_2 V_{CC}$$

3 kΩ ≤ R1, R2 ≤ 1 MΩ

Typical unity gain bandwidth product is 50 MHz.

A_{OL} = open loop amplification

A_u = voltage amplification



Note:

C_1 = 47 pF (typ.)

C_2 = 22 pF (typ.)

R_1 = 1 to 10 MΩ (typ.)

R_2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 2 mA at V_{CC} = 3 V and f = 1 MHz).

SV00408

Figure 5. Crystal oscillator configuration.

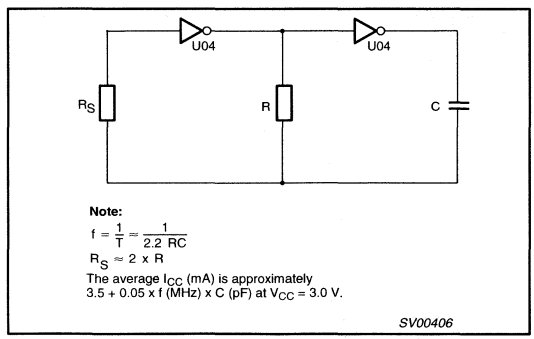
Note to Figure 5

C_1 = 47 pF (typ.)

C_2 = 22 pF (typ.)

R_1 = 1 to 10 MΩ (typ.)

R_2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC}.



Note:

$f = \frac{1}{T} \approx \frac{1}{2.2\ RC}$

$R_S \approx 2 \times R$

The average I_{CC} (mA) is approximately 3.5 + 0.05 x f (MHz) x C (pF) at V_{CC} = 3.0 V.

SV00406

Figure 6. LVCU04 used as an astable multivibrator.

Note to Figure 6

$$f = \frac{1}{T} \approx \frac{1}{2.2\ RC}$$

$R_S \approx 2 \times R$

Quad 2-input AND gate 74LVC08A

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC08A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC08A provides the 2-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 50 pF; V_{CC} = 3.3 V	2.6	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	28	pF

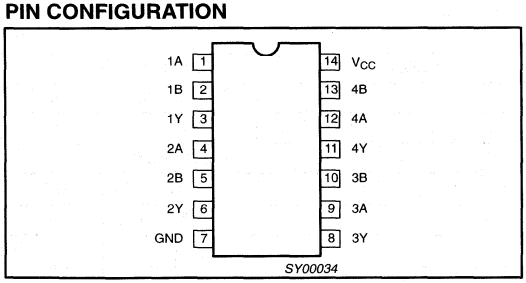
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

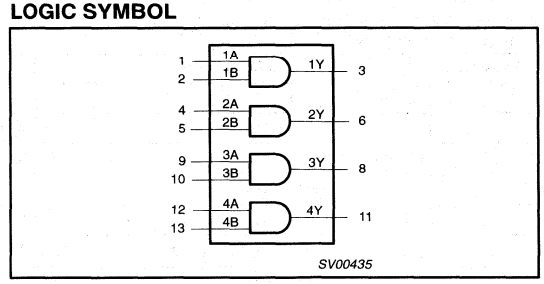
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVC08A D	74LVC08A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC08A DB	74LVC08A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC08A PW	74LVC08APW DH	SOT402-1

PIN CONFIGURATION



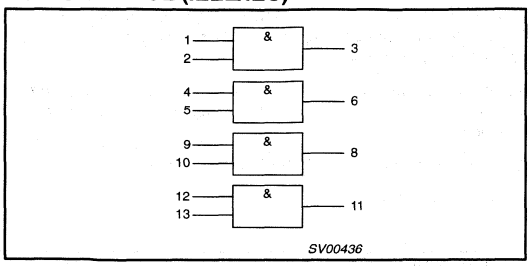
LOGIC SYMBOL



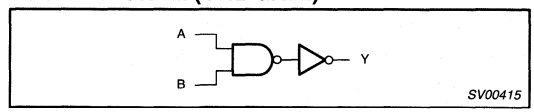
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

NOTES:
H = HIGH voltage level
L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	$V_{CC}-0.5$			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	$V_{CC}-0.2$	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −18mA	$V_{CC}-0.6$			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	$V_{CC}-0.8$			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

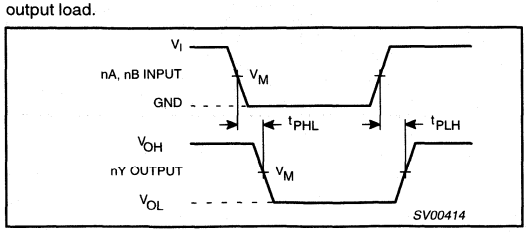
GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	TYP	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	1, 2	1.5	2.6	5.1	1.5	3.0	6.1	16	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

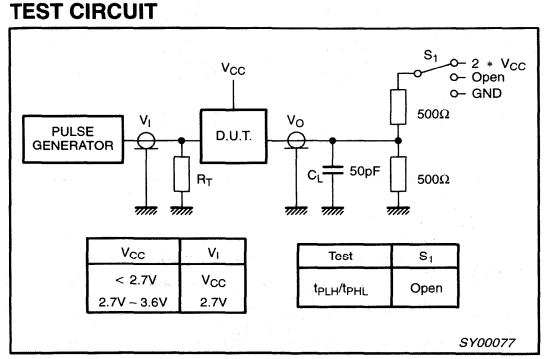
AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open

Waveform 2. Load circuitry for switching times.

Triple 3-input NAND gate | 74LVC10A

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LVC10A is a high performance, low power, low voltage, Si gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC10A provides the 3-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	C_L = 50 pF; V_{CC} = 3.3 V	3.9	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	26	pF

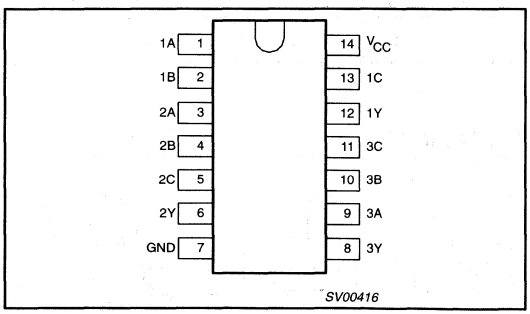
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

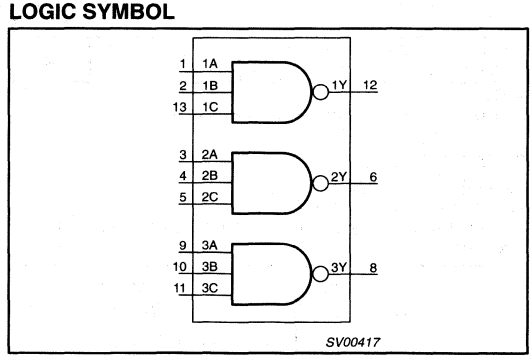
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVC10A D	74LVC10A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC10A DB	74LVC10A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC10A PW	74LVC10APW DH	SOT402-1

PIN CONFIGURATION



LOGIC SYMBOL

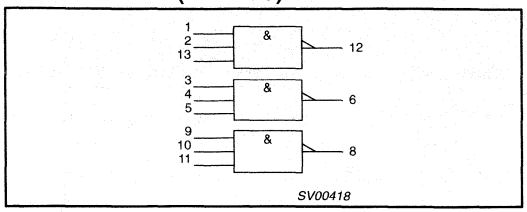


PIN DESCRIPTION

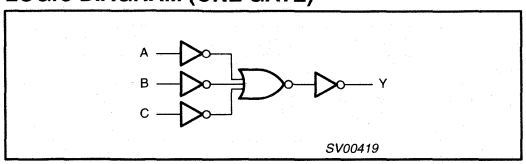
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
13, 5, 11	1C – 3C	Data inputs
14	V_{CC}	Positive supply voltage

Triple 3-input NAND gate 74LVC10A

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/ t_{PLH}	Propagation delay nA, nB, nC to nY	Figures 1, 2	1.5	3.9	5.7	1.5	6.7	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

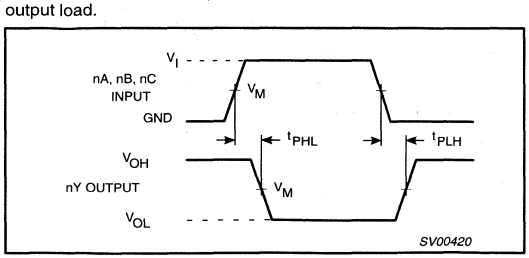


Figure 1. Input (nA, nB, nC) to output (nY) propagation delays.

TEST CIRCUIT

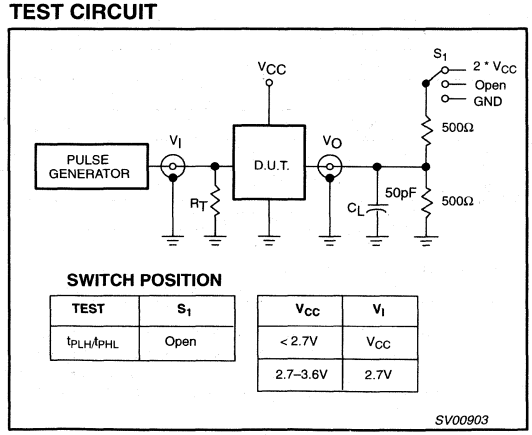


Figure 2. Load circuitry for switching times.

Triple 3-input AND gate 74LVC11

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LVC11 is a high-performance, low power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC11 provides the 3-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	C_L = 50 pF; V_{CC} = 3.3 V	3.7	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	26	pF

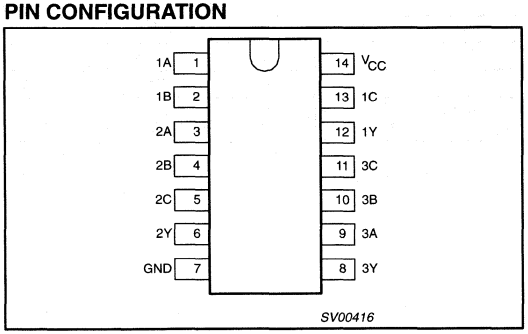
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

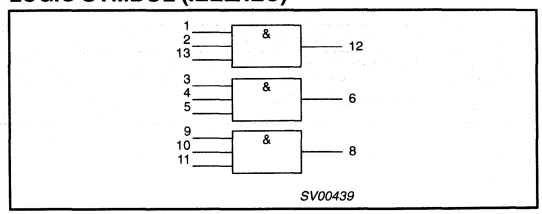
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVC11 D	74LVC11 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC11 DB	74LVC11 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC11 PW	74LVC11PW DH	SOT402-1

PIN CONFIGURATION



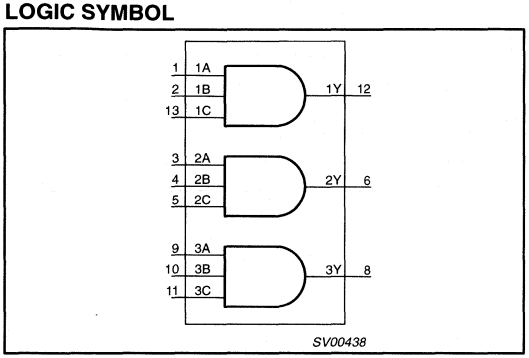
LOGIC SYMBOL (IEEE/IEC)



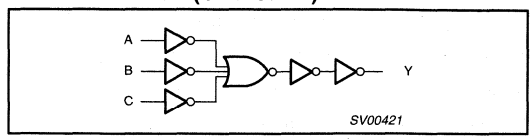
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
13, 5, 11	1C – 3C	Data inputs
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

NOTES:
H = HIGH voltage level
L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	−0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

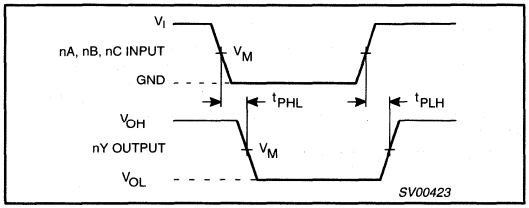
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	1, 2	–	3.7	6.2	–	7.0	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

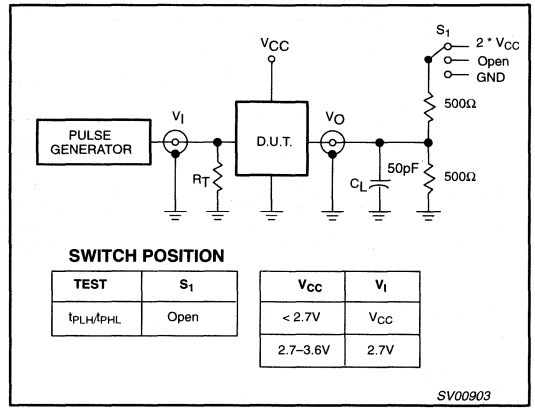
AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA, nB, nC) to output (nY) propagation delays.

TEST CIRCUIT



SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Waveform 2. Load circuitry for switching times.

Hex inverting Schmitt-trigger with 5V tolerant input

74LVC14A

FEATURES

- Wide supply voltage range of: 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

APPLICATIONS

- Wave and pulse shapers for highly noisy environments
- Astable multivibrators
- Monostable multivibrators

DESCRIPTION

The 74LVC14A is a high-performance, low power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC14A provides six inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r \leq t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 50 pF; V_{CC} = 3.3 V	4	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	25	pF

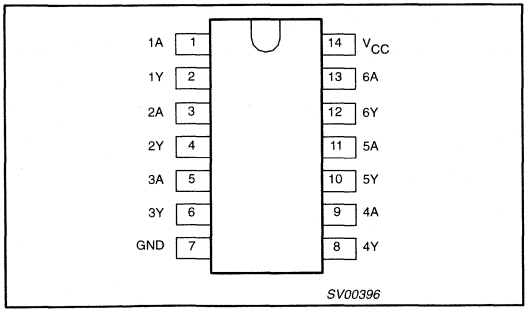
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVC14A D	74LVC14A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC14A DB	74LVC14A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC14A PW	74LVC14APW DH	SOT402-1

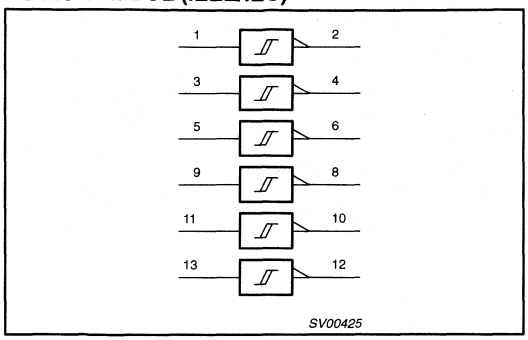
PIN CONFIGURATION



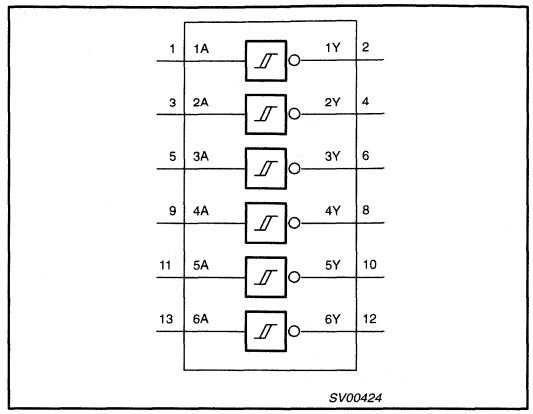
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A – 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y – 6Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

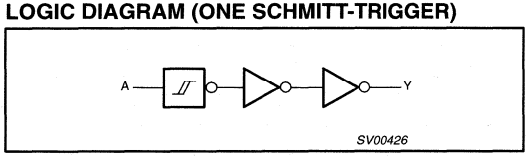
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM (ONE SCHMITT-TRIGGER)



FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC input voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW	Note 2	−0.5 to V_{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	−0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package			mW
	– plastic mini-pack (SO)	above +70°C derate linearly with 8 mW/K	500	
	– plastic shrink mini-pack (SSOP and TSSOP)	above +60°C derate linearly with 5.5 mW/K	500	

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

TRANSFER CHARACTERISTICS

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	T_{amb} (°C)			UNIT	TEST CONDITIONS	
		−40 TO +85				V_{CC} (V)	WAVEFORMS
		MIN	TYP[1]	MAX			
V_{T+}	Positive-going threshold	–	–	1.2	V	1.2	Figures 1 and 2
		1.1	–	2.0		2.7	
		1.1	–	2.0		2.7 to 3.6	
V_{T-}	Negative-going threshold	0	–	–	V	1.2	Figures 1 and 2
		0.8	–	1.5		2.7	
		0.8	–	1.5		2.7 to 3.6	
V_H	Hysteresis ($V_{T+} - V_{T-}$)	–	–	–	V	1.2	Figures 1, 2 and 3
		0.3	0.4	–		2.7	
		0.3	0.45*	–		2.7 to 3.6	

NOTES:

1. All typical values are measured at T_{amb} = 25°C
2. The V_{IH} and V_{IL} from the DC family characteristics are superseded by the V_{T+} and V_{T-}.

TRANSFER CHARACTERISTIC WAVEFORMS

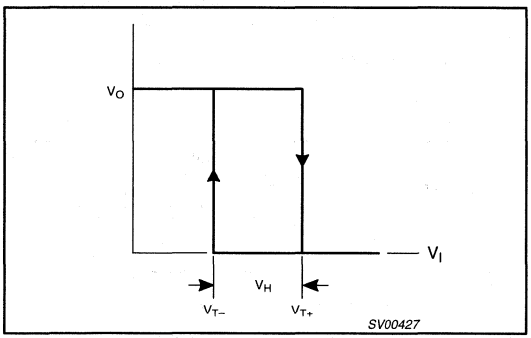


Figure 1. Transfer characteristic.

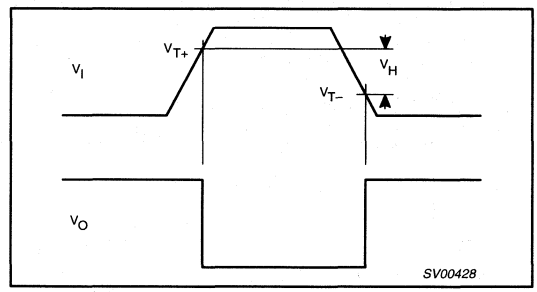


Figure 2. Definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 20% and 70%

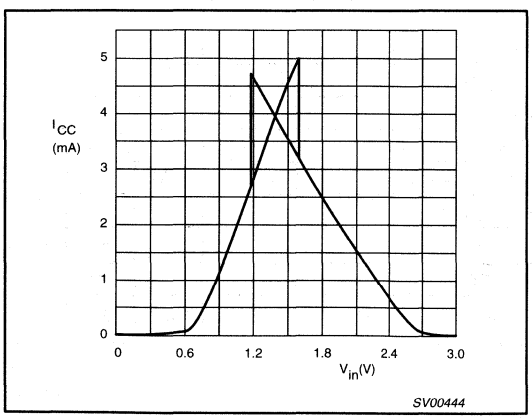


Figure 3. Typical 74LVC14 transfer characteristics; V_{CC} = 3.3 V.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	TYP	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay nA to nY	Figure 1, 2	1.5	4.5	6.4	1.5	5.0	7.5	18	ns

NOTE:
1. These typical values are at $V_{CC} = 3.3$V and $T_{amb} = 25°C$.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \bullet V_{CC}$ at $V_{CC} < 2.7$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

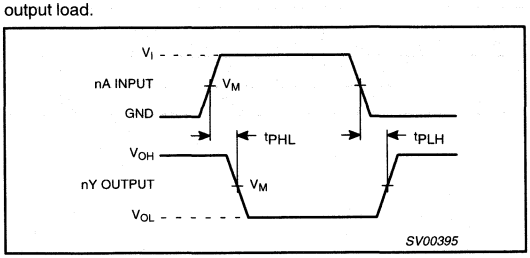
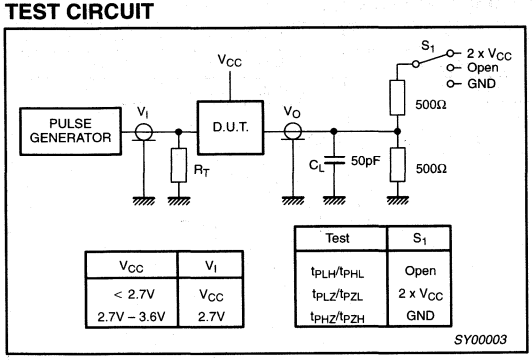


Figure 1. Input (nA) to output (nY) propagation delays.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 2. Load circuitry for switching times.

APPLICATION INFORMATION

All values given are typical unless otherwise specified.

Note to Figure 7: $f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$

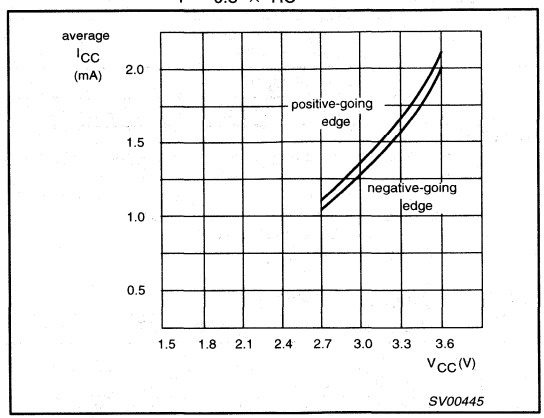


Figure 3. Average I_{CC} for LVC Schmitt-trigger devices; linear change of V_I between 0.8 V to 2.0 V.

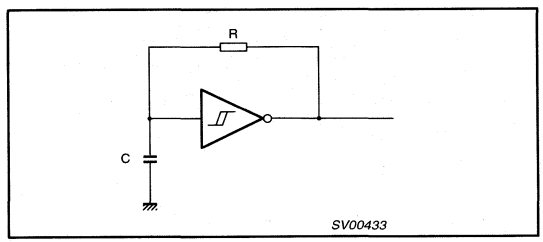


Figure 4. Relaxation oscillator using the LVC14.

Triple 3-input NOR gate 74LVC27

FEATURES

- Wide supply voltage: 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LVC27 is a high-performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC27 provides the 3-input NOR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	C_L = 50 pF; V_{CC} = 3.3 V	3.4	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	26	pF

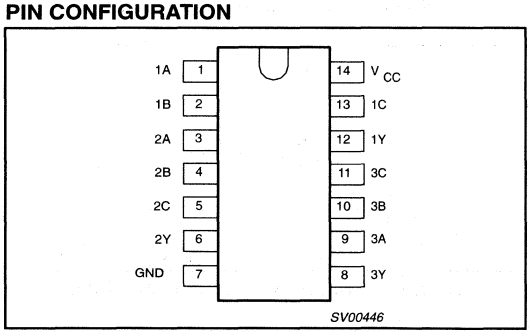
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

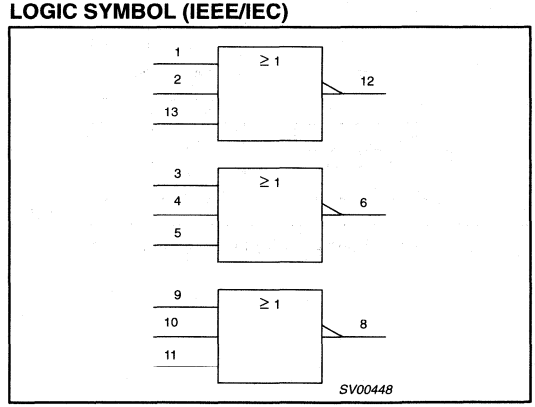
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVC27 D	74LVC27 D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC27 DB	74LVC27 DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC27 PW	74LVC27PW DH	SOT402-1

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)

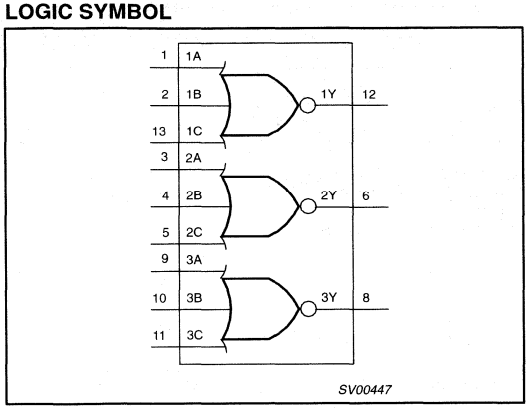


Triple 3-input NOR gate 74LVC27

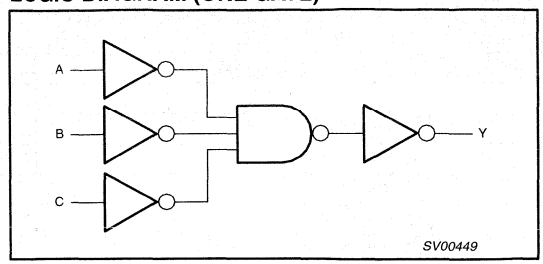
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
13, 5, 11	1C – 3C	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	−0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−60 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/ t_{PLH}	Propagation delay nA, nB, nC to nY	Figure 1, 2	–	3.4	5.9	–	7.0	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \bullet V_{CC}$ at $V_{CC} < 2.7$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

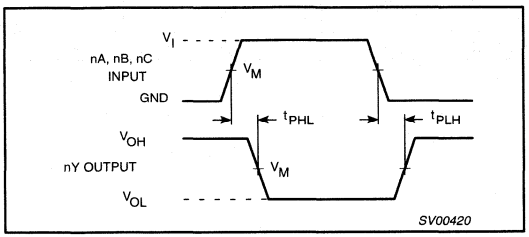
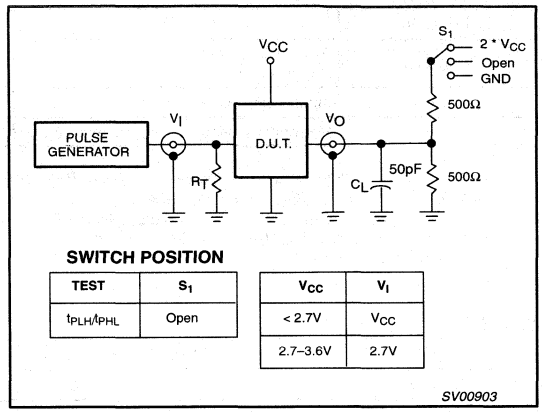


Figure 1. Input (nA, nB, nC) to output (nY) propagation delays.

TEST CIRCUIT



SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Figure 2. Load circuitry for switching times.

Quad 2-input OR gate 74LVC32A

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC32A is a high-performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC32A provides the 2-input OR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	C_L = 50 pF; V_{CC} = 3.3 V	2.6	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	28	pF

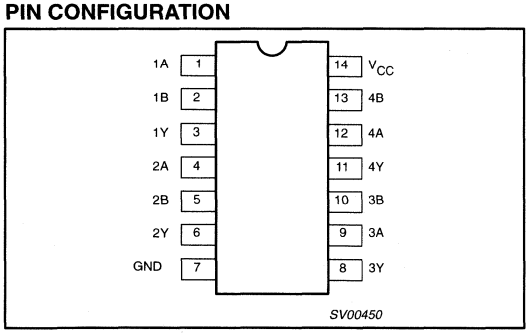
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	–40°C to +85°C	74LVC32A D	74LVC32A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC32A DB	74LVC32A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC32A PW	74LVC32APW DH	SOT402-1

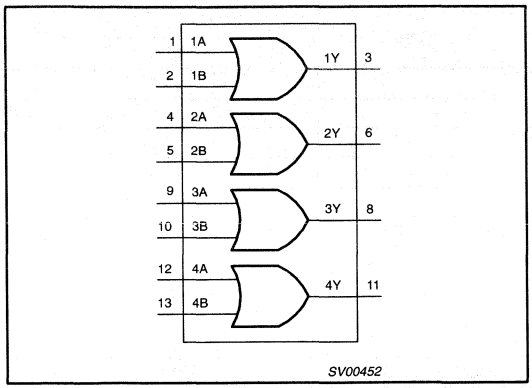
PIN CONFIGURATION



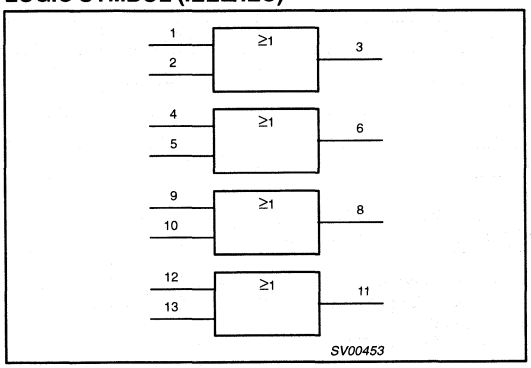
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

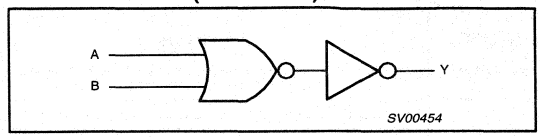
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

NOTES:
H = HIGH voltage level
L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		± 0.1	± 5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

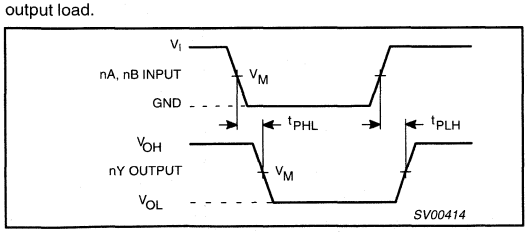
GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	WAVEFORMS	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	TYP	MAX	TYP	
t_{PHL}/ t_{PLH}	Propagation delay nA, nB to nY	1, 2	1.5	2.6	4.9	1.5	3.0	5.9	16	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

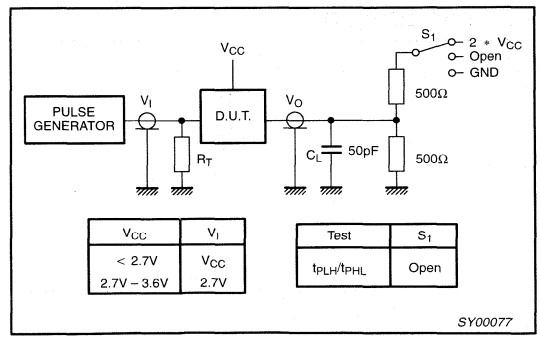
AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT



Waveform 2. Load circuitry for switching times.

Dual D-type flip-flop with set and reset; positive-edge trigger

74LVC74A

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC74A is a high-performance, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC74A is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action in all data inputs makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V	3.6 3.5 3.5	ns
f_{max}	Maximum clock frequency		250	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	30	pF

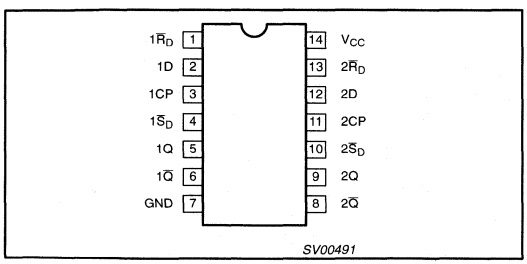
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + \sum (V_O^2/R_L) \times$ duty factor LOW, where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

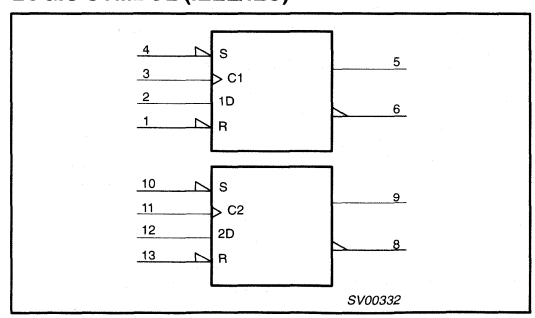
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	−40°C to +85°C	74LVC74A D	74LVC74A D	SOT108-1
14-Pin Plastic SSOP Type II	−40°C to +85°C	74LVC74A DB	74LVC74A DB	SOT337-1
14-Pin Plastic TSSOP Type I	−40°C to +85°C	74LVC74A PW	74LVC74APW DH	SOT402-1

PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



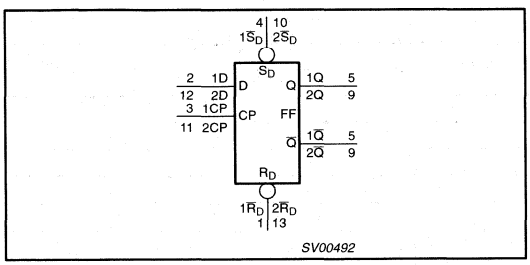
Dual D-type flip-flop with set and reset; positive-edge trigger

74LVC74A

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{R}_D$, $2\overline{R}_D$	Asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	Data inputs
3, 11	1CP, 2CP	Clock input (LOW-to-HIGH, edge triggered)
4, 10	$1\overline{S}_D$, $2\overline{S}_D$	Asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	True flip-flop outputs
6, 8	$1\overline{Q}$, $2\overline{Q}$	Complement flip-flop outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



FUNCTION TABLE

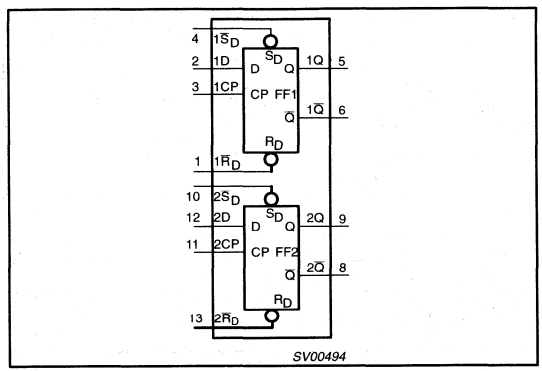
INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

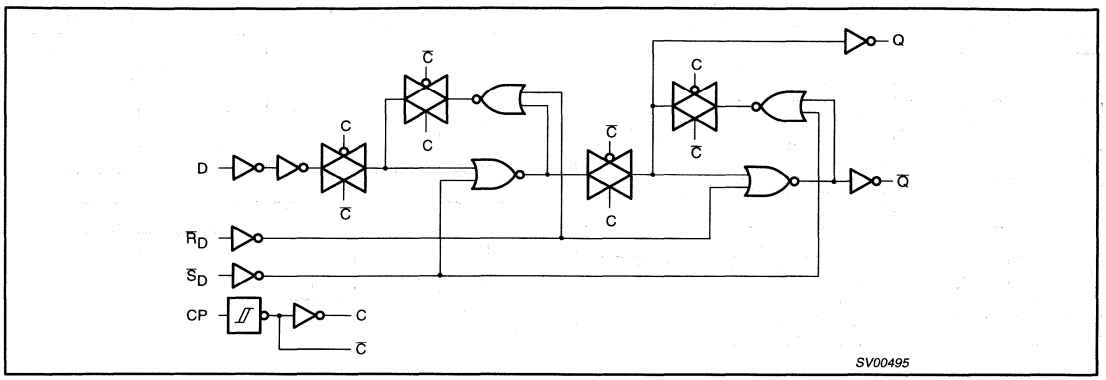
NOTES:

H = HIGH voltage level
L = LOW voltage level
X = don"t care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

FUNCTIONAL DIAGRAM



LOGIC DIAGRAM (ONE FLIP-FLOP)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP1	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = –40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/ t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$	Figures 1, 3	1.5	3.6	5.2	–	6.0	ns
	Propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$	Figures 2, 3	1.5	3.5	5.4	–	6.4	ns
	Propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$	Figures 2, 3	1.5	3.5	5.4	–	6.4	ns
t_W	Clock pulse width HIGH or LOW	Figure 1	3.3	1.3	–	–	–	ns
	Set or reset pulse width LOW	Figure 2	3.3	1.7	–	–	–	
t_{rem}	Removal time set or reset	Figure 2	1	–3	–	–	–	ns
t_{su}	Set-up time nD to nCP	Figure 1	2.0	0.8	–	–	–	ns
t_h	Hold time nD to nCP	Figure 1	1	–0.7	–	–	–	ns
f_{max}	Maximum clock pulse frequency	Figure 1	150	250	–	–	–	MHz

NOTE:

1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

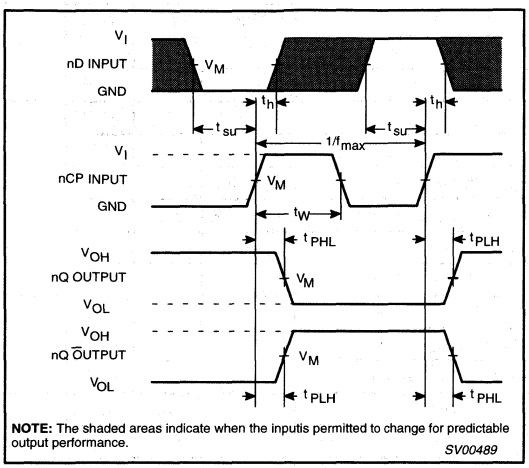


Figure 1. Clock (nCP) to output (nQ, nQ̄) propagation delays, clock pulse width, nD to nCP set-up times, the nCP to nD hold times, output transition times and maximum clock pulse frequency.

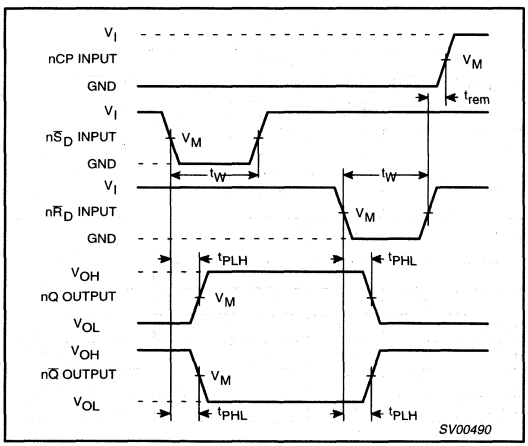
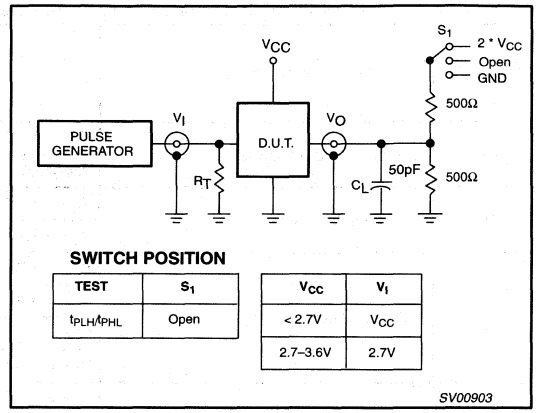


Figure 2. Set (nS̄D) and reset (nR̄D) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nR̄D to nCP removal time.

TEST CIRCUIT



SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Figure 3. Load circuitry for switching times.

Quad 2-input exclusive OR gate 74LVC86A

FEATURES

- Wide supply range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 5-volt tolerant inputs, for interfacing with 5-volt logic

DESCRIPTION

The 74LVC86A is a high-performance, low-power, low-voltage Si-gate CMOS device that is pin and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC86A provides the 2-input EXCLUSIVE-OR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL} t_{PLH}	Propagation delay nA, nB to nYn	C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	V_{CC} = 3.3 V, V_I = GND to V_{CC}[1]	28	pF

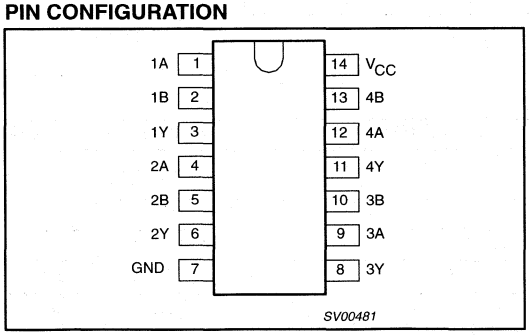
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

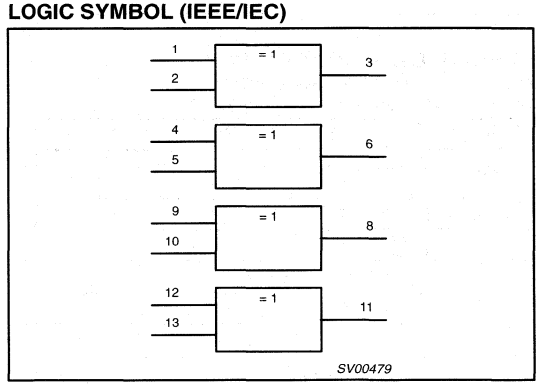
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	–40°C to +85°C	74LVC86A N	74LVC86A N	SOT27-1
14-Pin Plastic SO	–40°C to +85°C	74LVC86A D	74LVC86A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC86A DB	74LVC86A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC86A PW	74LVC86APW DH	SOT402-1

PIN CONFIGURATION



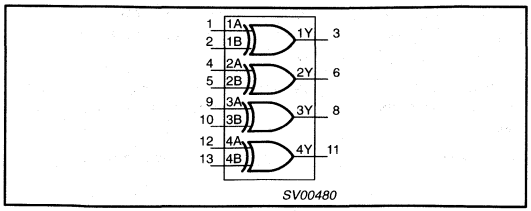
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL

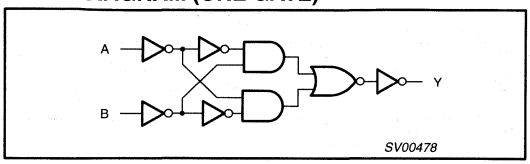


FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level

LOGIC DIAGRAM (ONE GATE)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage (for max. speed performance)		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} + 0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = –40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	TYP	
t_{PHL}/ t_{PLH}	Propagation delay nA, nB to nY	Figures 1, 2	1.5	3.0	5	1.5	3.4	5.8	11	ns

NOTE:

1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

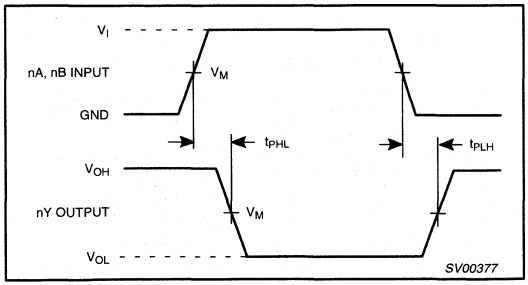
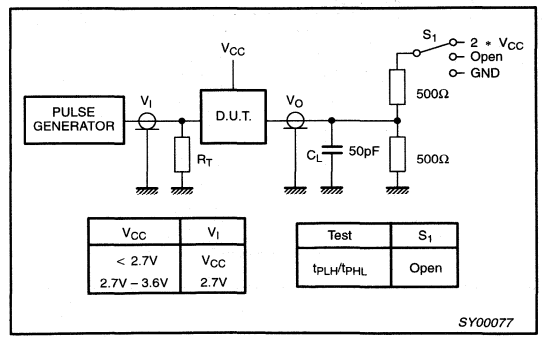


Figure 1. Input (nA, nB) to output (nY) propagation delays

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open

Figure 2. Load circuitry for switching times.

Dual $J\overline{K}$ flip-flop with set and reset; positive-edge trigger — 74LVC109

FEATURES

- Wide supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output capability: standard
- I_{CC} category: flip-flops

DESCRIPTION

The 74LVC109 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT109.

The 74LVC109 is a dual positive-edge triggered $J\overline{K}$-type flip-flop featuring individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table. The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. The $J\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V	4.0 4.5 4.5	ns
f_{max}	Maximum clock frequency		250	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_I = GND to V_{CC}[1]	27	pF

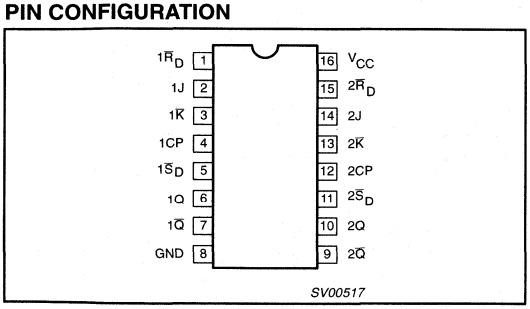
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic SO	–40°C to +85°C	74LVC109 D	74LVC109 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC109 DB	74LVC109 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC109 PW	74LVC109PW DH	SOT403-1

PIN CONFIGURATION

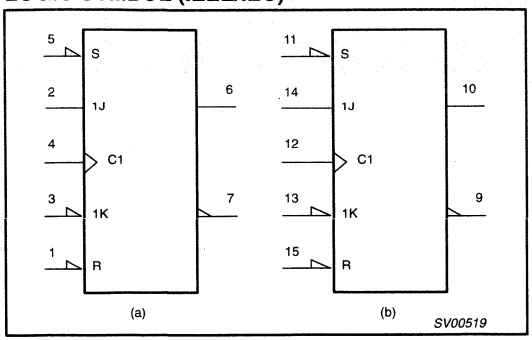


PIN DESCRIPTION

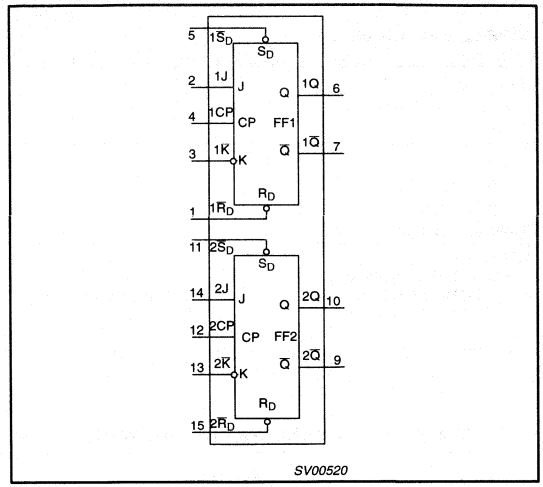
PIN NUMBER	SYMBOL	FUNCTION
1, 15	1$\overline{R}_D$, 2$\overline{R}_D$	Asynchronous reset input (active LOW)
2, 14, 3, 13	1J, 2J, 1$\overline{K}$, 2$\overline{K}$	Synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	Clock input (LOW-to-HIGH, edge-triggered)
5, 11	1$\overline{S}_D$, 2$\overline{S}_D$	Asynchronous set inputs (active LOW)
6, 10	1Q, 2Q	True flip-flop outputs
7, 9	1$\overline{Q}$, 2$\overline{Q}$	Complement flip-flop outputs
8	GND	Ground (O V)
16	V_{CC}	Positive supply voltage

Dual $\overline{JK}$ flip-flop with set and reset; positive-edge trigger 74LVC109

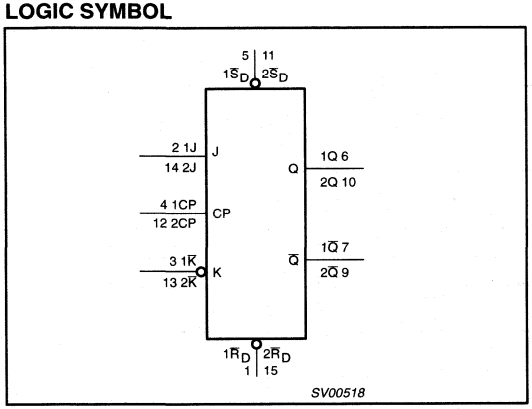
LOGIC SYMBOL (IEEE/IEC)



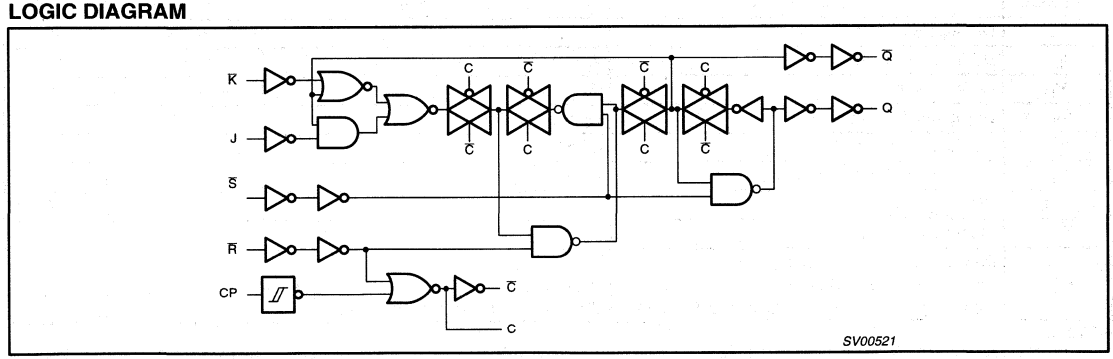
FUNCTIONAL DIAGRAM



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS					OUTPUTS	
	$n\overline{S}_D$	$n\overline{R}_D$	nCP	nJ	$n\overline{K}$	nQ	$n\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

NOTES:
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.
X = don't care
↑ = LOW-to-HIGH CP transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −24mA	V_{CC} − 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} −0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = −40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$	Figures 1, 3		4.3	7.5			8.5	ns
t_{PLH}	Propagation delay n$\overline{S}_D$ to nQ n$\overline{R}_D$ to n$\overline{Q}$	Figures 2, 3		4.5	8.0			9.0	ns
t_{PHL}	Propagation delay n$\overline{S}_D$ to n$\overline{Q}$ n$\overline{R}_D$ to nQ	Figures 2, 3		5.2	9.0			10	ns
t_W	Clock pulse width HIGH or LOW	Figure 1	3.3	2.0					ns
t_W	Set or reset pulse width HIGH or LOW	Figure 2	3.0						ns
t_{rem}	Removal time n$\overline{S}_D$, n$\overline{R}_D$ to nCP	Figure 2	3.0						ns
t_{su}	Set-up time nJ, n$\overline{K}$ to CP	Figure 1	2.5						ns
t_h	Hold time nJ, n$\overline{K}$ to nCP	Figure 1	2.0						ns
f_{max}	Maximum clock pulse frequency	Figure 1	150	225					MHz

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V; V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

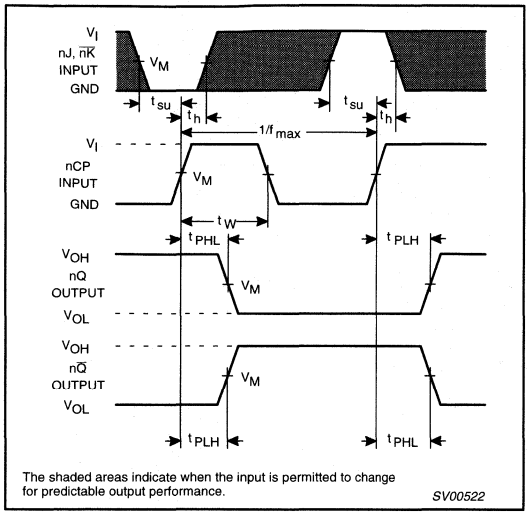


Figure 1. Clock (nCP) to output (nQ, nQ) propagation delays, the clock pulse width, the nJ and nK to nCP set-up, the nCP to nJ, nK hold times and the maximum clock pulse frequency.

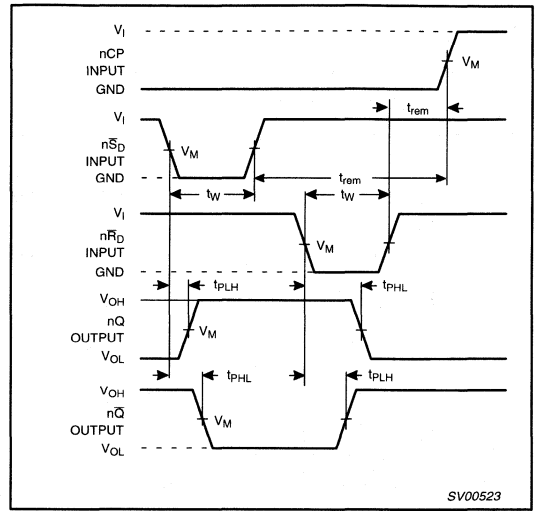
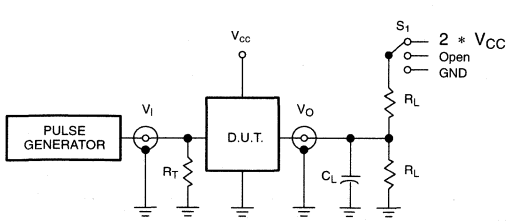
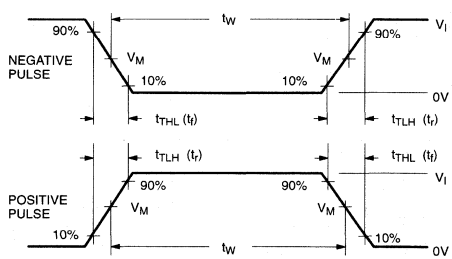


Figure 2. Set ($n\overline{S}_D$) and reset ($n\overline{R}_D$) input to output (nQ, nQ) propagation delays, the set and reset pulse widths and the $n\overline{R}_D$, $n\overline{S}_D$ to nCP removal time.

TEST CIRCUIT



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V
≥ 4.5 V	V_{CC}

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SV00904

Figure 3. Load circuitry for switching times.

Quad buffer/line driver with 5-volt tolerant inputs/outputs (3-state)

74LVC125A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V

DESCRIPTION

The 74LVC125A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-state operation, outputs can handle 5V.

The 74LVC125A consists of four non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3 V Notes 1 and 2	25	pF

NOTES:

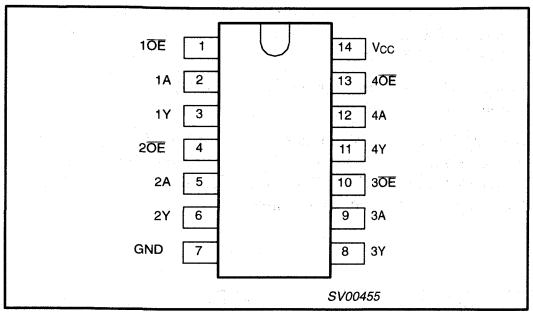
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic SO	–40°C to +125°C	74LVC125A D	74LVC125A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LVC125A DB	74LVC125A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LVC125A PW	7LVC125APW DH	SOT402-1

Quad buffer/line driver with 5-volt tolerant inputs/outputs (3-state) 74LVC125A

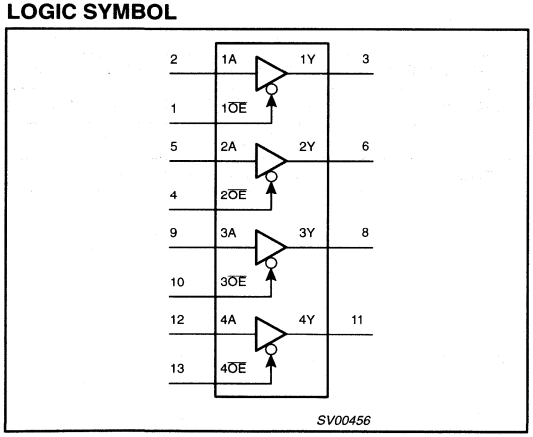
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$1\overline{OE} - 4\overline{OE}$	Data enable inputs (active LOW)
2, 5, 9, 12	1A – 4A	Data inputs
3, 6, 8, 11	1Y – 4Y	Data Outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



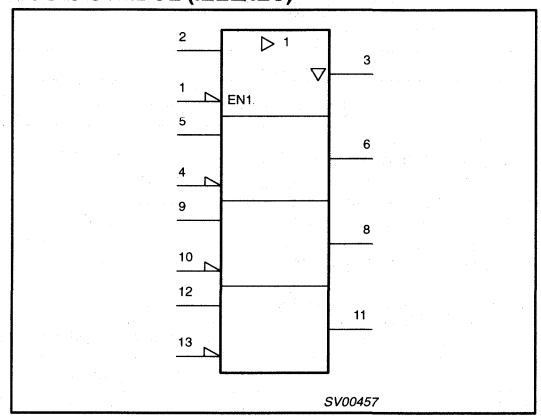
FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

NOTES:

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_{OUT}	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current[2]	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. For I/O ports the parameter I_{OZ} includes the input leakage current.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay nA to nY	Figures 1, 3	1.5	3.0	4.8	1.5	5.5	12.0	ns
t_{PZH} t_{PZL}	3-State output enable time $n\overline{OE}$ to nY	Figures 2, 3	1.5	3.8	5.7	1.5	6.7	13.0	ns
t_{PHZ} t_{PLZ}	3-State output disable time $n\overline{OE}$ to nY	Figures 2, 3	1.5	3.7	5.2	1.5	6.2	8	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 V at V_{CC} > 2.7 V
$V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ − 0.1 V at V_{CC} < 2.7 V

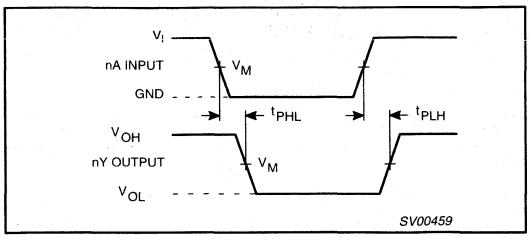


Figure 1. Input (nA) to output (nY) propagation delays.

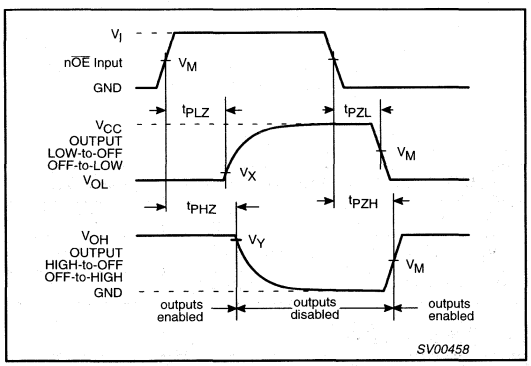
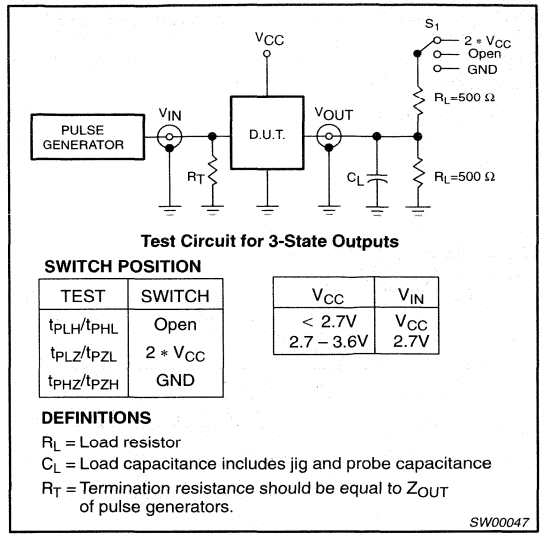


Figure 2. 3-state enable and disable times.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Figure 3. Load circuitry for switching times.

Quad buffer/line driver with 5-volt tolerant inputs/outputs (3-state)

74LVC126A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V

DESCRIPTION

The 74LVC126A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-state operation, outputs can handle 5V.

The 74LVC126A consists of four non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3 V	20	pF

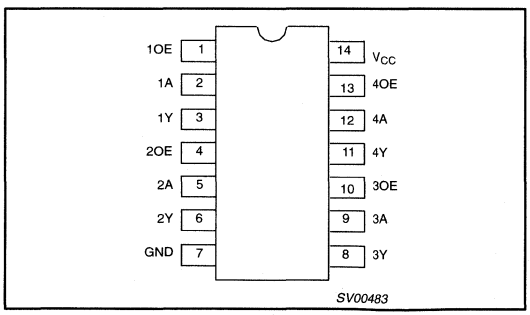
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic SO	–40°C to +125°C	74LVC126A D	74LVC126A D	SOT108-1
14-Pin Plastic SSOP Type II	–40°C to +125°C	74LVC126A DB	74LVC126A DB	SOT337-1
14-Pin Plastic TSSOP Type I	–40°C to +125°C	74LVC126A PW	74LVC126APW DH	SOT402-1

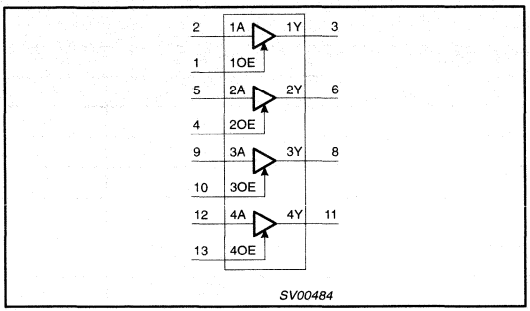
PIN CONFIGURATION



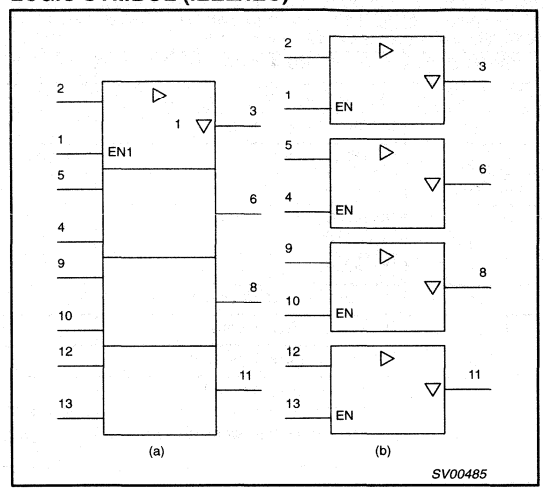
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1OE – 4OE	Data enable inputs (active HIGH)
2, 5, 9, 12	1A – 4A	Data inputs
3, 6, 8, 11	1Y – 4Y	Data Outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



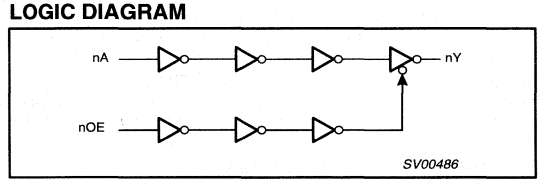
FUNCTION TABLE

INPUTS		OUTPUT
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

NOTES:

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	−0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	−0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 0.0V; V_I or V_O = 5.5V			±5	µA
I_{OFF}	Power off leakage current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay nA to nY	Figures 1, 3	1.5	3.2	5.5	1.5	6.5	13.0	ns
t_{PZH} t_{PZL}	3-state output enable time nOE to nY	Figures 2, 3	1.5	3.9	6.3	1.5	7.3	13.0	ns
t_{PHZ} t_{PLZ}	3-state output disable time nOE to nY	Figures 2, 3	1.5	4.4	6.2	1.5	7.2	10	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V; $V_X = V_{OL} + 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V
$V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7 V; $V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at V_{CC} < 2.7 V

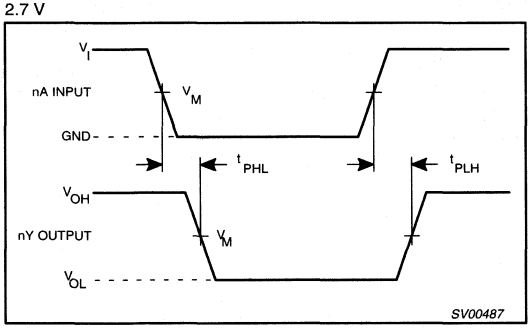


Figure 1. Input (nA) to output (nY) propagation delays.

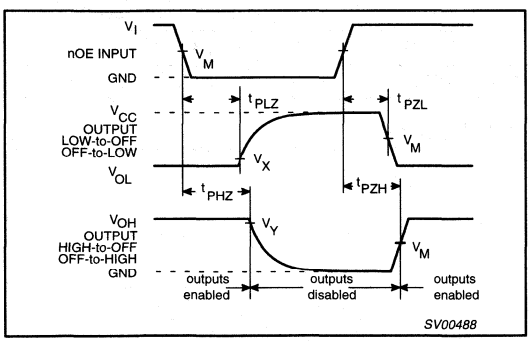
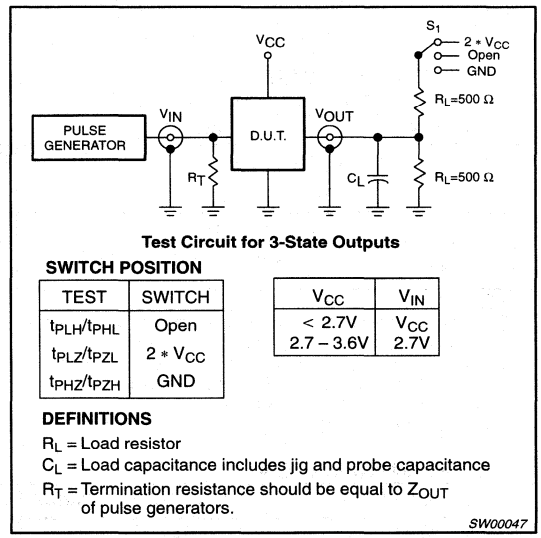


Figure 2. 3-state enable and disable times.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Figure 3. Load circuitry for switching times.

3-to-8 line decoder/demultiplexer; inverting | 74LVC138A

FEATURES

- Wide supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS lower power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 85°C

DESCRIPTION

The 74LVC138A is a low-voltage, low-power, high-performance Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC138A accepts three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provides 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).

The 74LVC138A features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74LV138A to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LV138A ICs and one inverter. The 74LV138A can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to $\overline{Y}n$, E_3 to $\overline{Y}n$, $\overline{E}n$ to $\overline{Y}n$	C_L = 50 pF; V_{CC} = 3.3 V	 3.5 3.5	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per package	V_{CC} = 3.3 V Notes 1 and 2	44	pF

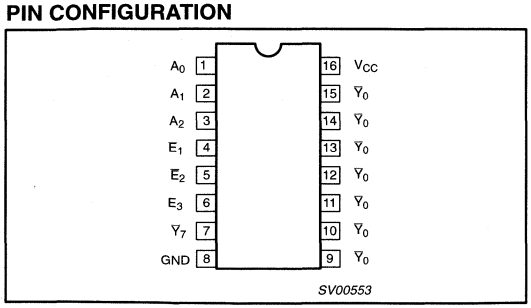
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

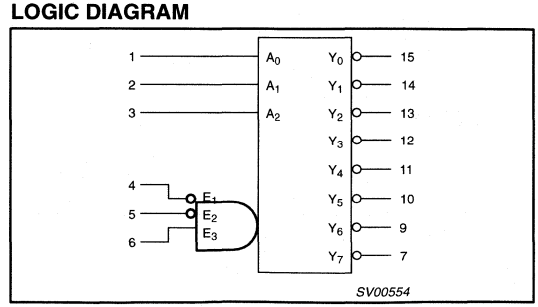
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic SO	–40°C to +85°C	74LVC138A D	74LVC138A D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC138A DB	74LVC138A DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC138A PW	74LVC138APW DH	SOT403-1

PIN CONFIGURATION



SV00553

LOGIC DIAGRAM

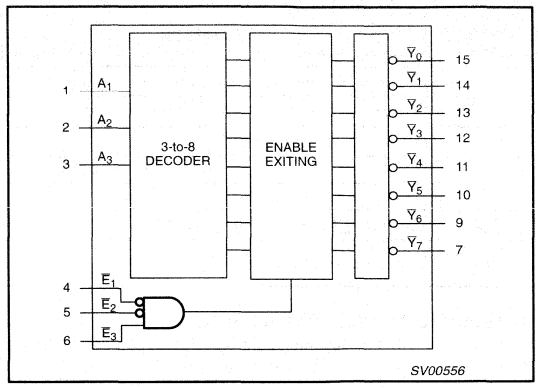


SV00554

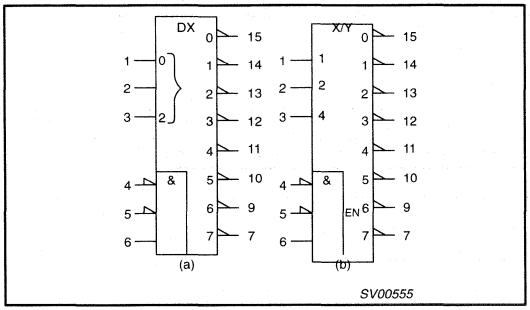
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	Address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	Enable inputs (active LOW)
6	E_3	Enable inputs (active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	Outputs
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES:

H = HIGH voltage level
L = LOW voltage level
X = don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC input voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = –40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay A_n to $\overline{Y}_n$	Figure 1, 3	1.5	3.5	5.8	1.5	6.8	ns
t_{PHL}/t_{PLH}	Propagation delay E_3 to $\overline{Y}_n$	Figure 1, 3	1.5	3.6	5.8	1.5	6.8	ns
t_{PHL}/t_{PLH}	Propagation delay E_n to $\overline{Y}_n$	Figure 2, 3	1.5	3.5	5.8	1.5	6.8	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

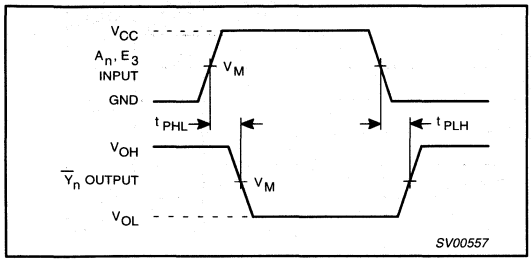


Figure 1. Input (nA) to output (nY) propagation delays.

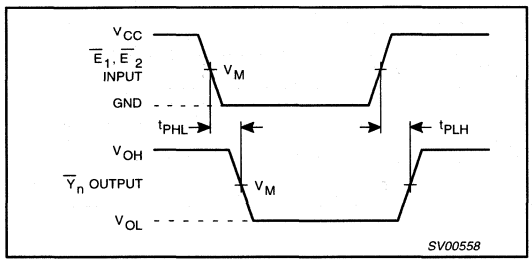


Figure 2. 3-State enable and disable times.

TEST CIRCUIT

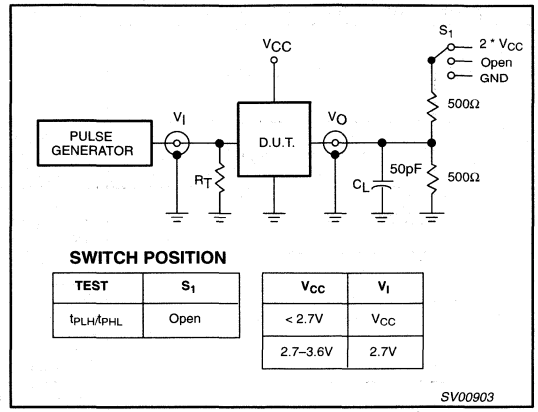


Figure 3. Load circuitry for switching times.

Dual 2-to-4 line decoder/demultiplexer | 74LVC139

FEATURES

- Wide supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS lower power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 85°C

DESCRIPTION

The 74LVC139 is a low-voltage, low-power, high-performance Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW input ($n\overline{E}$).

When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to $n\overline{Y}_n$, $n\overline{E}$ to $n\overline{Y}_n$,	C_L = 50 pF; V_{CC} = 3.3 V	 3.3 3.2	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per multiplexer	V_{CC} = 3.3 V Notes 1 and 2	36	pF

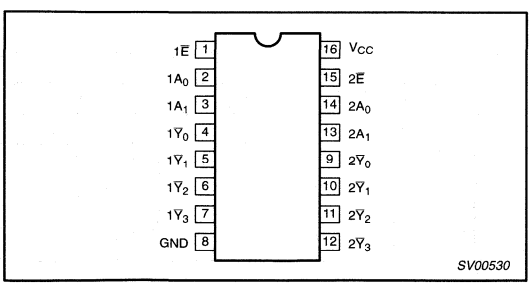
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_1 = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic SO	–40°C to +85°C	74LVC139 D	74LVC139 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC139 DB	74LVC139 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC139 PW	74LVC139PW DH	SOT403-1

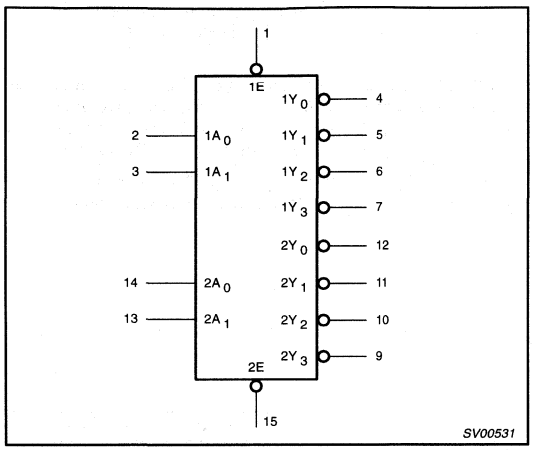
PIN CONFIGURATION



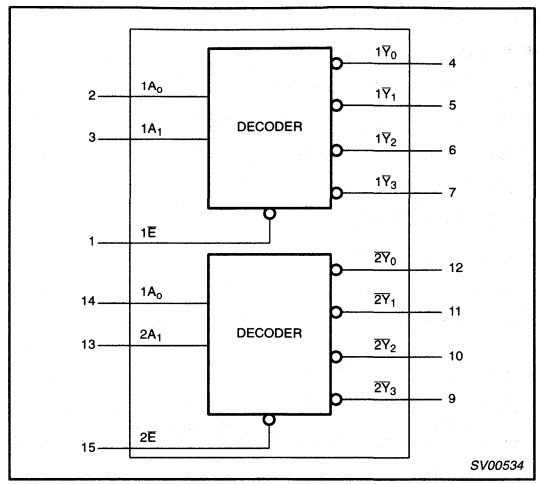
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	Enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	Address inputs
14, 13	$2A_0$, $2A_1$	
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	Outputs (active LOW)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	
8	GND	Ground (0 V)
16	V_{CC}	Positive supply voltage

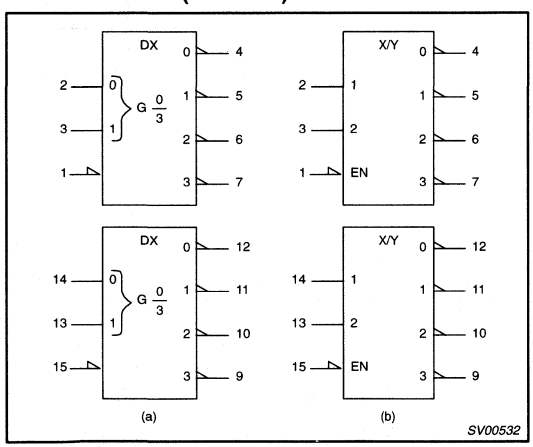
LOGIC DIAGRAM



FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS			OUTPUTS			
$n\overline{E}$	nA_0	nA_1	$n\overline{Y}_0$	$n\overline{Y}_1$	$n\overline{Y}_2$	$n\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range in free air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = –40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA_n to $\overline{Y}_n$	1, 3	1.5	3.3	6.0		7.5	ns
t_{PHL}/t_{PLH}	Propagation delay $n\overline{E}$ to $\overline{Y}_n$	2, 3	1.5	3.2	5.5		6.5	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

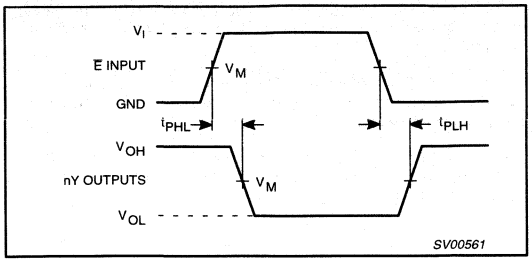


Figure 1. Input (nA) to output (nY) propagation delays.

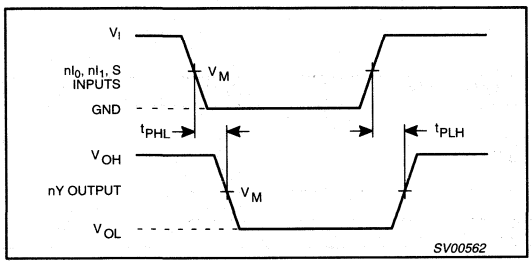
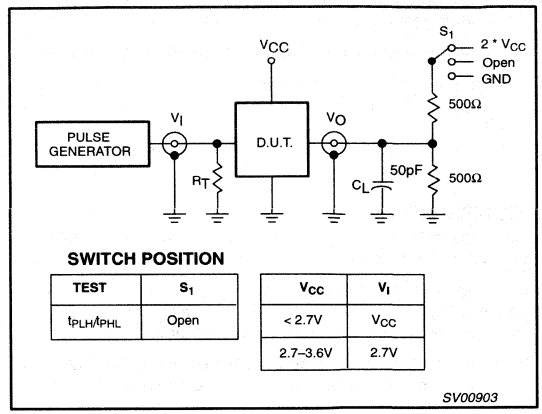


Figure 2. Enable input (nĒ) to output (nȲn) propagation delays.

TEST CIRCUIT



SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Figure 3. Load circuitry for switching times.

Quad 2-input multiplexer | 74LVC157A

FEATURES

- Wide supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- CMOS lower power consumption
- Direct interface with TTL levels
- 5 Volt tolerant inputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC157A is a high-performance, low-power, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC157A is a quad 2-input multiplexer which select 4 bits of data from two sources under the control of a common data select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions. Moving the data from two groups of registers to four common output buses is a common use of the 74LV157. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The 74LVC157A is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nI_0, nI1, to nY $\overline{E}$ to nY S to nY	C_L = 50 pF; V_{CC} = 3.3 V	3.1 3.0 3.3	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	33	pF

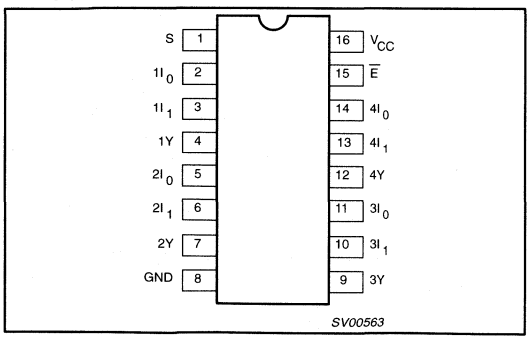
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic SO	–40°C to +85°C	74LVC157A D	74LVC157A D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC157A DB	74LVC157A DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC157A PW	74LVC157APW DH	SOT403-1

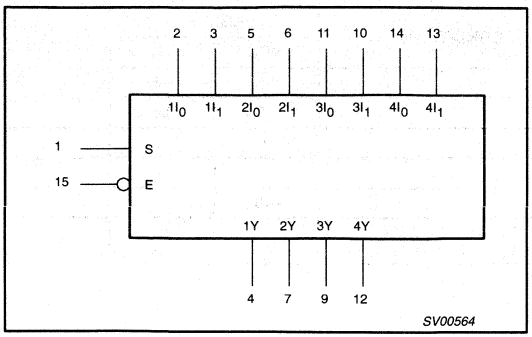
PIN CONFIGURATION



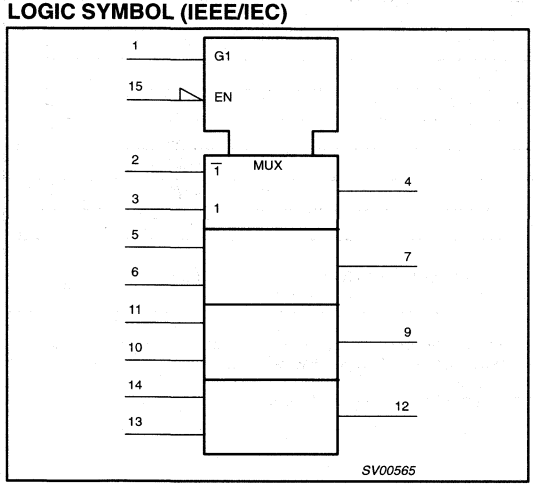
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	S	Common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	Data inputs from sources 0
3, 6, 10, 13	$1I_1$ to $4I_1$	Data inputs from sources 1
4, 7, 9, 12	1Y to 4Y	Multiplexer outputs
8	GND	Ground (0 V)
15	$\overline{E}$	Enable input (active LOW)
16	V_{CC}	Positive supply voltage

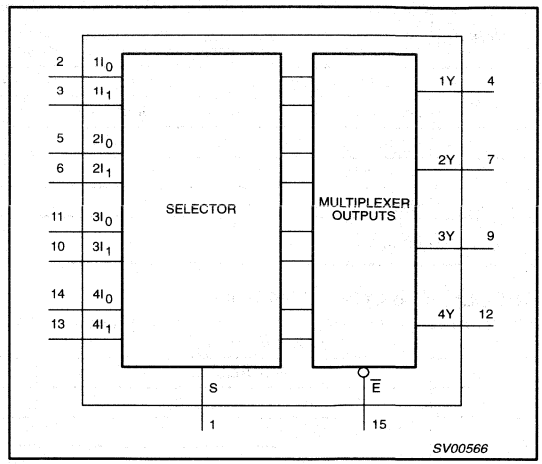
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM

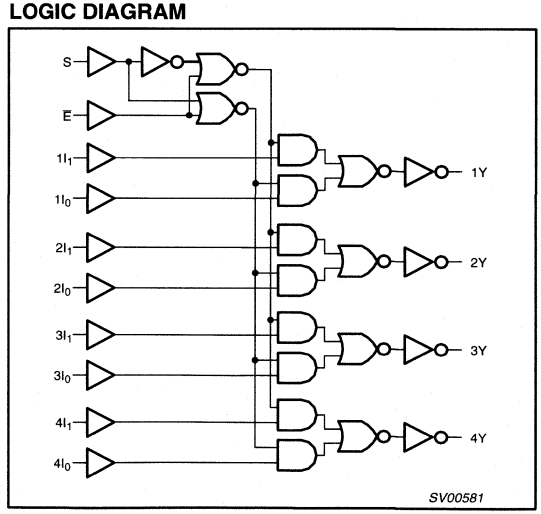


FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{E}$	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output diode current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are measured at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = –40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay nI_0 to nY; nI_1 to nY	Figure 2, 3	1.5	3.1	5.7	1.5	6.7	12	ns
t_{PHL}/t_{PLH}	Propagation delay $\overline{E}$ to nY	Figure 1, 3	1.5	3.0	6.3	1.5	7.3	11	ns
t_{PHL}/t_{PLH}	Propagation delay S to nY	Figure 2, 3	1.5	3.3	6.8	1.5	7.8	13	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$V
$V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

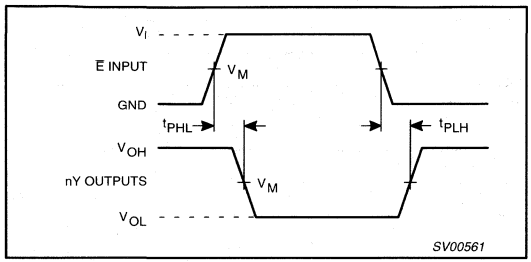


Figure 1. Enable input ($\overline{E}$) to output (nY) propagation delays.

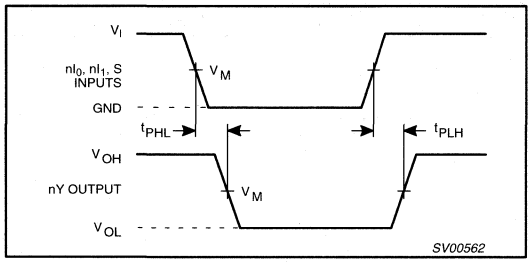
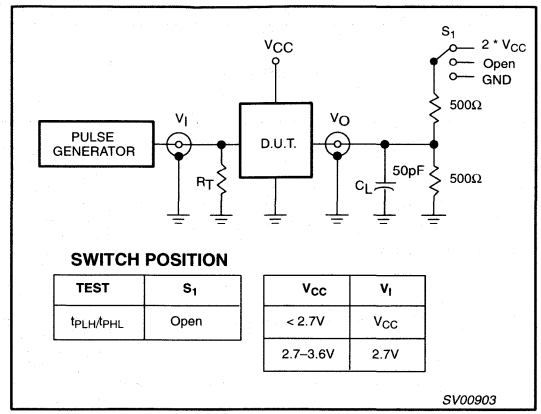


Figure 2. Data inputs (nI_0, nI_1) and common data select input (S) to output (nY) propagation delays.

TEST CIRCUIT



SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Figure 3. Load circuitry for switching times.

Presettable synchronous 4-bit binary counter; asynchronous reset

74LVC161

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8–1A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Asynchronous reset
- Synchronous counting and loading
- Two count enable inputs for n–bit cascading
- Positive edge–triggered clock
- Output drive capability 50 Ω transmission lines @85°C

DESCRIPTION

The 74LVC161 is a high–performance, low–power, low–voltage, Si–gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC161 is a synchronous presettable binary counter which features an internal look–head carry and can be used for high–speed counting. Synchronous operation is provided by having all flip–flops clocked simultaneously on the positive–going edge of the clock (CP). The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive–going edge of the clock (provided that the set–up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input (MR) sets all four outputs of the flip–flops (Q_0 to Q_3) to LOW level regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

The look–ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set–up time, according to the following formula:

$$f_{max} = \frac{1}{t_{p(max)}\ (\text{CP to TC}) + t_{SU}\ (\text{CEP to CP})}$$

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $T_R = T_F \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n CP to TC $\overline{MR}$ to Q_n $\overline{MR}$ to TC CET to TC	C_L = 50 pF V_{CC} = 3.3V	 4.9 5.7 5.2 5.7 4.5	ns
f_{MAX}	maximum clock frequency		200	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	39	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. The condition is V_1 = GND to V_{CC}

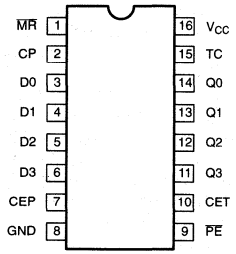
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
16-Pin Plastic SO	–40°C to +85°C	74LVC161 D	74LVC161 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC161 DB	74LVC161 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC161 PW	74LVC161PW DH	SOT403-1

Presettable synchronous 4-bit binary counter; asynchronous reset

74LVC161

PIN CONFIGURATION

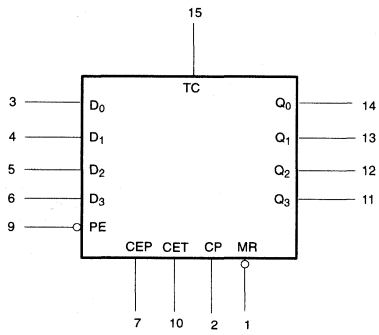


SF00656

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3,4,5,6	D_0 to D_3	data inputs
7	CEP	count enable inputs
8	GND	ground (0V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14,13,12,11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

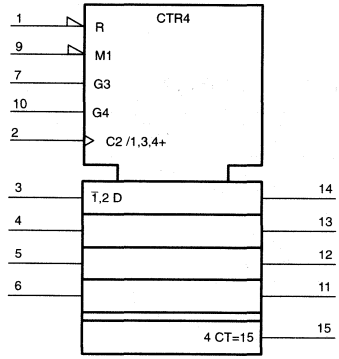
LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

SY00065

LOGIC SYMBOL (IEEE/IEC)

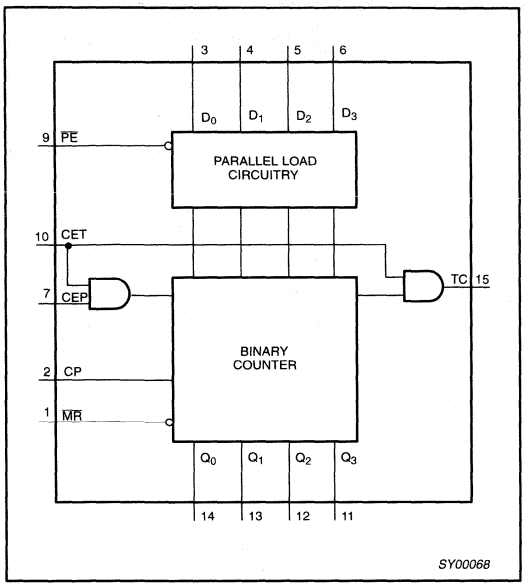


SY00066

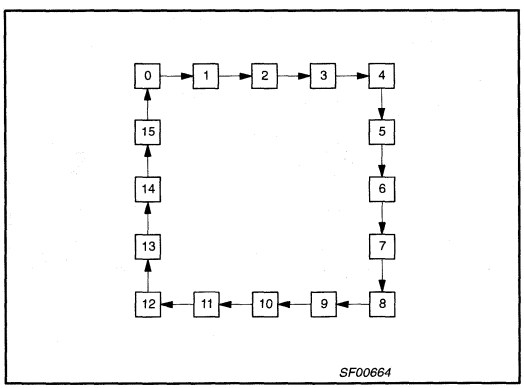
Presettable synchronous 4-bit binary counter; asynchronous reset

74LVC161

FUNCTIONAL DIAGRAM



STATE DIAGRAM



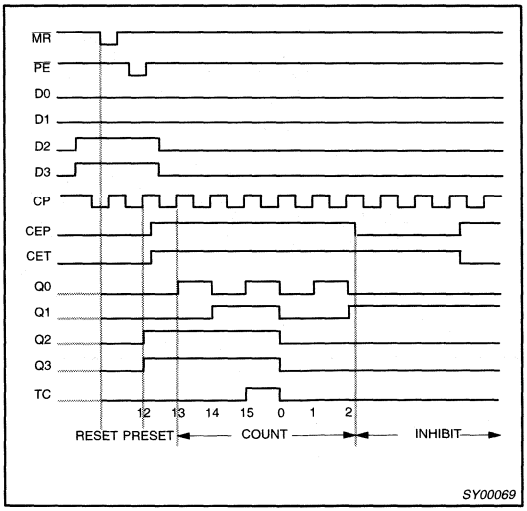
FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
Count	H	↑	h	h	h	X	count	*
Hold	H	X	l	X	h	X	q_n	*
(do nothing)	H	X	X	l	h	X	q_n	L

NOTES:

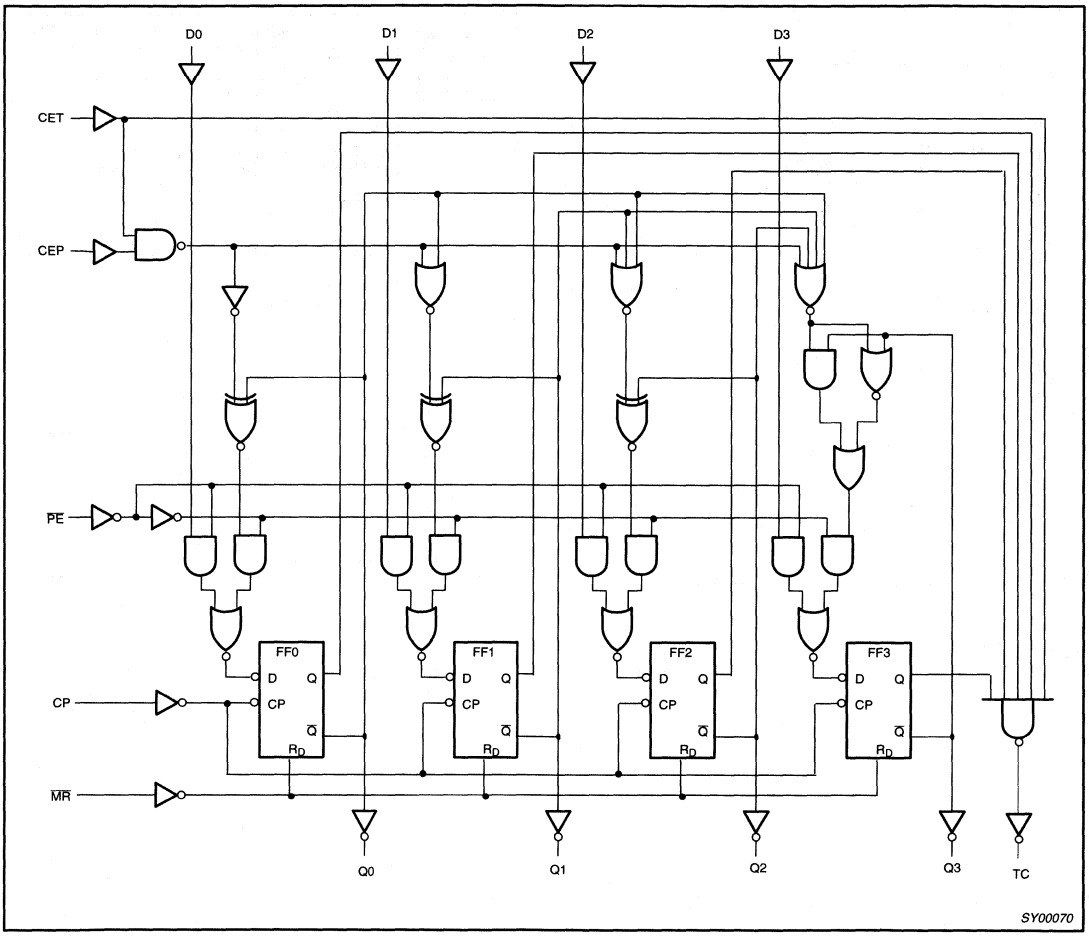
* = The TC output is High when CET is High and the counter is at Terminal Count (HHHH)
H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

TYPICAL TIMING SEQUENCE



Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one, and two; inhibit

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		−40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	−0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$

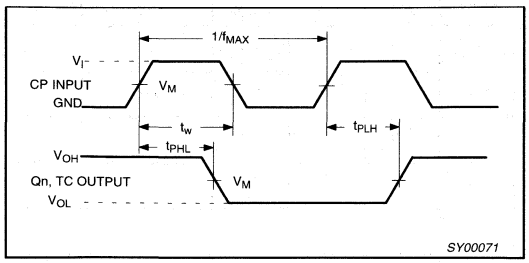
SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		$V_{CC} = 1.2V$	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay CP to Qn	1	–	4.9	8.0	–	9.0	24	ns
t_{PHL} t_{PLH}	Propagation delay CP to TC	1	–	5.7	9.5	–	11	28	ns
t_{PHL} t_{PLH}	Propagation delay CET to TC	2	–	4.5	7.8	–	8.8	22	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	3	–	5.2	9.0	–	10	28	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	3	–	5.7	10	–	11	20	ns
t_W	Clock pulse width HIGH or LOW	1	4.0	1.2	–	5.0	–	–	ns
t_W	Master reset width LOW	3	3.0	1.6	–	4.0	–	–	ns
t_{rem}	Removal time $\overline{MR}$ to CP	3	0	–0.3	–	0	–	–	ns
t_{su}	Set-up time D_n to CP	4	2.5	1.0	–	3.0	–	–	ns
t_{su}	Set-up time $\overline{PE}$ to CP	4	3.0	1.2	–	3.5	–	–	ns
t_{su}	Set-up time CEP, CET to CP	5	5.0	2.1	–	5.5	–	–	ns
t_h	Hold time D_n, $\overline{PE}$, CEP, CET to CP	4, 5	0	–1.7	–	0	–	–	ns
f_{max}	Maximum clock pulse frequency	1	125	200	–	110	–	–	MHz

NOTE:

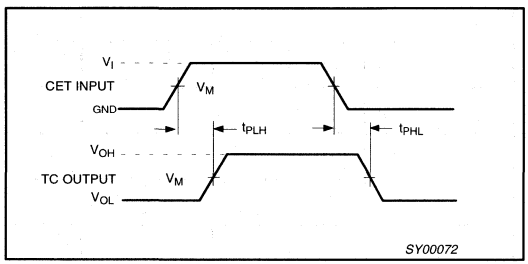
1. These typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25°C$.

AC WAVEFORMS

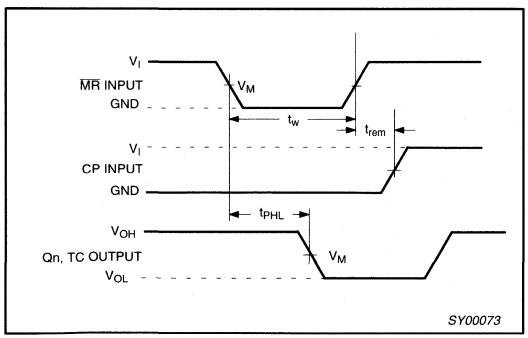
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



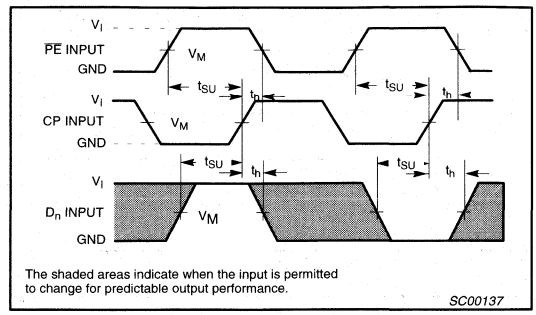
Waveform 1. Clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width and the maximum clock frequency.



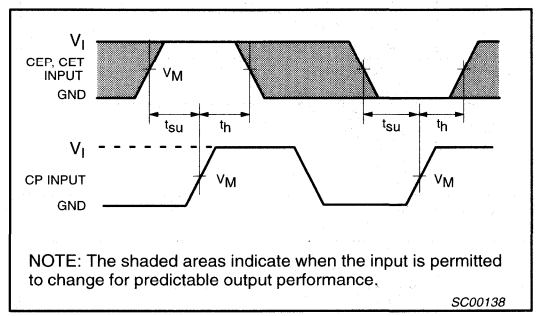
Waveform 2. Input (CET) to output (TC) propagation delays.



Waveform 3. Master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n, TC) propagation delays and the master reset to clock (CP) removal times.

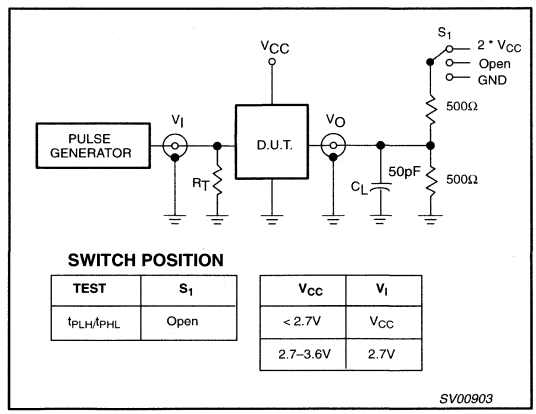


Waveform 4. Setup and hold times for the input (D_n) and parallel enable input ($\overline{PE}$).



Waveform 5. CEP and CET setup and hold times.

TEST CIRCUIT



SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Waveform 6. Load circuitry for switching times.

Presettable synchronous 4-bit binary counter; synchronous reset

74LVC163

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8–1A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Synchronous reset
- Synchronous counting and loading
- Two count enable inputs for n–bit cascading
- Positive edge–triggered clock

DESCRIPTION

The 74LVC163 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC163 is a synchronous presettable binary counter which features an internal look–head carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive–going edge of the clock (provided that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input (MR) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for PE are met).

This action occurs regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The look–ahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set–up time, according to the following formula:

$$f_{max} = \frac{1}{t_{p(max)}\ (\text{CP to TC}) + t_{SU}\ (\text{CEP to CP})}$$

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $T_R = T_F \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n CP to TC CET to TC	C_L = 50 pF V_{CC} = 3.3V	 4.9 5.7 4.5	ns
f_{MAX}	maximum clock frequency		200	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	39	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. The condition is V_1 = GND to V_{CC}

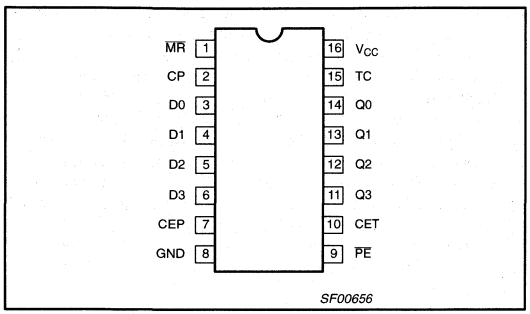
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
16-Pin Plastic SO	–40°C to +85°C	74LVC163 D	74LVC163 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC163 DB	74LVC163 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC163 PW	74LVC163PW DH	SOT403-1

Presettable synchronous 4-bit binary counter; synchronous reset

74LVC163

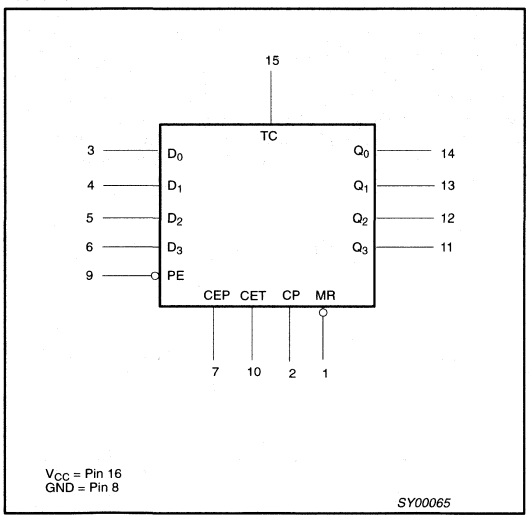
PIN CONFIGURATION



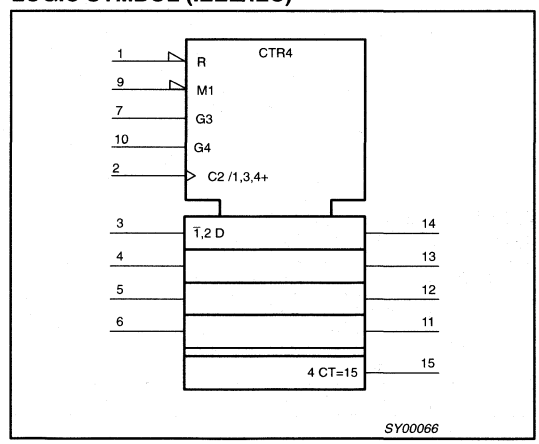
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3,4,5,6	D_0 to D_3	data inputs
7	CEP	count enable inputs
8	GND	ground (0V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
14,13,12,11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output
16	V_{CC}	positive supply voltage

LOGIC SYMBOL



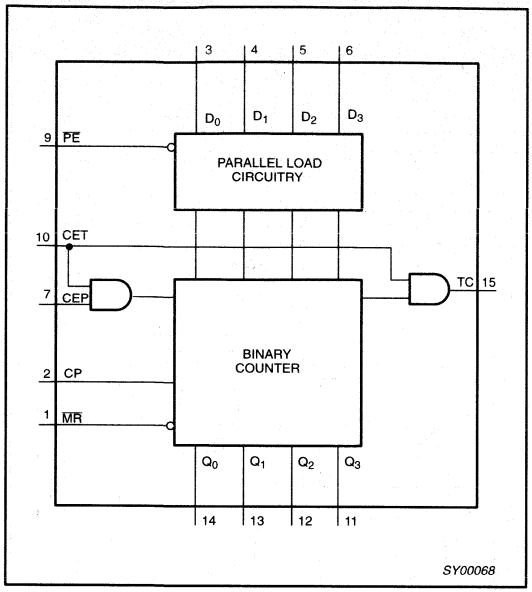
LOGIC SYMBOL (IEEE/IEC)



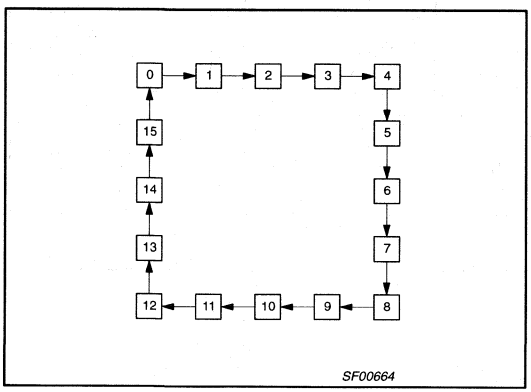
Presettable synchronous 4-bit binary counter; synchronous reset

74LVC163

FUNCTIONAL DIAGRAM



STATE DIAGRAM



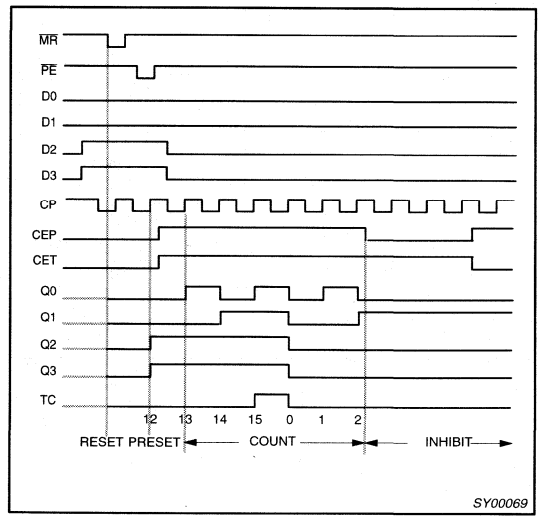
FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	*
Count	h	↑	h	h	h	X	count	*
Hold (do nothing)	h	X	l	X	h	X	q_n	*
	h	X	X	l	h	X	q_n	L

NOTES:

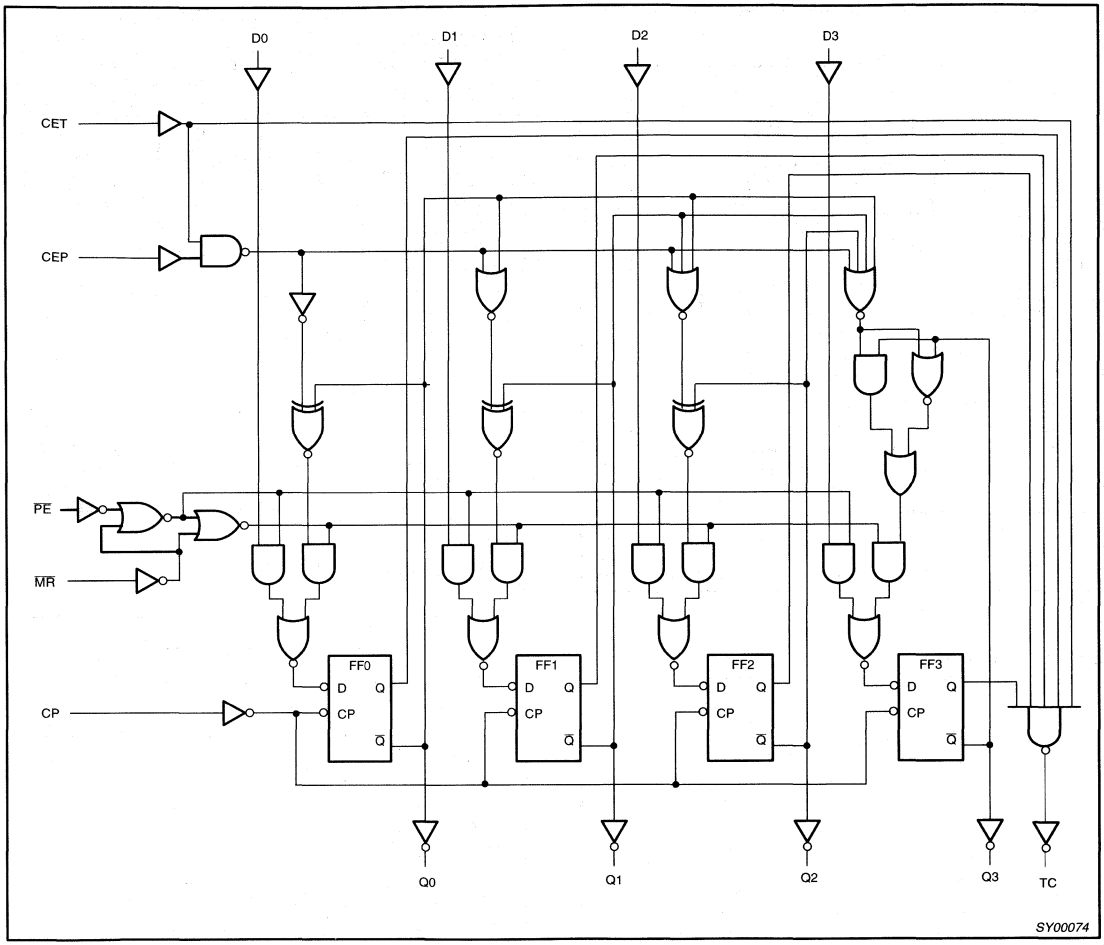
* = The TC output is High when CET is High and the counter is at Terminal Count (HHHH)
H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

TYPICAL TIMING SEQUENCE



Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one, and two; inhibit

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		−40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	−0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = –40°C to +85°C

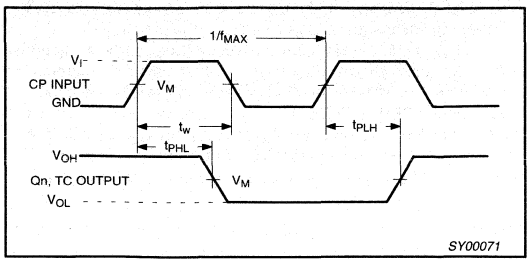
SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay CP to Qn	1	–	4.9	8.0	–	9.0	24	ns
t_{PHL} t_{PLH}	Propagation delay CP to TC	1	–	5.7	9.5	–	11	28	ns
t_{PHL} t_{PLH}	Propagation delay CET to TC	2	–	4.5	7.8	–	8.8	19	ns
t_W	Clock pulse width HIGH or LOW	1	4.0	1.2	–	5.0	–	–	ns
t_{su}	Set-up time D_n to CP	3, 4	2.5	1.0	–	3.0	–	–	ns
t_{su}	Set-up time $\overline{MR}$, $\overline{PE}$ to CP	4	3.0	1.2	–	3.5	–	–	ns
t_{su}	Set-up time CEP, CET to CP	5	5.0	2.1	–	5.5	–	–	ns
t_h	Hold time D_n, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP	3, 4, and 5	0	–1.7	–	0	–	–	ns
f_{max}	Maximum clock pulse frequency	1	125	200	–	110	–	–	MHz

NOTE:

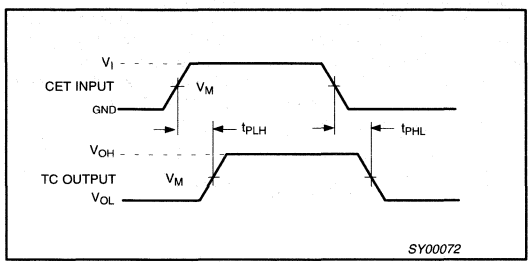
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

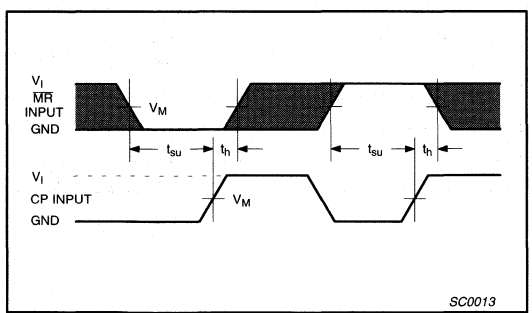
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



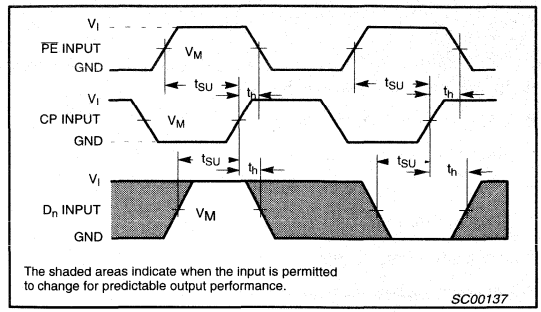
Waveform 1. Clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width and the maximum clock frequency.



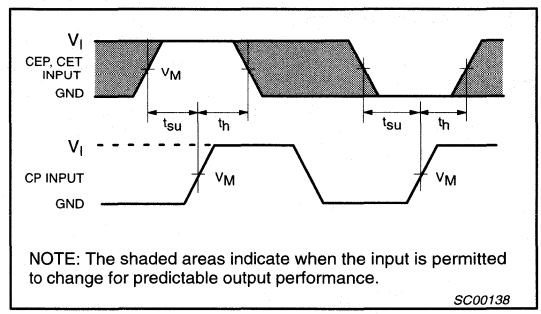
Waveform 2. Input (CET) to output (TC) propagation delays.



Waveform 3. Master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n, TC) propagation delays and the master reset to clock (CP) removal times.

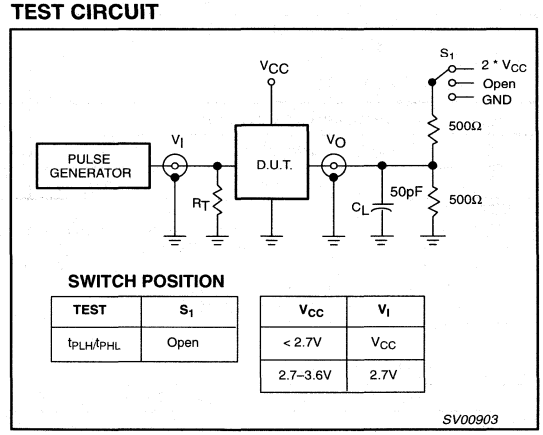


Waveform 4. Setup and hold times for the input (D_n) and parallel enable input ($\overline{PE}$).



Waveform 5. CEP and CET setup and hold times.

TEST CIRCUIT



Waveform 6. Load circuitry for switching times.

Presettable synchronous 4-bit up/down binary counter

74LVC169

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Synchronous counting and loading
- Up/down counting
- Modular 16 binary counter
- Two count enable inputs for n-bit cascading
- Built-in lookahead carry capability
- Presettable for programmable operation
- Positive-edge triggered clock

DESCRIPTION

The 74LVC169 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC169 is a synchronous presettable binary counter which features an internal lookahead carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q_0 to Q_3) of the counters may be preset to a HIGH or LOW level. A LOW level at the parallel enable input (PE) disables the counting action and causes the data at the data inputs (D_0 to D_3) to be loaded into the counter on the positive-going edge of the clock (provided that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (CEP and CET). A low level at the master reset input (MR) sets all four outputs of the flip-flops (Q_0 to Q_3) to LOW level after the next positive-going transition on the clock (CP) input (provided that the set-up and hold time requirements for PE are met).

This action occurs regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The lookahead carry simplifies serial cascading of the counters. Both count enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula:

$$f_{max} = \frac{1}{t_{p(max)}\ (\text{CP to TC}) + t_{SU}\ (\text{CEP to CP})}$$

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $T_R = T_F \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n CP to $\overline{TC}$ $\overline{CET}$ to $\overline{TC}$	C_L = 50 pF V_{CC} = 3.3V	 5.0 6.5 5.3	ns
f_{MAX}	maximum clock frequency		200	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	42	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
2. The condition is V_1 = GND to V_{CC}

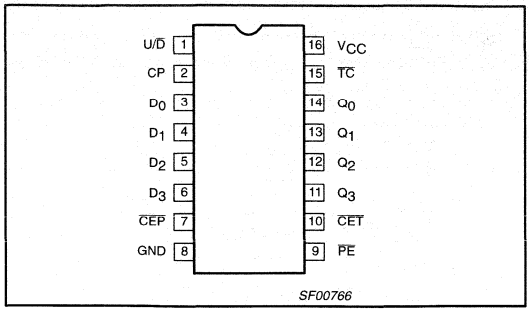
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
16-Pin Plastic SO	–40°C to +85°C	74LVC169 D	74LVC169 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC169 DB	74LVC169 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC169 PW	74LVC169PW DH	SOT403-1

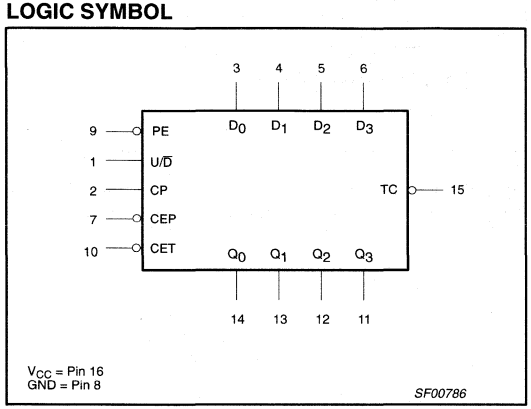
Presettable synchronous 4-bit up/down binary counter

74LVC169

PIN CONFIGURATION



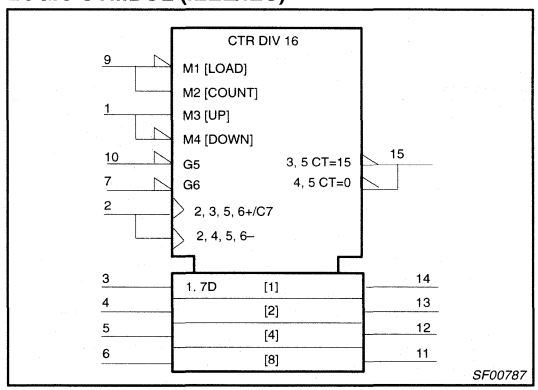
LOGIC SYMBOL



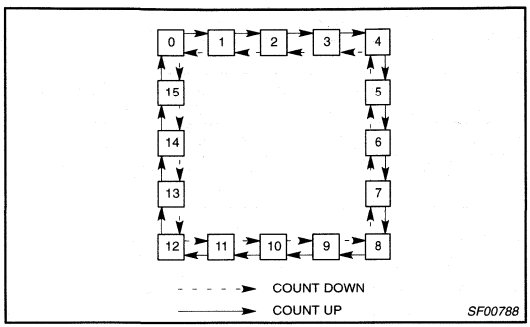
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$U/\overline{D}$	up/down control input
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3,4,5,6	D_0 to D_3	data inputs
7	CEP	count enable inputs (active LOW)
8	GND	ground (0V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input (active LOW)
14,13,12,11	Q_0 to Q_3	flip-flop outputs
15	TC	terminal count output (active LOW)
16	V_{CC}	positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



STATE DIAGRAM

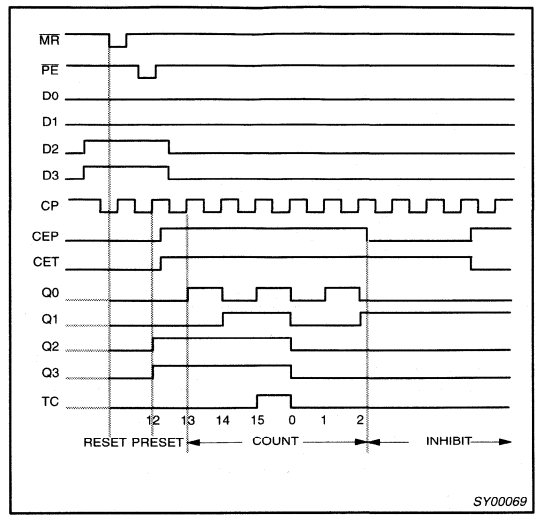


FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS	
	CP	U/D	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel load (Dn→Qn)	↑	X	X	X	l	l	L	*
	↑	X	X	X	X	X	H	*
Count Up (increment)	↑	h	l	l	h	X	Count Up	*
Count Down (decrement)	↑	l	l	l	h	X	Count Down	*
Hold (do nothing)	↑	X	h	X	h	X	q_n	*
	↑	X	X	X	h	X	q_n	H

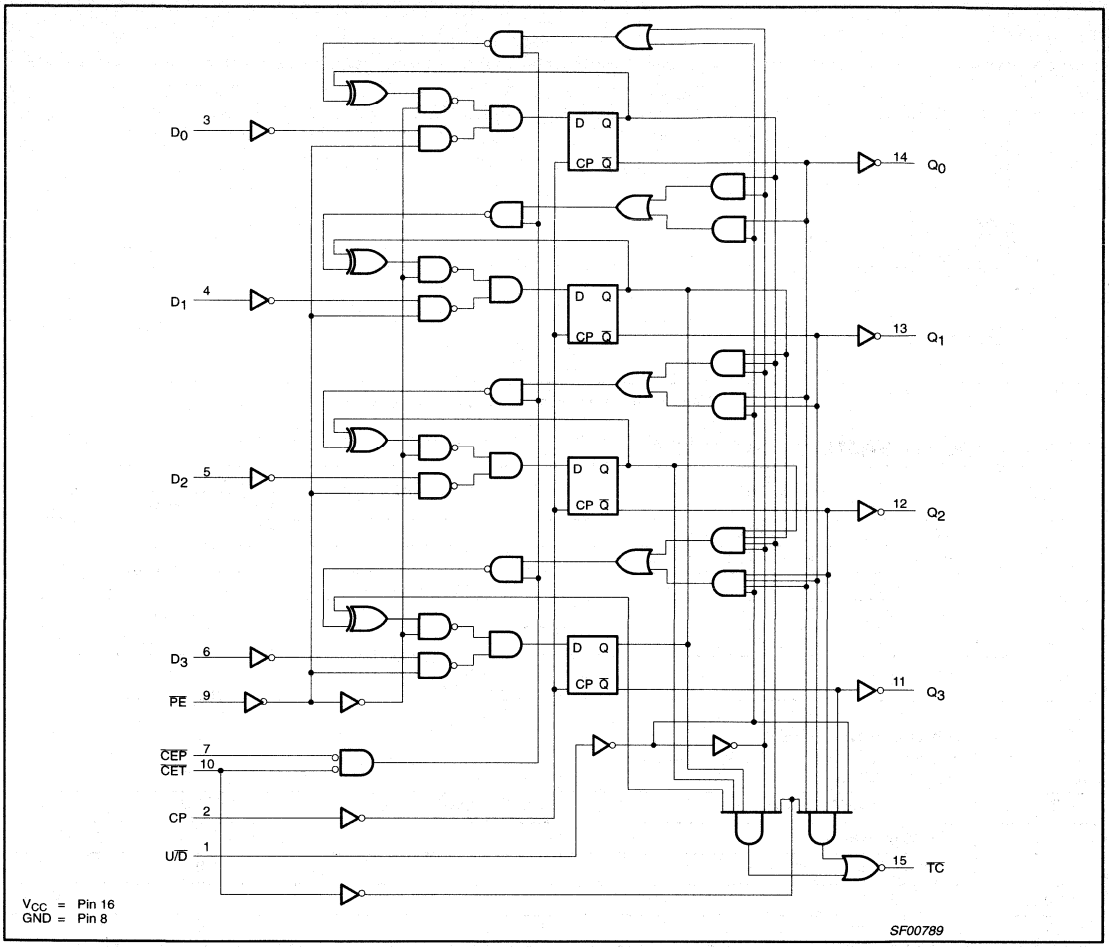
H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
* = The $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count.
Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL).

TYPICAL TIMING SEQUENCE

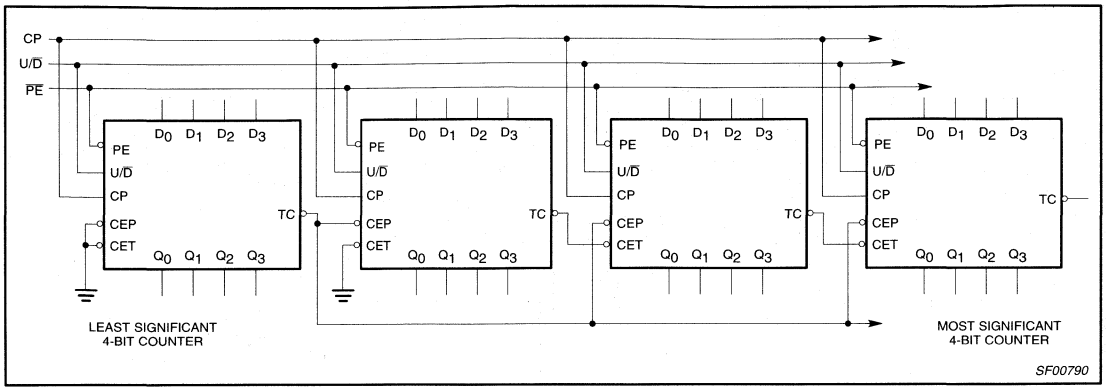


Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one, and two; inhibit

LOGIC DIAGRAM



APPLICATION



Synchronous multistage counting scheme

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$

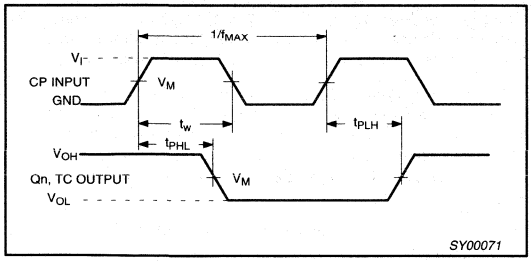
SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN.	TYP[1]	MAX.	MIN.	MAX.	TYP	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	1	-	5.0	8.5	-	9.5	24	ns
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{TC}$	1	-	6.5	10.8	-	12.8	30	ns
t_{PHL}/t_{PLH}	propagation delay $\overline{CET}$ to $\overline{TC}$	2	-	5.3	8.7	-	9.7	19	ns
t_{PHL}/t_{PLH}	propagation delay U/$\overline{D}$ to $\overline{TC}$	4	-	5.7	9.5	-	10.5	24	ns
t_W	clock pulse width HIGH or LOW	1	4.0	1.2	-	5.0	-	-	ns
t_{su}	set-up time D_n to CP	3	2.5	1.0	-	3.0	-	-	ns
t_{su}	set-up time $\overline{PE}$ to CP	3	3.0	1.2	-	3.5	-	-	ns
t_{su}	set-up time U/$\overline{D}$ to CP	5	5.5	2.8	-	6.5	-	-	ns
t_{su}	set-up time $\overline{CEP}$, $\overline{CET}$ to CP	5	4.5	2.1	-	5.5	-	-	ns
t_h	hold time D_n, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$, U/$\overline{D}$ to CP	3 and 5	0	−2.5	-	0	-	-	ns
f_{max}	maximum clock pulse frequency	1	125	200	-	110	-	-	MHz

NOTE:

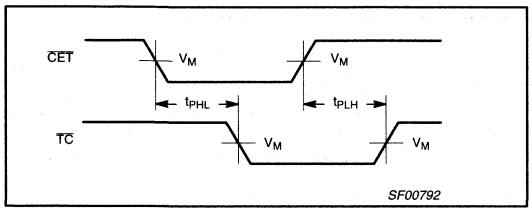
1. These typical values are measured at $V_{CC} = 3.3$V and $T_{amb} = 25°C$.

AC WAVEFORMS

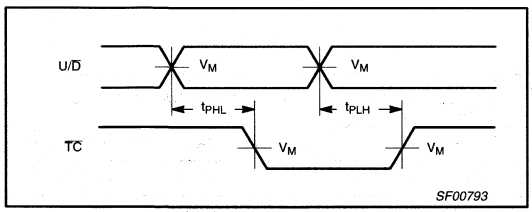
V_M = 1.5 V at V_{CC} ≥ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



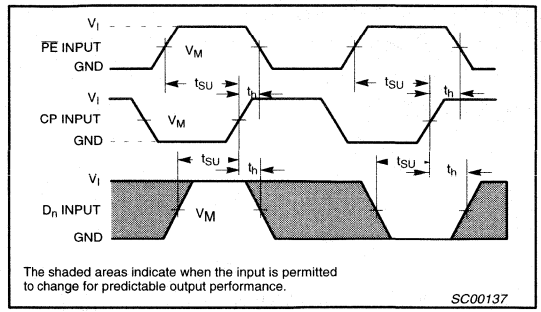
Waveform 1. Clock (CP) to outputs (Q_n, TC) propagation delays, the clock pulse width and the maximum clock frequency.



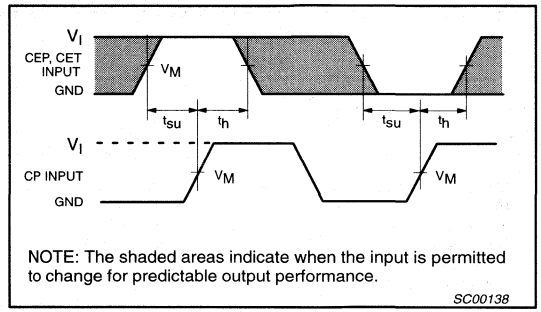
Waveform 2. Input (CET) to output (TC) propagation delays and output transition times.



Waveform 3. Master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n, TC) propagation delays and the master reset to clock (CP) removal times.

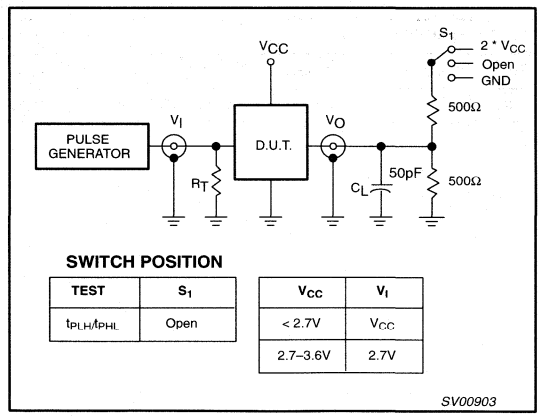


Waveform 4. Setup and hold times for the input (D_n) and parallel enable input ($\overline{PE}$).



Waveform 5. CEP and CET setup and hold times.

TEST CIRCUIT



Waveform 6. Load circuitry for switching times.

Octal buffer/line driver with 5-volt tolerant inputs/outputs; inverting (3-State)

74LVC240A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V

DESCRIPTION

The 74LVC240A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices as translators in a mixed 3.3V/5V environment.

The '240A is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

The '240' is functionally identical to the '244', but the '244' has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50pF V_{CC} = 3.3V	3.5	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 2 and 3	20	pF

NOTE:

2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
3. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Small Outline (SO)	–40°C to +85°C	74LVC240A D	74LVC240A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVC240A DB	74LVC240A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVC240A PW	7LVC240APW DH	SOT360-1

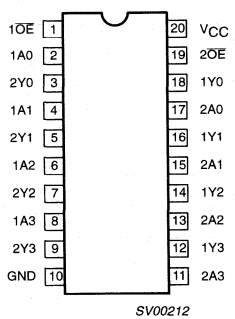
Octal buffer/line driver with 5-volt tolerant inputs/outputs; inverting (3-State)

74LVC240A

PIN DESCRIPTION

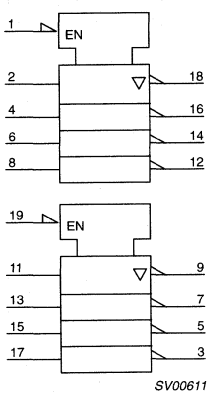
PIN NUMBER	SYMBOL	FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	Data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	Bus outputs
10	GND	Ground (0V)
17, 15, 13, 11	$2A_0$ to $2A_3$	Bus inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	Bus outputs
19	$\overline{2OE}$	Output enable input (active-LOW)
20	V_{CC}	Positive power supply

PIN CONFIGURATION



SV00212

LOGIC SYMBOL (IEEE/IEC)



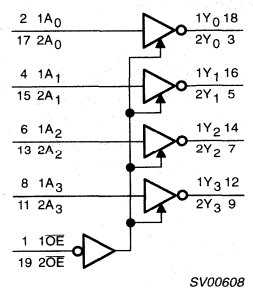
SV00611

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

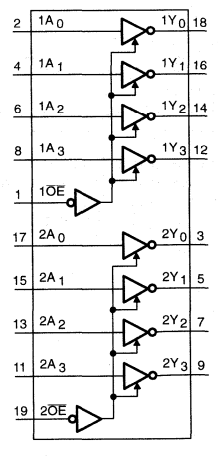
H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

LOGIC SYMBOL



SV00608

FUNCTIONAL DIAGRAM



SV00610

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC Output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current[2]	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{off}	Power off leakage current	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

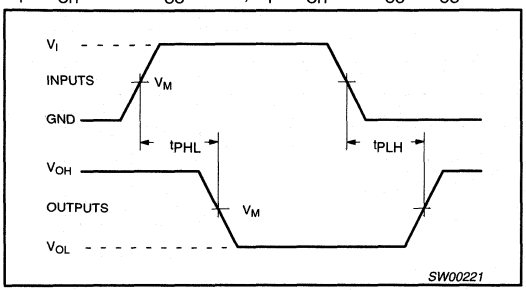
GND = 0V; $t_r = t_f \leq$ 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PLH} t_{PHL}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	1, 3	1.5	3.5	6.5	1.5	7.5	16.0	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{1OE}$ to $1Y_n$; $\overline{2OE}$ to $2Y_n$	2, 3	1.5	4.3	8.0	1.5	9.0	19.0	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{1OE}$ to $1Y_n$; $\overline{2OE}$ to $2Y_n$	2, 3	1.5	3.7	7.0	1.5	8.0	17.0	ns

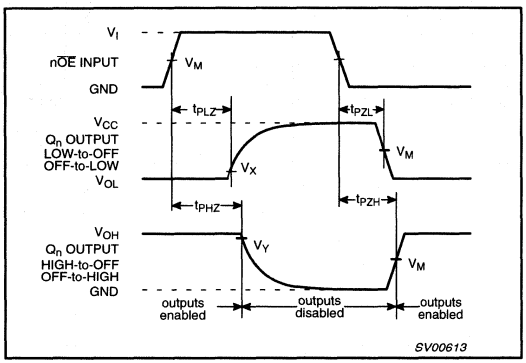
NOTE:
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at V_{CC} ≥ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V

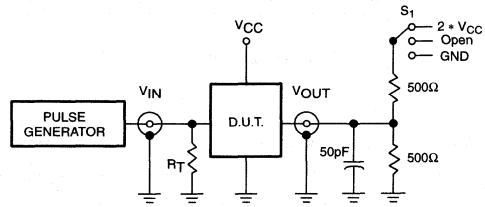


Waveform 1. Inputs ($1A_n$, $2A_n$) to outputs ($1Y_n$, $2Y_n$) propagation delays.



Waveform 2. 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00233

Waveform 3. Load circuitry for switching times.

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC241A

FEATURES

- 5-Volt tolerant inputs/outputs, for interfacing with 5-volt logic.
- Supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- CMOS lower power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0 V

DESCRIPTION

The 74LVC241A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-State operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC241A is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

QUICK REFERENCE DATA

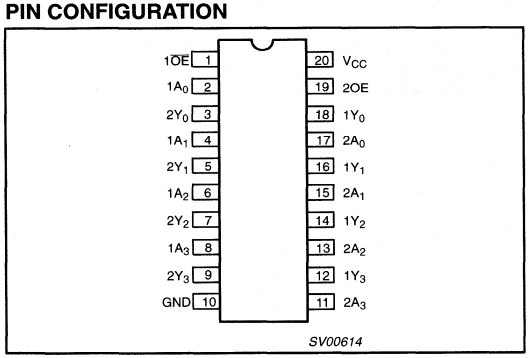
GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50 pF; V_{CC} = 3.3 V	3.2	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3 V	25	pF

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic SO	–40°C to +85°C	74LVC241A D	74LVC241A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC241A DB	74LVC241A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC241A PW	7LVC241APW DH	SOT360-1

PIN CONFIGURATION



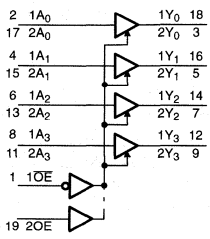
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	Data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	Bus outputs
10	GND	Ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	Data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	Bus outputs
19	2OE	Output enable input (active HIGH)
20	V_{CC}	Positive supply voltage

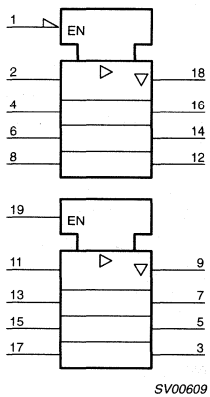
Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC241A

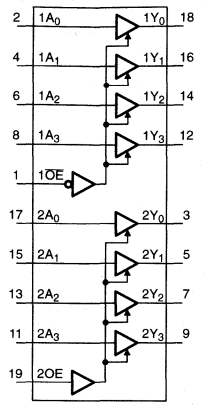
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	2OE	$2A_n$	$1Y_n$	$2Y_n$
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range;output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range;output 3-state		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage;output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage;output 3-state	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = –40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	Figures 1, 4	1.5	3.2	6.1	1.5	7.1	11	ns
t_{PZH}/t_{PZL}	3-State output enable time $1\overline{OE}$ to $1Y_n$	Figures 2, 4	1.5	3.8	7.1	1.5	8.1	13	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $1\overline{OE}$ to $1Y_n$	Figures 2, 4	1.5	3.7	6.0	1.5	7.0	8	ns
t_{PZH}/t_{PZL}	3-State output enable time 2OE to $2Y_n$	Figures 3, 4	1.5	3.6	7.1	1.5	8.1	13	ns
t_{PHZ}/t_{PLZ}	3-State output disable time 2OE to $2Y_n$	Figures 3, 4	1.5	3.6	6.0	1.5	7.0	8	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V
$V_x = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_x = V_{OL}$ + 0.1 V × V_{CC} at V_{CC} < 2.7 V
$V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ − 0.1 × V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

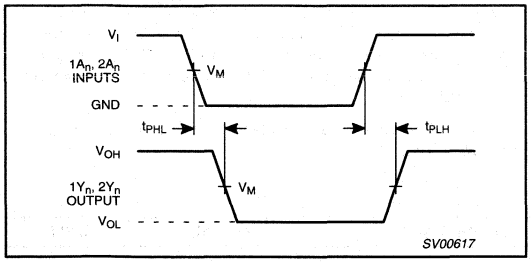


Figure 1. Input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays.

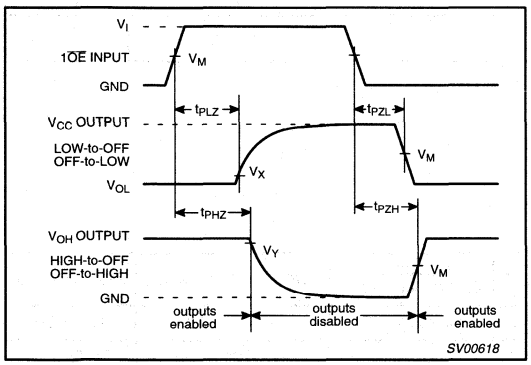


Figure 2. 3-state enable and disable times for input $1\overline{OE}$.

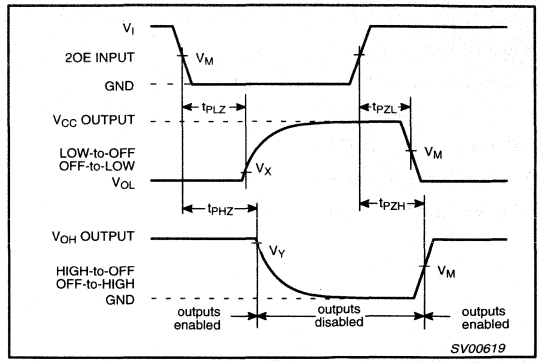
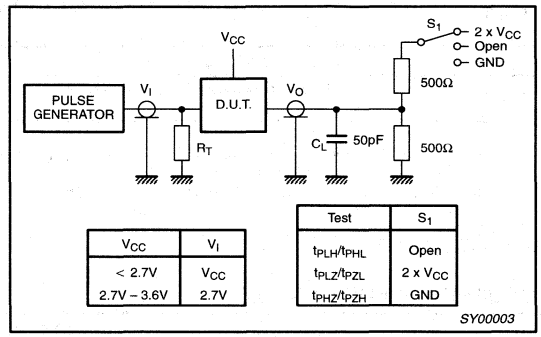


Figure 3. 3-state enable and disable times for input 2OE.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 4. Load circuitry for switching times.

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A
74LVCH244A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V
- Bushold on all data inputs (74LVCH244A only)

DESCRIPTION

The 74LVC244A/74LVCH244A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC244A/74LVCH244A is an octal non-inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

The '244' is functionally identical to the '240', but the '240' has non-inverting outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50pF V_{CC} = 3.3V	3.5	ns
C_I	Input capacitance		4.4	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1 and 2	22.6	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	–40°C to +85°C	74LVC244A D	74LVC244A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVC244A DB	74LVC244A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVC244A PW	7LVC244APW DH	SOT360-1
20-Pin Plastic Shrink Small Outline (SO)	–40°C to +85°C	74LVCH244A D	74LVCH244A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVCH244A DB	74LVCH244A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVCH244A PW	LVCH244APW DH	SOT360-1

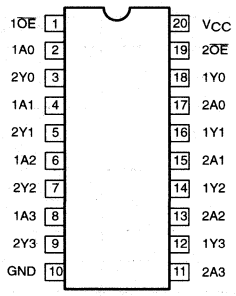
Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC244A
74LVCH244A

PIN DESCRIPTION

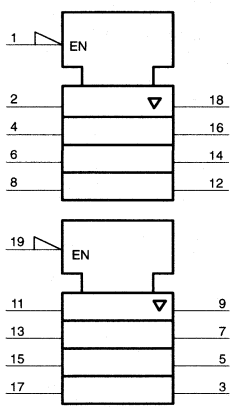
PIN NUMBER	SYMBOL	FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	Data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	Bus outputs
10	GND	Ground (0V)
17, 15, 13, 11	$2A_0$ to $2A_3$	Bus inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	Bus outputs
19	$\overline{2OE}$	Output enable input (active-LOW)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION



SV00212

LOGIC SYMBOL (IEEE/IEC)



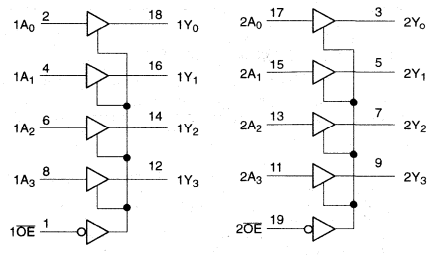
SV00209

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

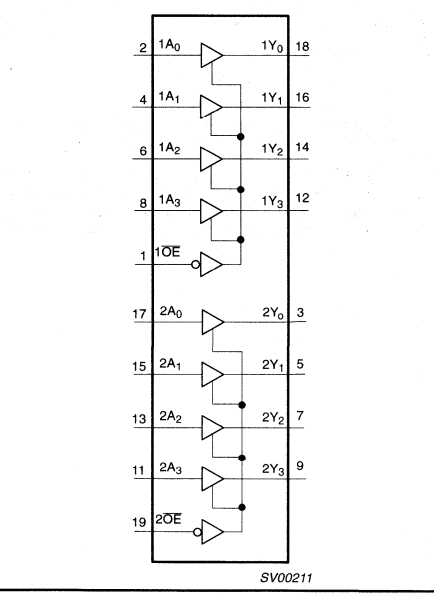
H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

LOGIC SYMBOL



SV00210

FUNCTIONAL DIAGRAM



SV00211

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC Output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA
I_{BHL}	Bushold LOW sustaining current[2, 3, 4]	V_{CC} = 3.0V; V_I =0.8V	75	–	–	µA
I_{BHH}	Bushold HIGH sustaining current[2, 3, 4]	V_{CC} = 3.0V; V_I =2.0V	–75	–	–	µA
I_{BHLO}	Bushold LOW overdrive current[2, 3, 5]	V_{CC} = 3.6V	500	–	–	µA
I_{BHHO}	Bushold HIGH overdrive current[2, 3, 5]	V_{CC} = 3.6V	–500	–	–	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bushold parts (LVCH-A) only.
3. For data inputs only, control inputs do not have a bushold circuit
4. The specified sustaining current at the data inputs do not have a bushold circuit.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bushold parts, the bushold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

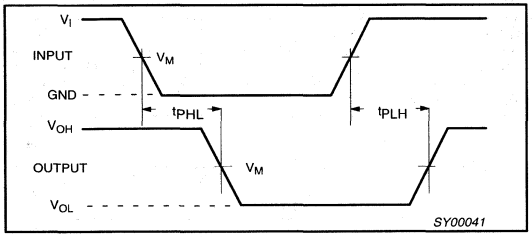
SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	1, 3	1.5	3.5	5.9	1.5	6.9	16.0	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{1OE}$ to $1Y_n$; $\overline{2OE}$ to $2Y_n$	2, 3	1.5	4.3	7.6	1.5	8.6	19.0	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{1OE}$ to $1Y_n$; $\overline{2OE}$ to $2Y_n$	2, 3	1.5	3.7	5.8	1.5	6.8	17.0	ns

NOTE:
1. Unless otherwise stated, all typical values are at $V_{CC} = 3.3$V and $T_{amb} = 25°C$.

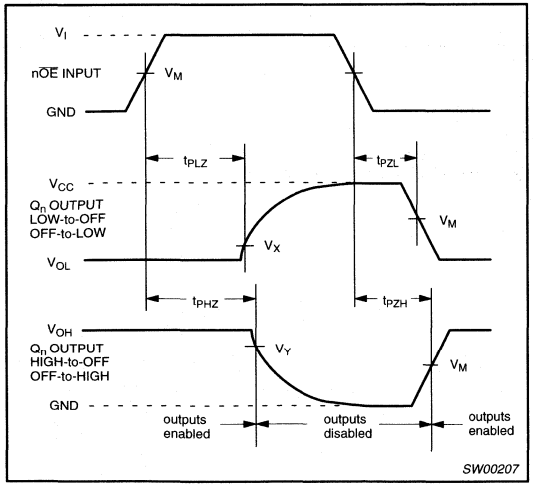
AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V; $V_M = 0.5\ V_{CC}$ at $V_{CC} < 2.7$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3$V at $V_{CC} \geq 2.7$V; $V_X = V_{OL} + 0.1\ V_{CC}$ at $V_{CC} < 2.7$V
$V_Y = V_{OH} - 0.3$V at $V_{CC} \geq 2.7$V; $V_Y = V_{OH} - 0.1\ V_{CC}$ at $V_{CC} < 2.7$V

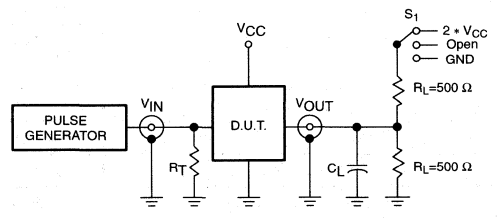


Waveform 1. Input (D_n) to output (Qn) propagation delays.



Waveform 2. 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 3. Load circuitry for switching times.

Octal bus transceiver with direction pin with 5-volt tolerant inputs/outputs (3-State)

74LVC245A
74LVCH245A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V
- Bushold on all data inputs (74LVCH245A only)

DESCRIPTION

The 74LVC245A/74LVCH245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC245A/74LVCH245A is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The '245' features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

The '245' is functionally identical to the '640', but the '640' has true (non-inverting) outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n; B_n to A_n	C_L = 50pF V_{CC} = 3.3V	3.6	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1 and 2	33	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}

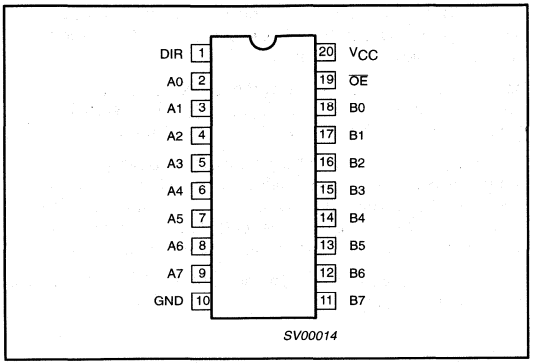
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	–40°C to +85°C	74LVC245A D	74LVC245A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVC245A DB	74LVC245A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVC245A PW	7LVC245APW DH	SOT360-1
20-Pin Plastic Shrink Small Outline (SO)	–40°C to +85°C	74LVCH245A D	74LVCH245A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVCH245A DB	74LVCH245A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVCH245A PW	LVCH245APW DH	SOT360-1

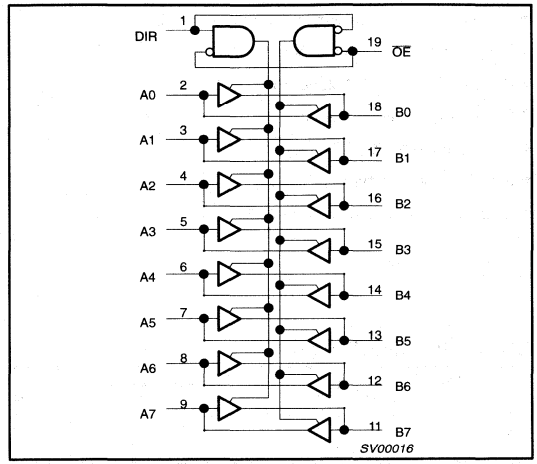
Octal bus transceiver with direction pin with 5-volt tolerant inputs/outputs (3-State)

74LVC245A 74LVCH245A

PIN CONFIGURATION



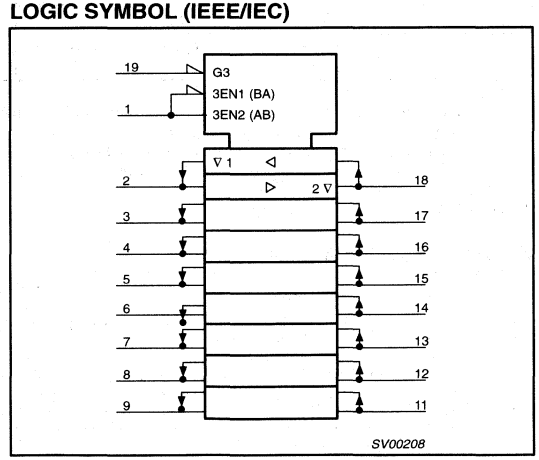
LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	DIR	Direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	Data inputs/outputs
10	GND	Ground (0V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	Data inputs/outputs
19	$\overline{OE}$	Output enable input (active-Low)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	B_0
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC Output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current[6]	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current[6, 7]	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA
I_{BHL}	Bushold LOW sustaining current[2, 3, 4]	V_{CC} = 3.0V; V_I =0.8V	75	–	–	µA
I_{BHH}	Bushold HIGH sustaining current[2, 3, 4]	V_{CC} = 3.0V; V_I =2.0V	–75	–	–	µA
I_{BHLO}	Bushold LOW overdrive current[2, 3, 5]	V_{CC} = 3.6V	500	–	–	µA
I_{BHHO}	Bushold HIGH overdrive current[2, 3, 5]	V_{CC} = 3.6V	–500	–	–	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bushold parts (LVCH-A) only.
3. For data inputs only, control inputs do not have a bushold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bushold parts, the bushold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.
7. For I/O ports the parameter I_{OZ} includes the input leakage current.

AC CHARACTERISTICS

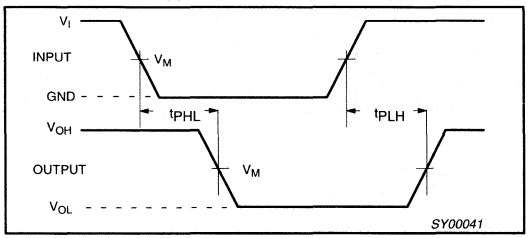
GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay A_n to B_n; B_n to A_n	1, 3	1.5	3.6	6.3	1.5	7.3	16	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n	2, 3	1.5	5.1	8.5	1.5	9.5	23	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n	2, 3	1.5	4.5	7.0	1.5	8.0	16	ns

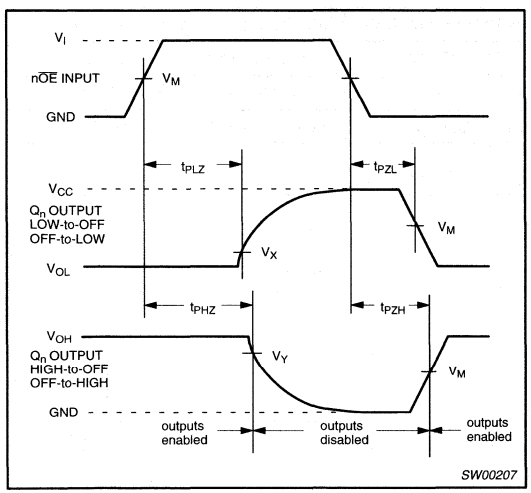
NOTE:
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ −0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ − 0.1 V_{CC} at V_{CC} < 2.7V

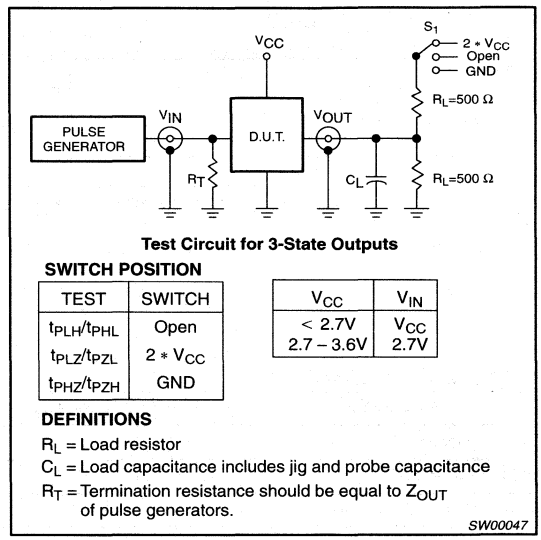


Waveform 1. Input (D_n) to output (Qn) propagation delays.



Waveform 2. 3-State enable and disable times.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 3. Load circuitry for switching times.

Quad 2-input multiplexer with 5 Volt tolerant inputs/outputs (3-State)

74LVC257A

FEATURES

- Wide supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- CMOS lower power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at 85°C
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC257A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC257A is a quad 2-input multiplexer with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S). The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S in HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs. The 74LVC257A is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S. The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nI_0, nI_1 to nY S to nY	C_L = 50 pF; V_{CC} = 3.3 V	 3.9 3.5	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per channel	V_I = GND to V_{CC}[1]	30	pF

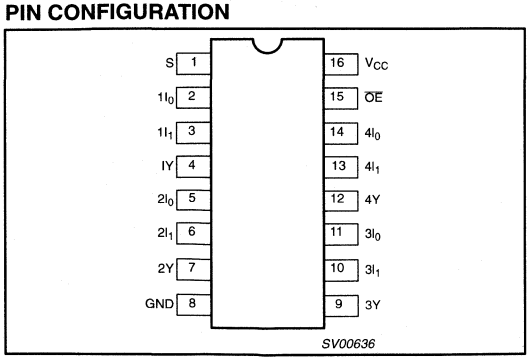
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

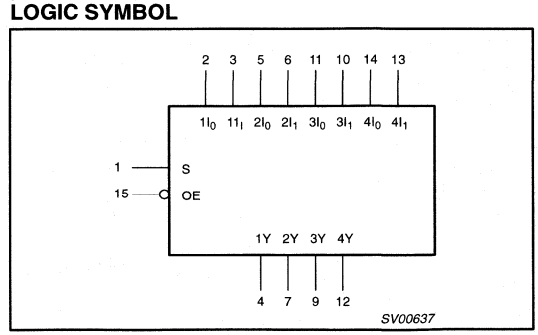
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic SO	–40°C to +85°C	74LVC257A D	74LVC257A D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC257A DB	74LVC257A DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC257A PW	74LVC257APW DH	SOT403-1

PIN CONFIGURATION



LOGIC SYMBOL



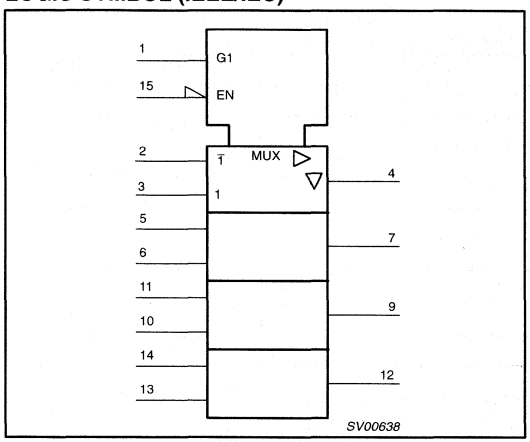
Quad 2-input multiplexer with 5 Volt tolerant inputs/outputs (3-State)

74LVC257A

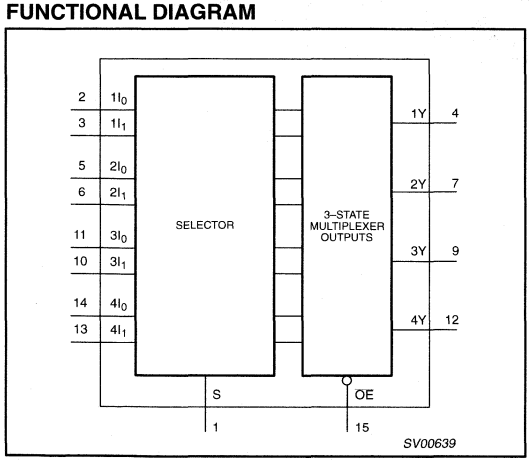
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	S	Common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	Data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	Data outputs from source 1
4, 7, 9, 12	1Y to 4Y	3-State multiplexer outputs
8	GND	Ground (0 V)
15	$\overline{OE}$	3-State output enable input (active LOW)
16	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM

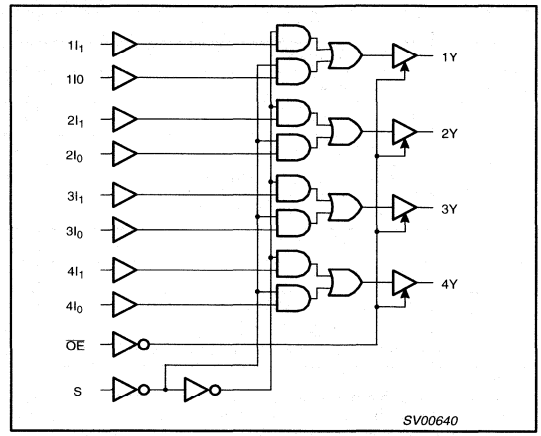


FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}$	S	nI_0	nI_1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC input voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134); Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −100μA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100μA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	μA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	±5	μA
I_{OFF}	Power off leakage current	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	μA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	μA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} −0.6V; I_O = 0		5	500	μA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = −40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay nI_0 to nY nI_1 to nY	Figures 1, 3	1.5	3.9	5.1	1.5	3.3	6.1	11	ns
t_{PHL}/t_{PLH}	Propagation delay S to nY	Figures 1, 3	1.5	3.5	6.4	1.5	4.3	7.5	14	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY	Figures 2, 3	1.5	3.7	6.5	1.5	4.6	7.5	15	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	Figures 2, 3	1.5	3.2	5.2	1.5	3.5	6.2	12	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$V
$V_Y = V_{OH} - 0.1 \times V_{CC}$ at $V_{CC} < 2.7$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

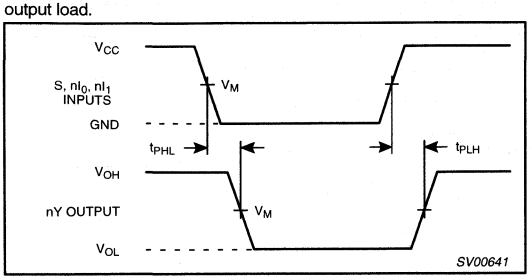


Figure 1. Input (S, nI_0, nI_1) to output (nY) propagation delays.

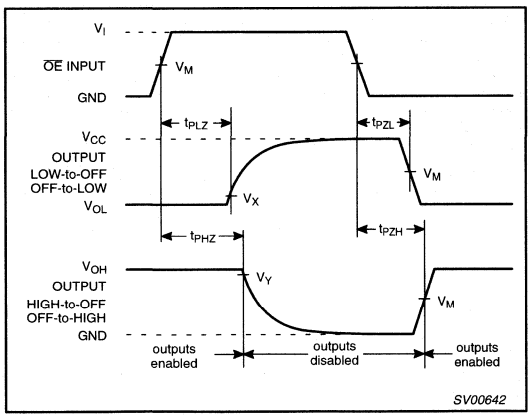
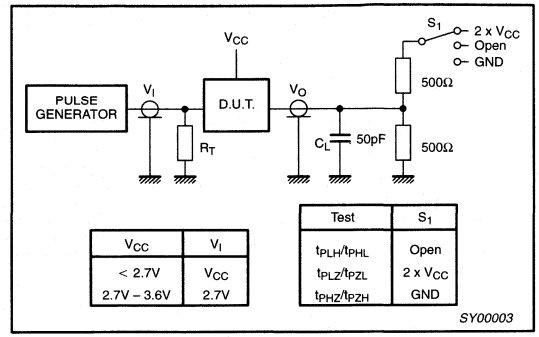


Figure 2. 3-state enable and disable times.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 3. Load circuitry for switching times.

Octal D-type flip-flop with reset; positive-edge trigger 74LVC273

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Conforms to JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC273 is a low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC273 has eight edge-triggered , D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn; $\overline{MR}$ to Q_n	C_L = 50pF V_{CC} = 3.3V	6.0 6.0	ns
f_{max}	Maximum clock frequency		230	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_I = GND to V_{CC}[1]	22	pF

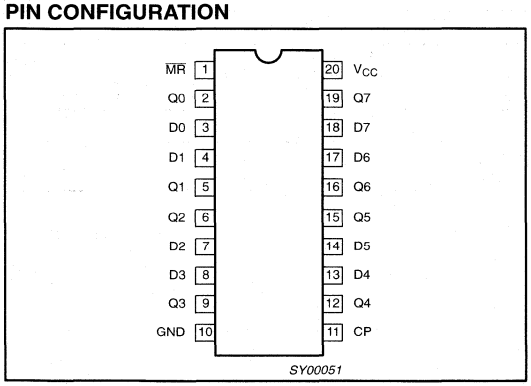
NOTE:

1 C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SO	−40°C to +85°C	74LVC273 D	74LVC273 D	SOT163-1
20-Pin Plastic SSOP Type II	−40°C to +85°C	74LVC273 DB	74LVC273 DB	SOT339-1
20-Pin Plastic TSSOP Type I	−40°C to +85°C	74LVC273 PW	74LVC273PW DH	SOT360-1

PIN CONFIGURATION

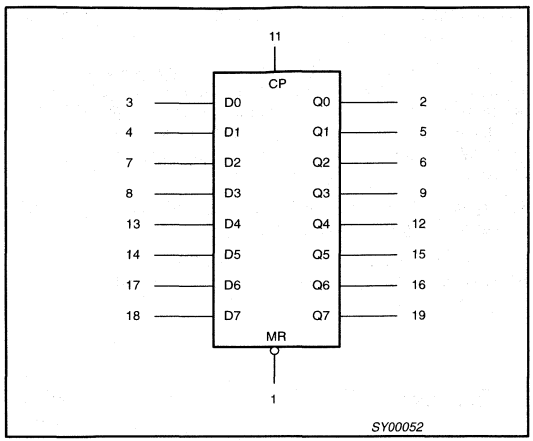


PIN DESCRIPTION

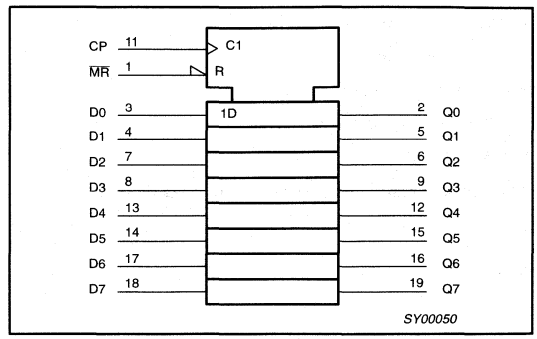
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{MR}$	Master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 – Q7	Flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 – D7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive power supply

Octal D-type flip-flop with reset; positive-edge trigger 74LVC273

LOGIC SYMBOL



IEEE/IEC LOGIC SYMBOL



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUT
	$\overline{MR}$	CP	Dn	Q0 – Q7
Reset (clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
↑ = LOW-to-HIGH transition
X = Don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
$V_{I/O}$	DC Input voltage range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	−0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

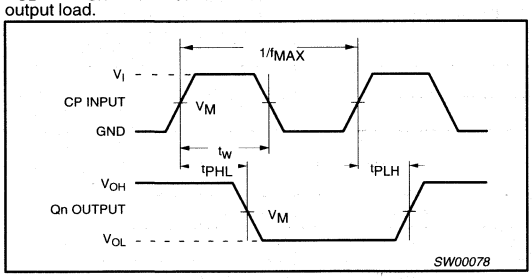
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
			MIN	TYP[1]	MAX	MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay CP to Qn	1		6.0	10.2		6.6	11.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	2		6.3	11.0		7.4	12.0	ns
t_W	Clock pulse width HIGH or LOW	1	4	1.2		5	1.8		ns
t_W	Master reset pulse width LOW	2	4	1.2		5	1.7		ns
t_{rem}	Removal time $\overline{MR}$ to CP	2	2	–1.0		3	–1.0		ns
t_{su}	Set-up time D_n to CP	3	2	0.7		3	1.0		ns
t_h	Hold time D_n to CP	3	0	–0.6		0	–0.9		ns
f_{max}	Maximum clock pulse frequency	1	125			100			MHz

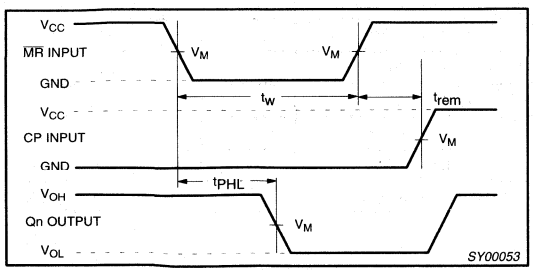
NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

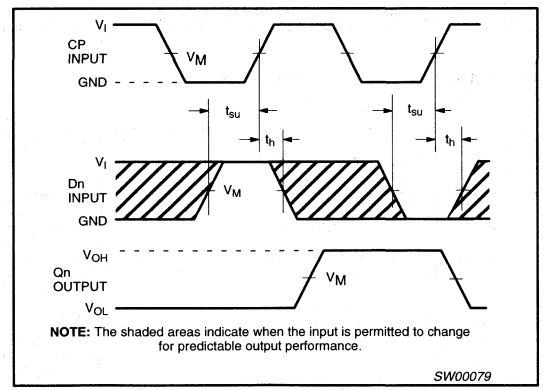
V_M = 1.5V at $V_{CC} \geq$ 2.7V.
V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. Clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency

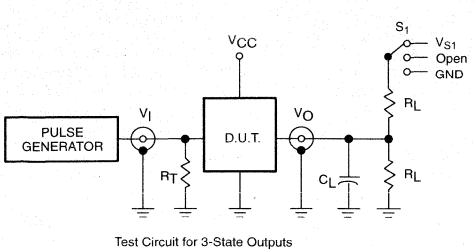


Waveform 2. Master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time

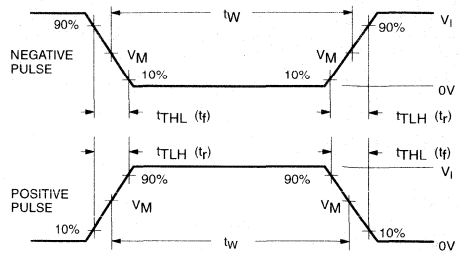


Waveform 3. Data set-up and hold times for the data input (D_n)

TEST CIRCUIT



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

Switch position

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{S1}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_{S1}
< 2.7V	V_{CC}	2 * V_{CC}
2.7–3.6V	2.7V	2 * V_{CC}

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SY00044

Waveform 4. Load circuitry for switching times

Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC373A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V

DESCRIPTION

The 74LVC373A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC373A is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus-oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '373' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition, the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW, the latches store the information that was present at the D-inputs one setup time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '373' is functionally identical to the '573', but the '573' has a different pin arrangement.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n; LE to Q_n	C_L = 50pF V_{CC} = 3.3V	 4.2 4.6	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1 and 2	20	pF

NOTE:

2. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
3. The condition is V_I = GND to V_{CC}

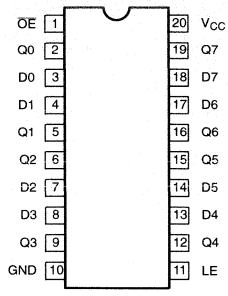
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	–40°C to +85°C	74LVC373A D	74LVC373A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVC373A DB	74LVC373A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVC373A PW	7LVC373APW DH	SOT360-1

Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

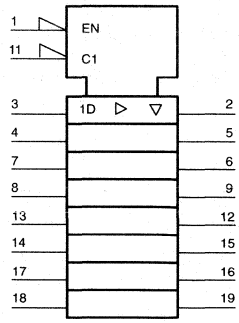
74LVC373A

PIN CONFIGURATION



SA00383

LOGIC SYMBOL (IEEE/IEC)

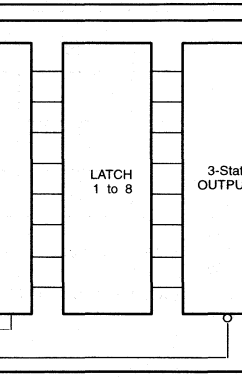


SA00385

PIN DESCRIPTION

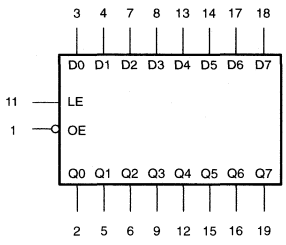
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	Data outputs
11	LE	Latch enable input (active-High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM



SA00387

LOGIC SYMBOL

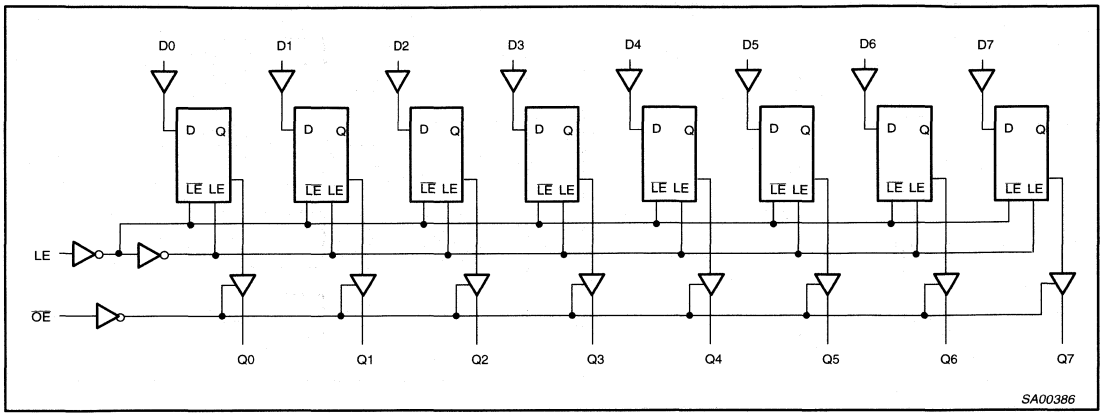


SA00384

Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC373A

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	H H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC Output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current[2]	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

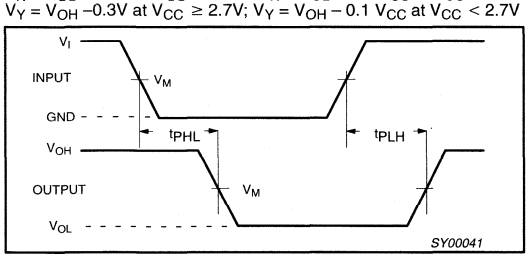
GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		$V_{CC} = 1.2V$	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay D_n to Q_n	1, 5	1.5	4.2	6.8	1.5	7.8	19	ns
t_{PHL} t_{PLH}	Propagation delay LE to Q_n	2, 5	1.5	4.6	7.2	1.5	8.2	21	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	3, 5	1.5	4.8	7.7	1.5	8.7	22	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	3, 5	1.5	4.3	6.1	1.5	7.1	15	ns
t_W	LE pulse width HIGH	2	3.0	1.5	–	3.0	–	–	ns
t_{SU}	Setup time D_n to LE	4	2.0	0	–	2.0	–	–	ns
t_h	Hold time D_n to LE	4	1.5	0.3	–	1.5	–	–	ns

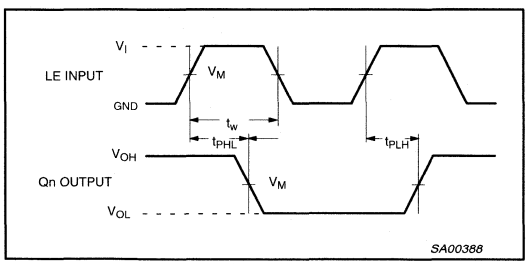
NOTE:
1. Unless otherwise stated, all typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25°C$.

AC WAVEFORMS

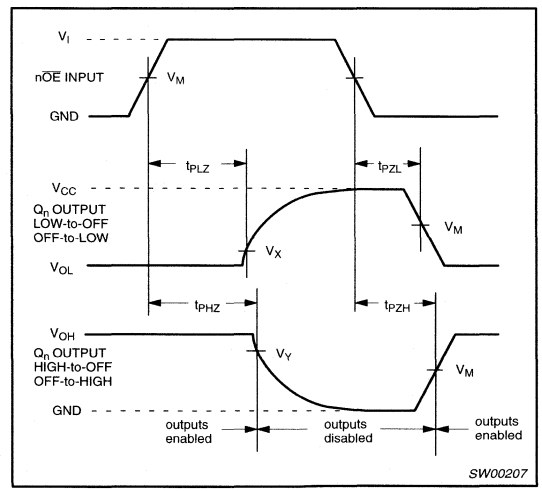
$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5\ V_{CC}$ at $V_{CC} < 2.7V$.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1\ V_{CC}$ at $V_{CC} < 2.7V$
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1\ V_{CC}$ at $V_{CC} < 2.7V$



Waveform 1. Input (D_n) to output (Qn) propagation delays.



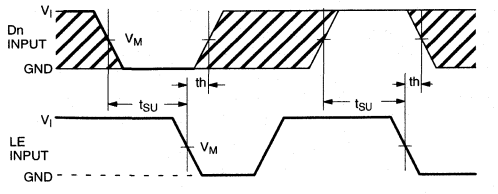
Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays



Waveform 3. 3-State enable and disable times.

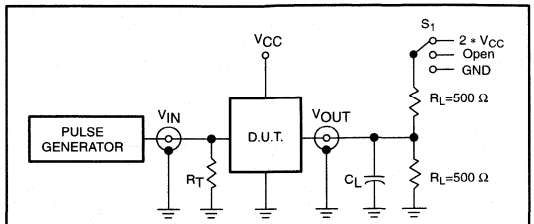
AC WAVEFORMS

with 5-volt tolerant inputs/outputs V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V



Waveform 4. Data setup and hold times for the D_n input to the LE input. (The shaded areas indicate when the input is permitted to change for predictable output performance).

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 5. Load circuitry for switching times.

Octal D-type flip-flop with 5-volt tolerant inputs/outputs; positive edge-trigger (3-State)

74LVC374A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V
- 8-bit positive edge-triggered register
- Independent register and 3-State buffer operation

DESCRIPTION

The 74LVC374A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC374A is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus-oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The '374' is functionally identical to the '574', but the '574' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} =25°C; $t_r = t_f \leq$ 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	C_L = 50pF V_{CC} = 3.3V	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	20	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}

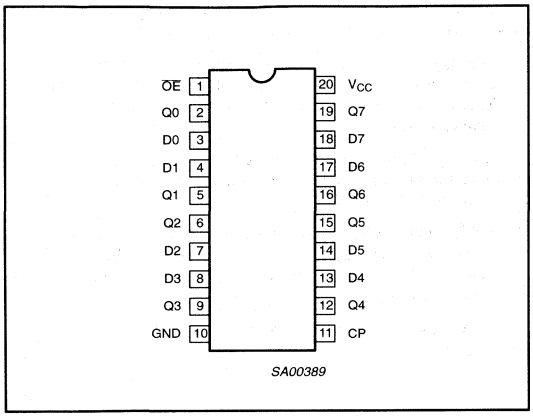
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	–40°C to +85°C	74LVC374A D	74LVC374A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVC374A DB	74LVC374A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVC374A PW	7LVC374APW DH	SOT360-1

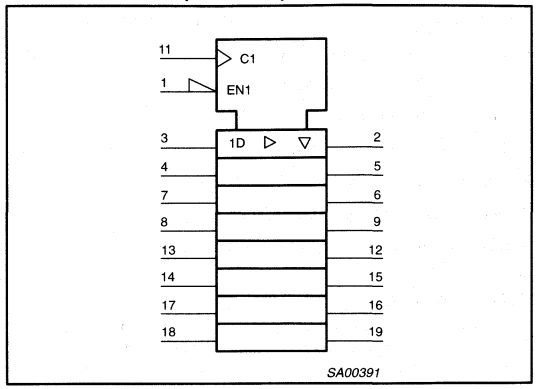
Octal D-type flip-flop with 5-volt tolerant inputs/outputs; positive edge-trigger (3-State)

74LVC374A

PIN CONFIGURATION



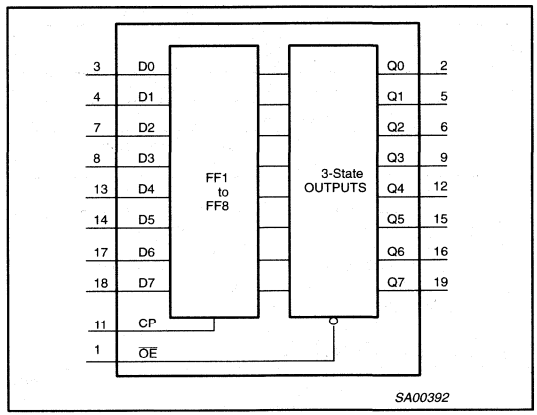
LOGIC SYMBOL (IEEE/IEC)



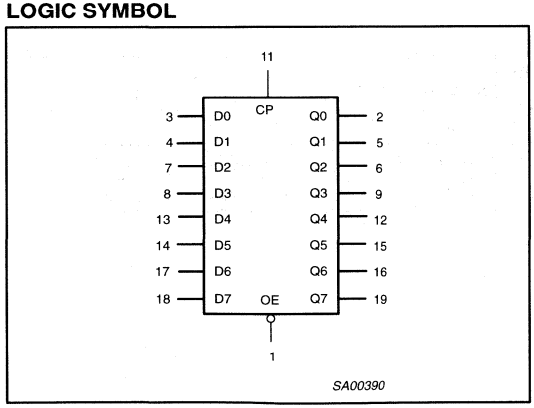
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
3, 4, 7, 8, 13, 14, 17, 18	D0-D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0-Q7	3-state flip-flop outputs
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTIONAL DIAGRAM

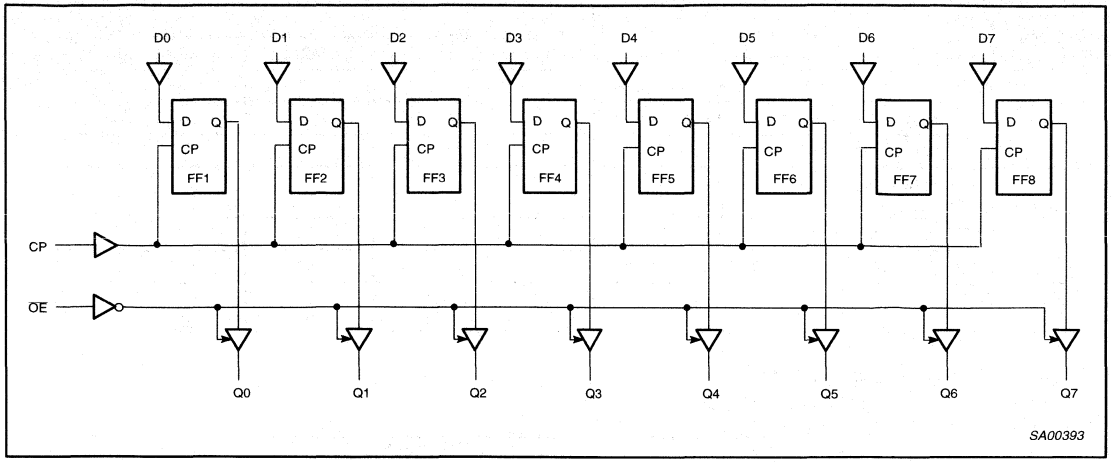


LOGIC SYMBOL



Octal D-type flip-flop with 5-volt tolerant inputs/outputs; positive edge-trigger (3-State) 74LVC374A

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH CP transition
Z = High impedance OFF-state
↑ = LOW-to-HIGH clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current[2]	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

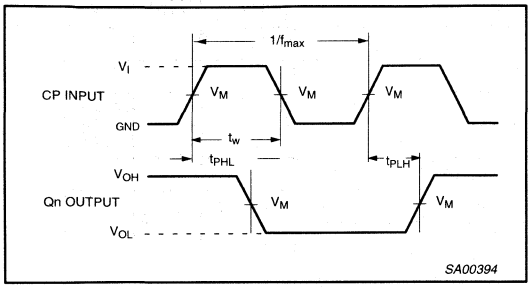
GND = 0V; $t_r = t_f \leq$ 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay CP to Q_n	1, 4	1.5	4.8	7.0	1.5	8.0	21	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	2, 4	1.5	4.8	7.5	1.5	8.5	22	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	2, 4	1.5	4.3	6.0	1.5	7.0	15	ns
t_W	Clock pulse width HIGH or LOW	1	3.0	1.5	–	3.0	–	–	ns
t_{SU}	Setup time D_n to CP	3	2.0	0	–	2.0	–	–	ns
t_h	Hold time D_n to CP	3	1.5	0.6	–	1.5	–	–	ns
f_{max}	maximum clock pulse frequency	1	100	–	–	80	–	–	MHz

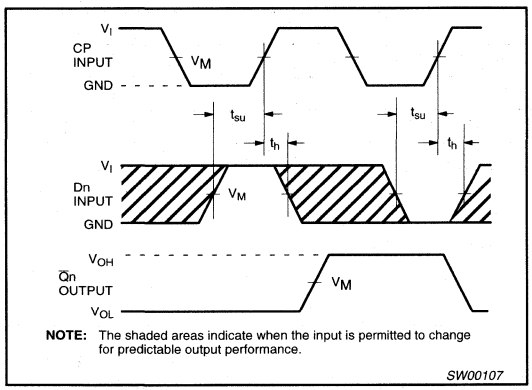
NOTE:
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

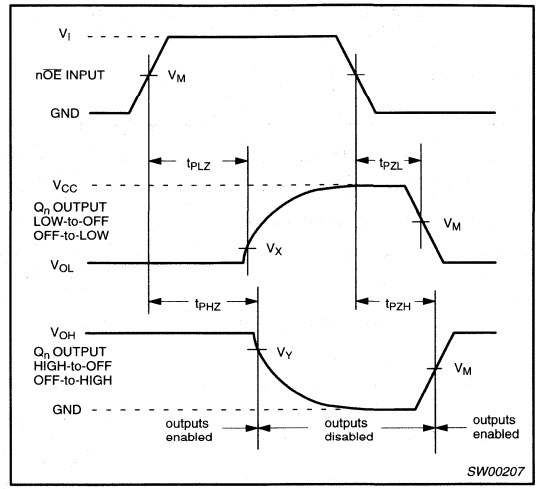
V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V



Waveform 1. Clock (CP) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

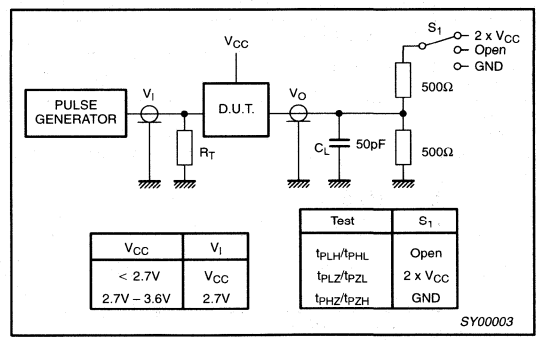


Waveform 2. Data setup and hold times for the D_n input to the CP input.



Waveform 3. 3-State enable and disable times.

TEST CIRCUIT



Waveform 4. Load circuitry for switching times.

Octal D-type flip-flop with data enable; positive-edge trigger

74LVC377

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Conforms to JEDEC standard 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC377 is a low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC377 has eight edge-triggered , D-type flip-flops with individual D inputs and Q outputs. A common clock (CP) input loads all flip-flops simultaneously when the data enable $\overline{E}$ is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. The $\overline{E}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn;	C_L = 50pF V_{CC} = 3.3V	6.0	ns
f_{max}	Maximum clock frequency		230	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_I = GND to V_{CC}[1]	22	pF

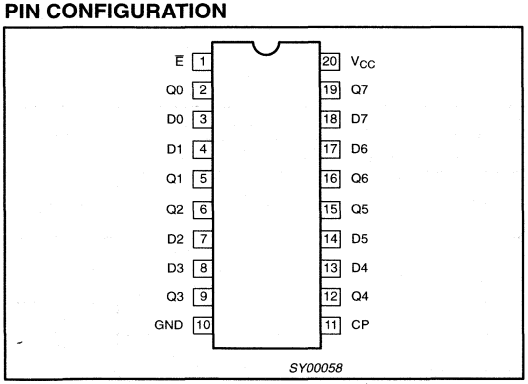
NOTES:

1 C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SO	–40°C to +85°C	74LVC377 D	74LVC377 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC377 DB	74LVC377 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC377 PW	74LVC377PW DH	SOT360-1

PIN CONFIGURATION



SY00058

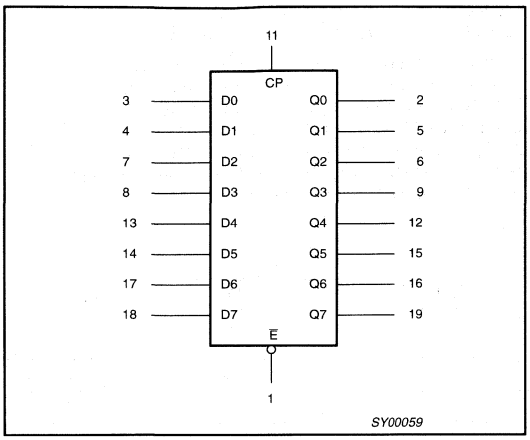
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{E}$	Data enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 – Q7	Flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 – D7	Data inputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive power supply

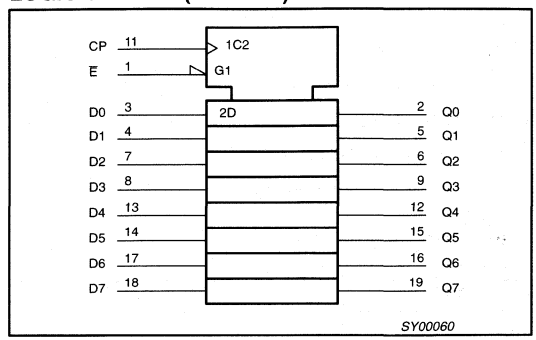
Octal D-type flip-flop with data enable; positive-edge trigger

74LVC377

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUT
	CP	$\overline{E}$	Dn	Q_n
Load '1'	↑	l	h	H
Load '0'	↑	l	l	L
hold (do nothing)	↑ X	h H	X X	no change no change

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH transition
X = Don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
$V_{I/O}$	DC Input voltage range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		−40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +5.5	V
$V_{I/O}$	DC input voltage range for I/Os		−0.5 to V_{CC} +0.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_{OUT}	DC output voltage	Note 2	−0.5 to V_{CC} +0.5	V
I_{OUT}	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−60 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND (Not for I/O pins)		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND		±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

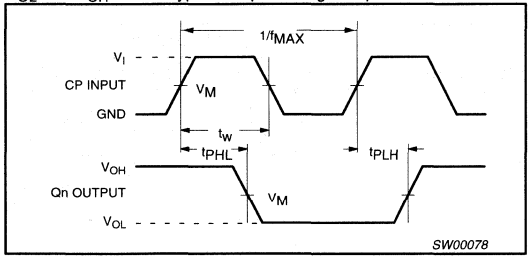
GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
			MIN	TYP[1]	MAX	MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay CP to Qn	1		6.0	10.2		6.6	11.2	ns
t_W	Clock pulse width HIGH or LOW	1	4	1.0		5	1.6		ns
t_{su}	Set-up time $\overline{E}$ to CP	2	4	2.3		5	2.9		ns
t_h	Hold time $\overline{E}$ to CP	2	0	−2.2		0	−2.8		ns
t_{su}	Set-up time D_n to CP	3	2	1.3		3	1.8		ns
t_h	Hold time D_n to CP	3	0	−1.2		0	−1.6		ns
f_{max}	Maximum clock pulse frequency	1	125			100			MHz

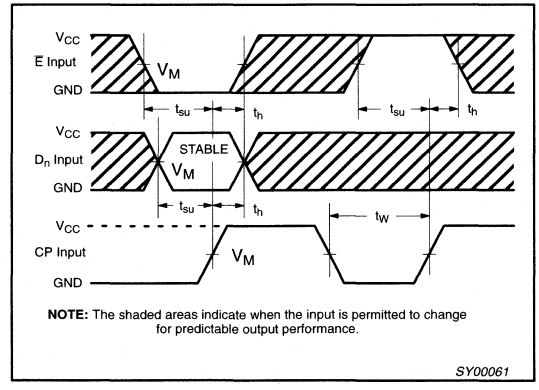
NOTE:
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V.
V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

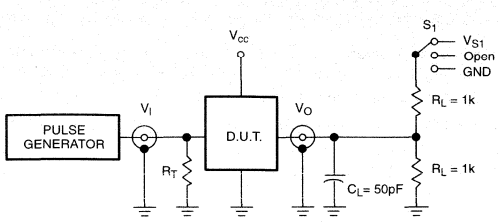


Waveform 1. Clock (CP) to output (Qn) propagation delays the clock pulse width and the maximum clock pulse frequency.

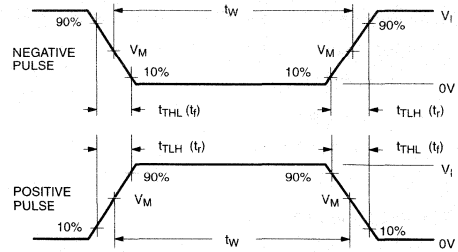


Waveform 2. Data set-up and hold times from the data input (Dn) and from the enable input ($\overline{E}$) to the clock (CP).

TEST CIRCUIT



Test Circuit for Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{S1}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I	V_{S1}
< 2.7V	V_{CC}	2 * V_{CC}
2.7–3.6V	2.7V	2 * V_{CC}
≥ 4.5 V	V_{CC}	2 * V_{CC}

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SY00044

Waveform 3. Load circuitry for switching times.

Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC541A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Wide supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC541A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC541A is an octal non-inverting buffer/line driver with 5-volt tolerant inputs/outputs. The 3-State outputs are controlled by the output enable inputs $\overline{OE}1$ and $\overline{OE}2$.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Yn	C_L = 50 pF; V_{CC} = 3.3 V	3.3	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1 and 2	20	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic SO	–40°C to +85°C	74LVC541A D	74LVC541A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC541A DB	74LVC541A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC541A PW	7LVC541APW DH	SOT360-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{OE}1$, $\overline{OE}2$	Output enable inputs (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	A0 to A7	Data inputs
10	GND	Ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	Y0 to Y7	Bus outputs
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

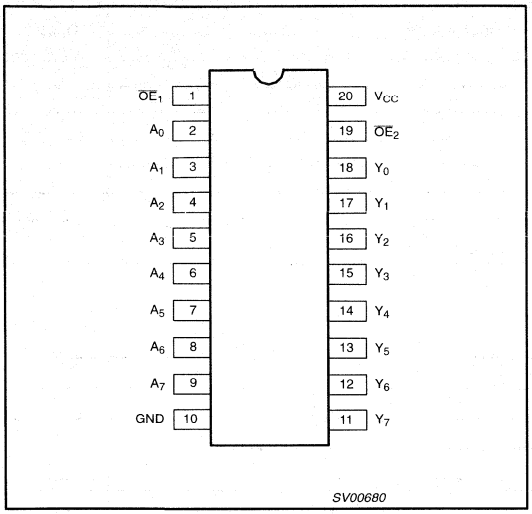
INPUTS	INPUTS		OUTPUT
$\overline{OE}1$	$\overline{OE}2$	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

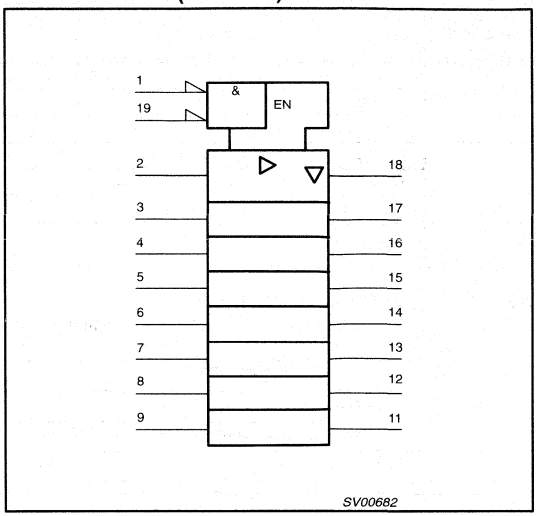
Octal buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC541A

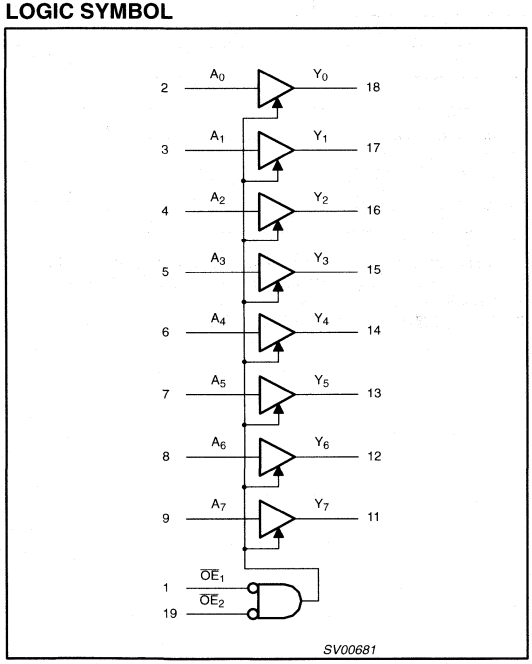
PIN CONFIGURATION



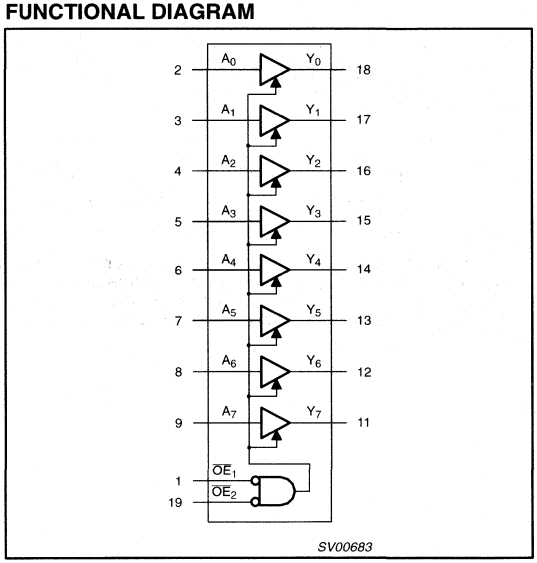
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to +6.5	
I_O	DC output diode current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–60 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{OFF}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V			±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	TYP	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay An to Yn	Figures 1, 3	1.5	3.3	5.6	1.5	3.9	6.6	14	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$n to Yn	Figures 2, 3	1.5	4.4	7.4	1.5	5.2	8.4	2.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$n to Yn	Figures 2, 3	1.5	3.8	6.0	1.5	4.3	7.0	11	ns

NOTE:
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 • V_{CC} at V_{CC} < 2.7 V
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 · V_{CC} at V_{CC} < 2.7 V
$V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ – 0.1 · V_{CC} at V_{CC} < 2.7 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

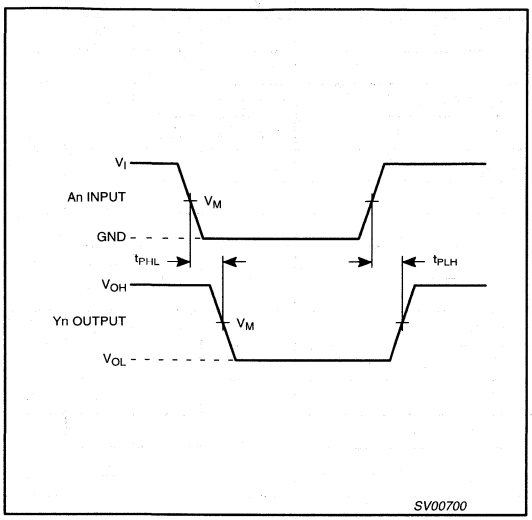


Figure 1. Input (A_n) to output (Y_n) propagation delays.

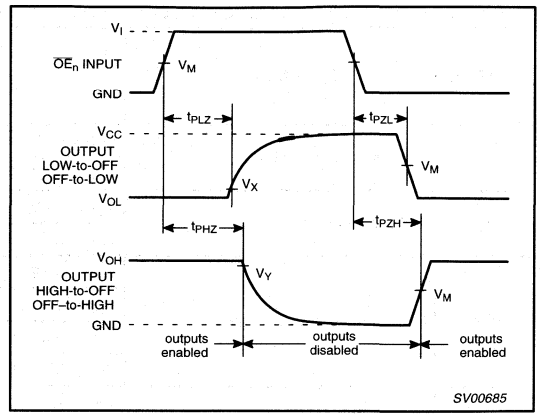
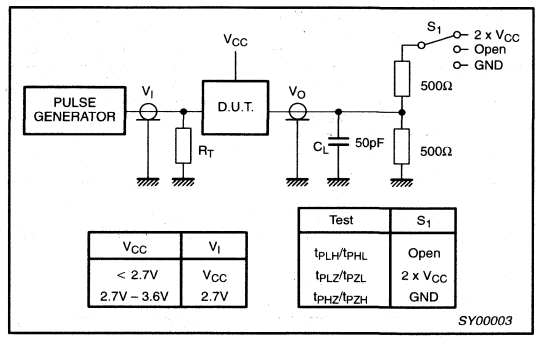


Figure 2. 3-state enable and disable times.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 3. Load circuitry for switching times.

Octal D-type registered transceiver (3-State) 74LVC543A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8–1A
- CMOS low power consumption
- Direct interface with TTL levels
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State non-inverting outputs for bus oriented applications
- High impedance when V_{CC} = 0V

DESCRIPTION

The 74LVC543A is a high–performance, low–power, low–voltage, Si–gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC543A is an octal registered transceiver containing two sets of D–type latches for temporary storage of the data flow in either direction. Separate latch enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and output enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The 74LVC543A contains eight D–type latches, with separate inputs and controls for each set. For data flow from A to B, for example, the A–to–B enable ($\overline{E}_{AB}$) input must be LOW in order to enter data from A_0–A_7 or take data from B_0–B_7, as indicated in the function table. With $\overline{E}_{AB}$ LOW, a LOW signal on the A–to–B latch enable ($\overline{LE}_{AB}$) input makes the A–to–B latches transparent; a subsequent LOW–to HIGH transition of the $\overline{LE}_{AB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both low, the 3–state B output buffers are active and display the data present at the outputs of the A latches

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $T_r = T_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n	C_L = 50 pF V_{CC} = 3.3V	3.3	ns
C_I	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10.0	pF
C_{PD}	power dissipation capacitance per latch	V_{CC} = 3.3V	27	pF

NOTES:

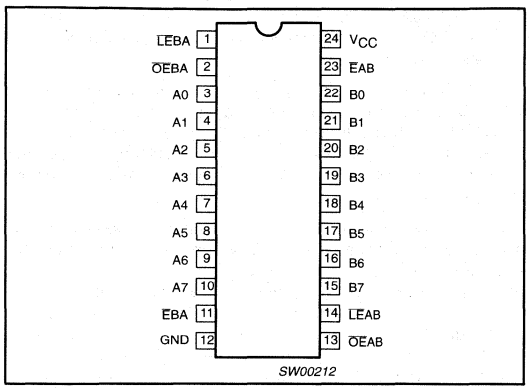
2. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs
3. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG DWG. #
24-Pin Plastic Small Outline (SO)	–40°C to +85°C	74LVC543A D	74LVC543A D	SOT137-1
24-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVC543A DB	74LVC543A DB	SOT340-1
24-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVC543A PW	7LVC543APW DH	SOT355-1

Octal D-type registered transceiver (3-State) 74LVC543A

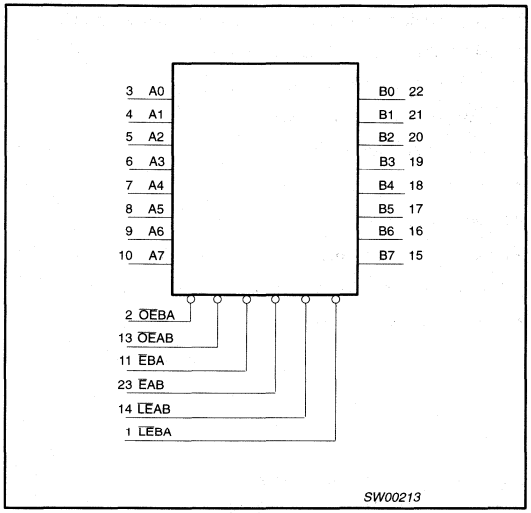
PIN CONFIGURATION



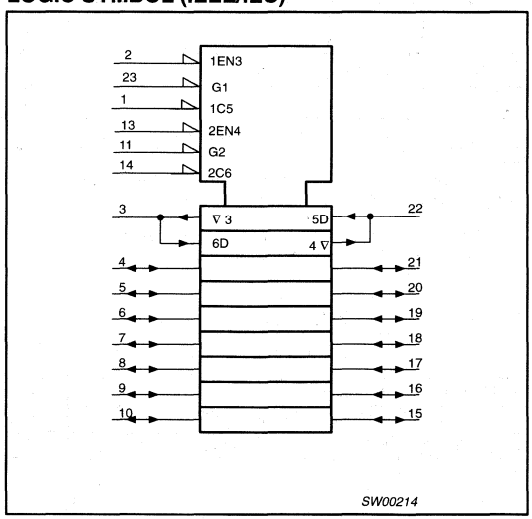
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{LE}_{BA}$	'B' to 'A' latch enable input (active LOW)
2	$\overline{OE}_{BA}$	'B' to 'A' output enable input (active LOW)
3,4,5,6, 7, 8, 9 10	A_0 to A_7	'A' data inputs/outputs
11	$\overline{E}_{BA}$	'B' to 'A' enable input (active LOW)
12	GND	ground (0V)
22, 21, 20, 19, 18, 17, 16, 15	B_0 to B_7	'B' data inputs/outputs
13	$\overline{OE}_{AB}$	'A' to 'B' output enable input (active LOW)
14	$\overline{LE}_{AB}$	'A' to 'B' latch enable input (active LOW)
23	$\overline{E}_{AB}$	'A' to 'B' enable input (active LOW)
24	V_{CC}	positive supply voltage

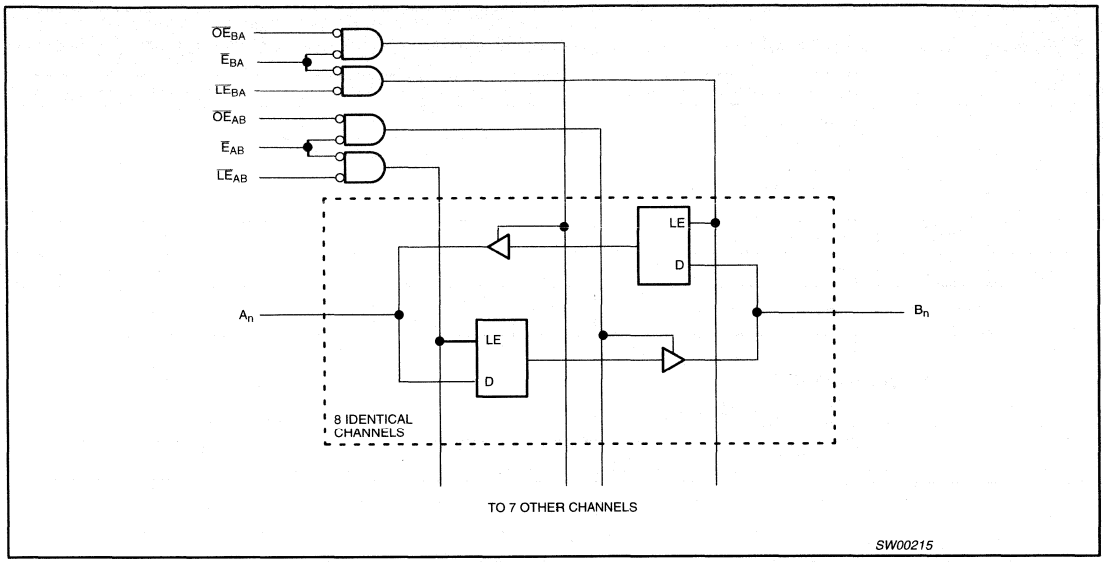
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS
	$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	DATA	
Disabled	H	X	X	X	Z
Disabled	X	H	X	X	Z
Disabled + Latch	L L	↑ ↑	L L	h l	Z Z
Latch + Display	L L	L L	↑ ↑	h l	H L
Transparent	L L	L L	L L	H L	H L
Hold (do nothing)	L	L	H	X	NC

NOTES:

XX = AB for A-to-B direction, BA for B-to-A direction
H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$, $\overline{E}_{BA}$
l = Low state must be present one setup time before the Low-to-High transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$, $\overline{E}_{BA}$
X = Don't care
↑ = Low-to-High level transition
NC = No change
Z = High impedance OFF state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
$V_{I/O}$	DC Output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC input voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	–0.5 to 6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

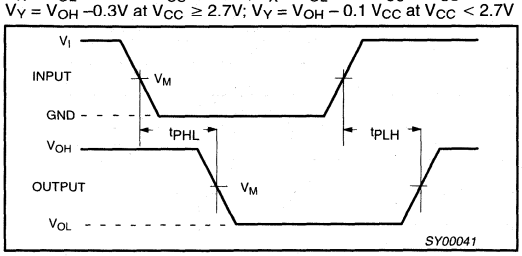
GND = 0V; $t_r = t_f$ =2.5ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay A_n to B_n, B_n to A_n	1, 5	1.5	3.3	7	1.5	8	13.0	ns
t_{PHL} t_{PLH}	Propagation delay $\overline{LE}_{BA}$ to A_n, $\overline{LE}_{AB}$ to B_n,	2, 5	1.5	4.1	8.5	1.5	9.5	16.0	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to A_n, $\overline{OE}_{AB}$ to B_n,	3, 5	1.5	4.2	7.7	1.5	9.2	15.0	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}_{BA}$ to A_n, $\overline{OE}_{AB}$ to B_n,	3, 5	1.5	3.4	7.0	1.5	7.5	8.0	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{E}_{BA}$ to A_n, $\overline{E}_{AB}$ to B_n,	3, 5	1.5	4.4	8.0	1.5	9.3	15.0	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{E}_{BA}$ to A_n, $\overline{E}_{AB}$ to B_n,	3, 5	1.5	3.6	7.0	1.5	7.5	8.0	ns
t_W	$\overline{LE}_{XX}$ pulse width LOW	2	3.0	0.9	–	3.0	–	4.0	ns
t_{su}	Set-up time A_n/B_n to $\overline{LE}_{XX}$, A_n/B_n to $\overline{E}_{XX}$	4	1.5	–0.5	–	1.5	–	–1.5	ns
t_h	Hold time A_n/B_n to $\overline{LE}_{XX}$, A_n/B_n to $\overline{E}_{XX}$	4	1.5	0.6	–	1.5	–	2.0	ns

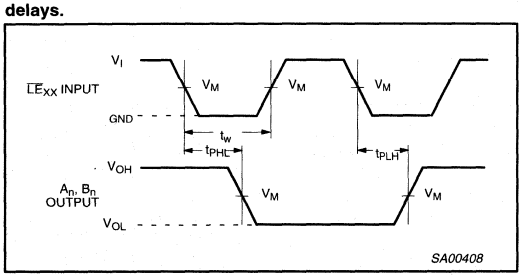
NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

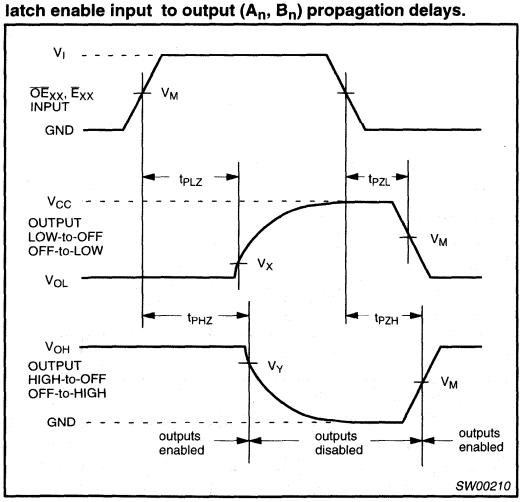
V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V



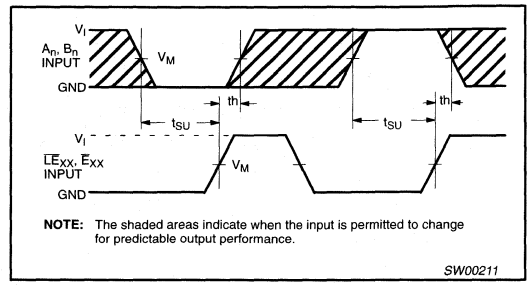
Waveform 1. Input (A_n, B_n) to output (B_n, A_n) propagation delays.



Waveform 2. Latch enable input ($\overline{LE}_{XX}$) pulse width and the latch enable input to output (A_n, B_n) propagation delays.

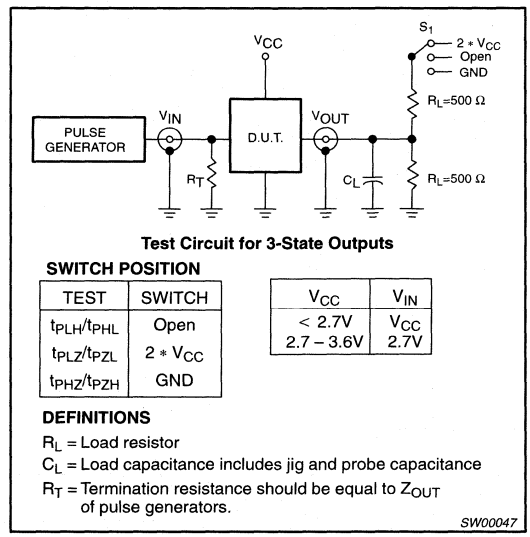


Waveform 3. 3-State enable and disable times



Waveform 4. Data setup and hold times for the (A_n, B_n) input to the $\overline{LE}_{XX}$ and $\overline{E}_{XX}$ inputs.

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 5. Load circuitry for switching times.

Octal D-type registered transceiver, inverting (3-State) 74LVC544A

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- Combines 74LVC640 and 74LVC533 type functions in one chip
- Octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State inverting outputs for bus oriented applications
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC544A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC544A is an octal registered inverting transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable ($\overline{LE}$AB, $\overline{LE}$BA) and output enable ($\overline{OE}$AB, $\overline{OE}$BA) inputs are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The '544A' contains eight D-type latches with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($\overline{E}$AB) input must be LOW in order to enter data from $\overline{A0}$–$\overline{A7}$ or take data from $\overline{B0}$–$\overline{B7}$, as indicated in the function table.

With $\overline{E}$AB LOW, a LOW signal on the A-to-B latch enable ($\overline{LE}$AB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LE}$AB signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{E}$AB and $\overline{OE}$AB both LOW, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $\overline{An}$ to $\overline{Bn}$	C_L = 50pF V_{CC} = 3.3V	4	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74LVC544A D	74LVC544A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC544A DB	74LVC544A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC544A PW	7LVC544APW DH	SOT355-1

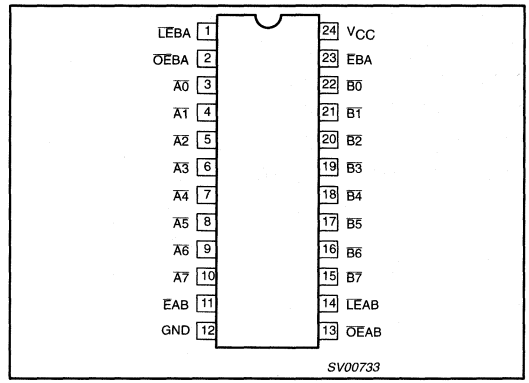
Octal D-type registered transceiver, inverting (3-State)

74LVC544A

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{LE}BA$	'B' to 'A' latch enable input (active LOW)
2	$\overline{OE}BA$	'B' to 'A' output enable input (active LOW)
3, 4, 5, 6, 7, 8, 9, 10	$\overline{A0}$–$\overline{A7}$	'A' data inputs/outputs
11	$\overline{E}BA$	'B' to 'A' enable input (active LOW)
12	GND	Ground (0V)
22, 21, 20, 19, 18, 17, 16, 15	$\overline{B0}$–$\overline{B7}$	'B' data inputs/outputs
13	$\overline{OE}AB$	'A' to 'B' output enable input (active LOW)
14	$\overline{LE}AB$	'A' to 'B' latch enable input (active LOW)
23	$\overline{E}AB$	'A' to 'B' enable input (active LOW)
24	VCC	Positive supply voltage

PIN CONFIGURATION

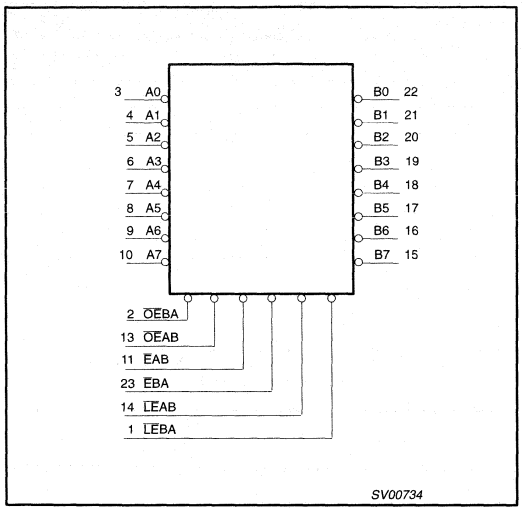


FUNCTION TABLE

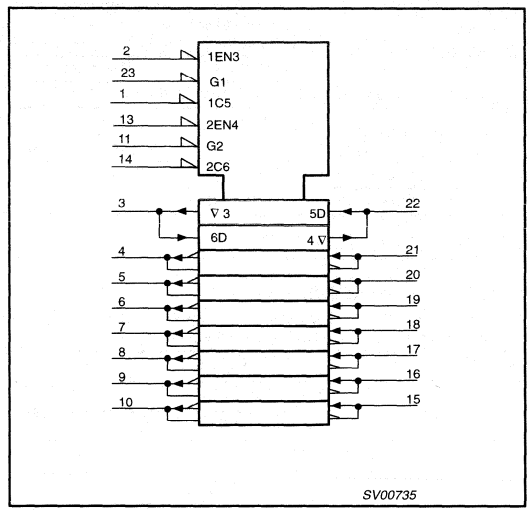
INPUTS				OUTPUTS	STATUS
$\overline{OE}XX$	$\overline{E}XX$	$\overline{LE}XX$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	L H	Latch + Display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}AB$, $\overline{LE}BA$, $\overline{E}AB$, $\overline{E}BA$
l = LOW state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}AB$, $\overline{LE}BA$, $\overline{E}AB$, $\overline{E}BA$
X = Don't care
↑ = LOW–to–HIGH level transition
NC = No change
Z = High impedance OFF-state

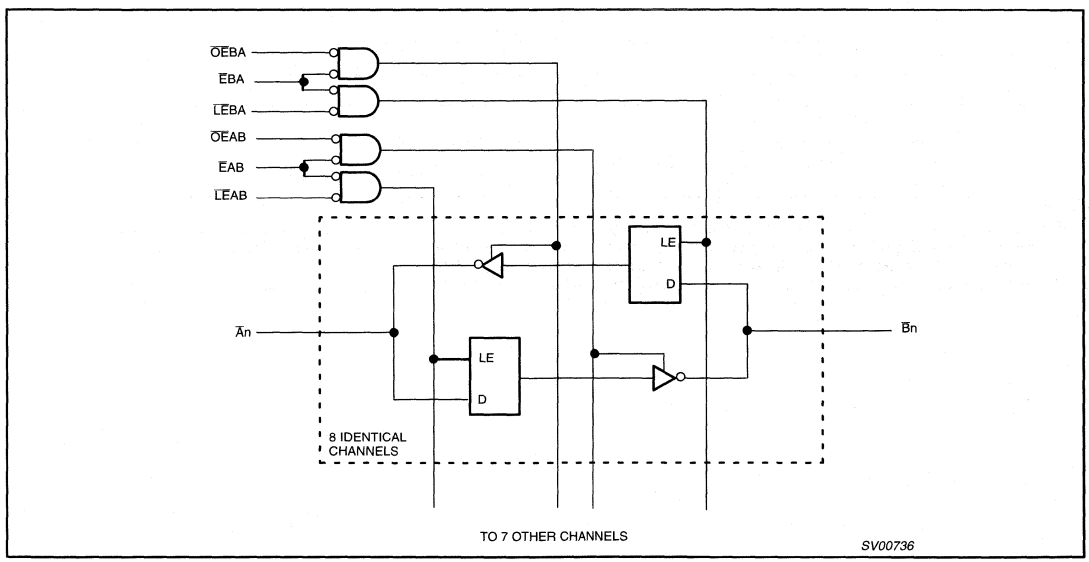
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{OFF}	Power off leakage current	V_{CC} = 0.0V; V_I = 5.5V; V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} −0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay $\overline{An}$ to $\overline{Bn}$, $\overline{Bn}$ to $\overline{An}$	Figures 1, 5	1.5	4	6.5	1.5	7.5	ns
t_{PHL}/t_{PLH}	Propagation delay $\overline{LE}BA$ to $\overline{An}$, $\overline{LE}AB$ to $\overline{Bn}$	Figures 2, 5	1.5	4.3	7.5	1.5	8.5	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}BA$ to $\overline{An}$, $\overline{OE}AB$ to $\overline{Bn}$	Figures 3, 5	1.5	4.5	8.5	1.5	9.5	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}BA$ to $\overline{An}$, $\overline{OE}AB$ to $\overline{Bn}$	Figures 3, 5	1.5	3.9	6.5	1.5	7.5	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{E}BA$ to $\overline{An}$, $\overline{E}AB$ to $\overline{Bn}$	Figures 3, 5	1.5	4.7	8.9	1.5	9.9	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{E}BA$ to $\overline{An}$, $\overline{E}AB$ to $\overline{Bn}$	Figures 3, 5	1.5	3.9	6.9	1.5	7.9	ns
t_W	$\overline{LE}XX$ pulse width HIGH	Figure 2	2.0	–	–	2.0	–	ns
t_{su}	Set-up time $\overline{An}/\overline{Bn}$ to $\overline{LE}XX$, $\overline{An}/\overline{Bn}$ to $\overline{E}XX$	Figure 4	2.0	–	–	2.0	–	ns
t_h	Hold time $\overline{An}/\overline{Bn}$ to $\overline{LE}XX$, $\overline{An}/\overline{Bn}$ to $\overline{E}XX$	Figure 4	4.0	–	–	1.0	–	ns

NOTE:

1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V
$V_X = V_{OL}$ + 0.1V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH}$ – 0.1V_{CC} at V_{CC} < 2.7V

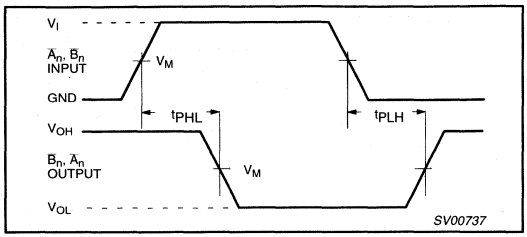


Figure 1. Input ($\overline{A}$n, $\overline{B}$n) to output ($\overline{B}$n, $\overline{A}$n) propagation delays.

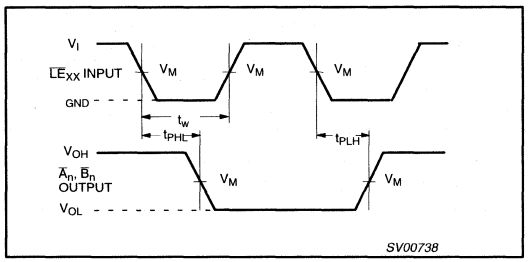


Figure 2. Latch enable input ($\overline{LE}$XX) pulse width, the latch enable input to output ($\overline{A}$n, $\overline{B}$n) propagation delays.

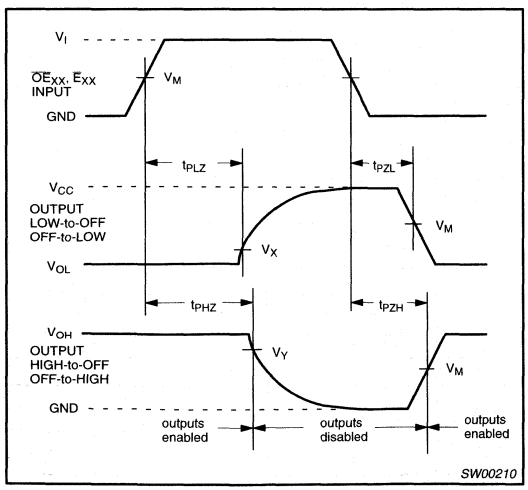


Figure 3. 3-State enable and disable times

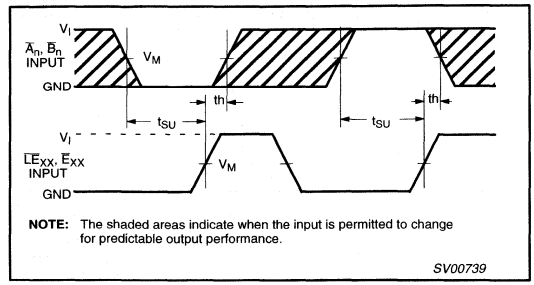
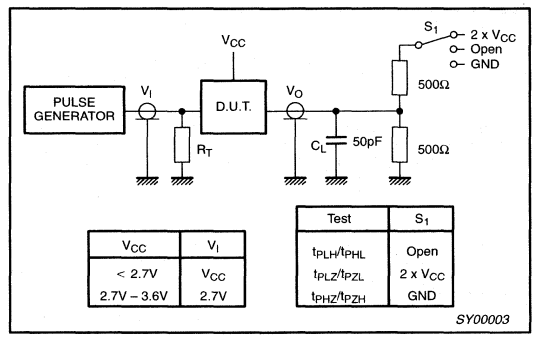


Figure 4. Data set-up and hold times for the ($\overline{A}$n, $\overline{B}$n) input to the $\overline{LE}$XX and $\overline{E}$XX inputs

TEST CIRCUIT



VCC	VI
< 2.7V	VCC
2.7V – 3.6V	2.7V

Test	S1
tPLH/tPHL	Open
tPLZ/tPZL	2 x VCC
tPHZ/tPZH	GND

Figure 5. Load circuitry for switching times

Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC573A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V
- Flow-through pin-out architecture

DESCRIPTION

The 74LVC573A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC573A is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus-oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '573A' consists of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition, the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When LE is LOW, the latches store the information that was present at the D-inputs one setup time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '573A' is functionally identical to the '373A', but the '373A' has a different pin arrangement.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n; LE to Q_n	C_L = 50pF V_{CC} = 3.3V	 4.3 4.6	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 2 and 3	20	pF

NOTE:

2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
3. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	–40°C to +85°C	74LVC573A D	74LVC573A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVC573A DB	74LVC573A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVC573A PW	7LVC573APW DH	SOT360-1

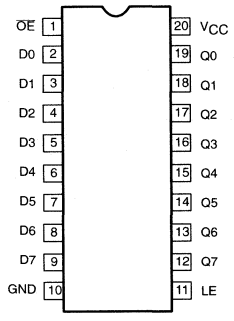
Octal D-type transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC573A

PIN DESCRIPTION

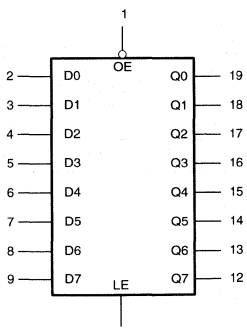
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
10	GND	Ground (0V)
11	LE	Latch enable input (active-High)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION



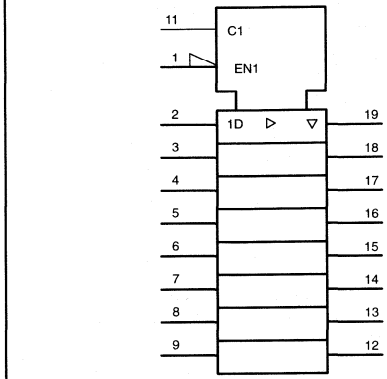
SA00395

LOGIC SYMBOL



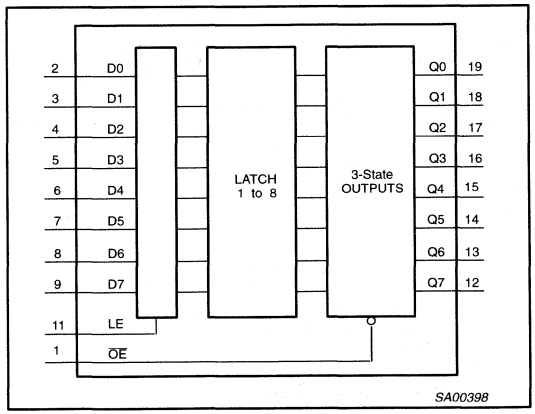
SA00396

LOGIC SYMBOL (IEEE/IEC)



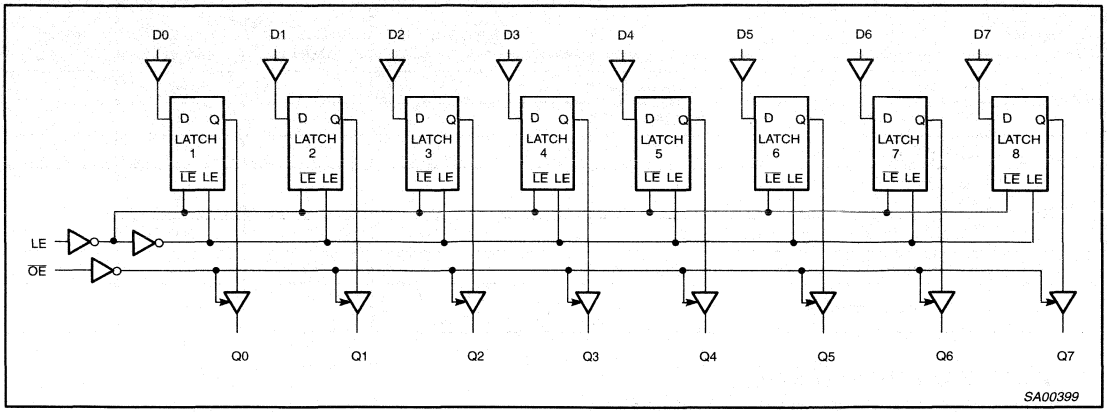
SA00397

FUNCTIONAL DIAGRAM



SA00398

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW LE transition
X = Don't care
Z = High impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current[2]	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

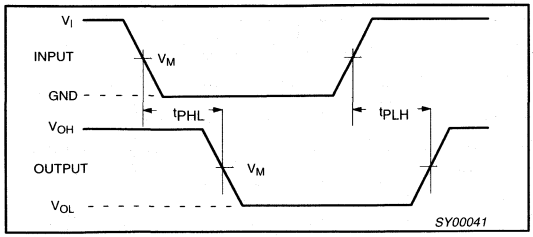
GND = 0V; $t_r = t_f \leq$ 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay D_n to Q_n	1, 5	1.5	4.3	6.2	1.5	7.2	19	ns
t_{PHL} t_{PLH}	Propagation delay LE to Q_n	2, 5	1.5	4.6	6.5	1.5	7.5	21	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	2, 5	1.5	3.8	7.5	1.5	8.5	17	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	3, 5	1.5	3.5	6.0	1.5	6.5	15	ns
t_W	LE pulse width HIGH	2	3.2	1.6	–	3.2	–	–	ns
t_{SU}	Setup time D_n to LE	4	1.7	0.3	–	1.7	–	–	ns
t_h	Hold time D_n to LE	4	1.4	0.2	–	1.5	–	–	ns

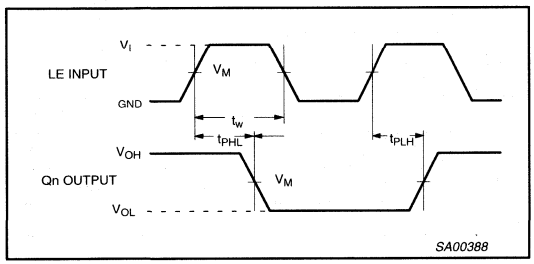
NOTE:
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

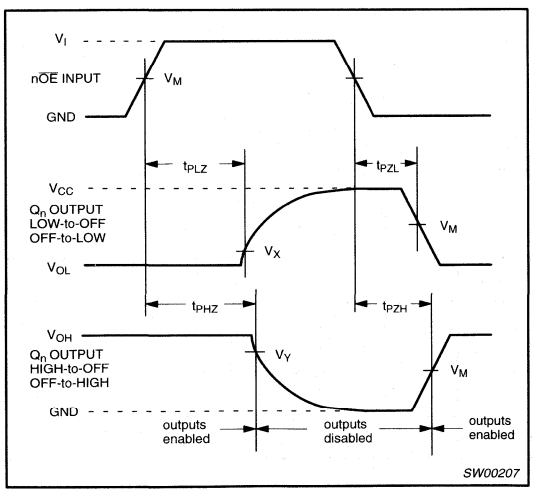
V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ −0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ − 0.1 V_{CC} at V_{CC} < 2.7V



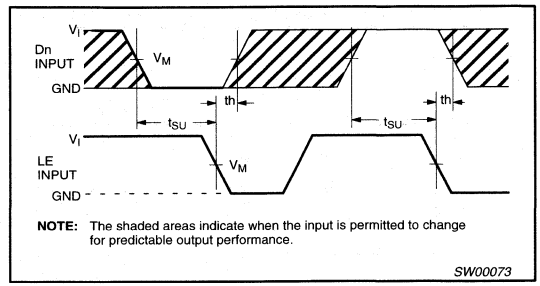
Waveform 1. Input (D_n) to output (Qn) propagation delays.



Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays

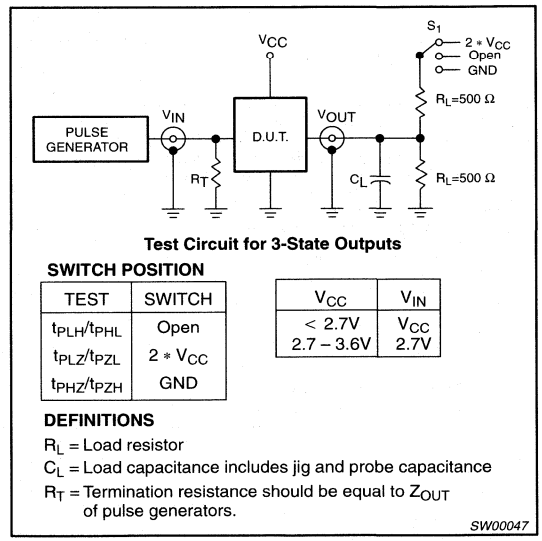


Waveform 3. 3-State enable and disable times.



Waveform 4. Data setup and hold times for the D_n input to the LE input.

TEST CIRCUIT



SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Waveform 5. Load circuitry for switching times.

Octal D-type flip-flop with 5-volt tolerant inputs/outputs; positive edge-trigger (3-State)

74LVC574A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V
- 8-bit positive edge-triggered register
- Independent register and 3-State buffer operation
- Flow-through pin-out architecture

DESCRIPTION

The 74LVC574A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC574A is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus-oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The '574A' is functionally identical to the '374A', but the '374A' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; T_{amb} =25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	C_L = 50pF V_{CC} = 3.3V	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 2 and 3	20	pF

NOTE:

2. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
3. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic Shrink Small Outline (SO)	–40°C to +85°C	74LVC574A D	74LVC574A D	SOT163-1
20-Pin Plastic Shrink Small Outline (SSOP) Type II	–40°C to +85°C	74LVC574A DB	74LVC574A DB	SOT339-1
20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I	–40°C to +85°C	74LVC574A PW	7LVC574APW DH	SOT360-1

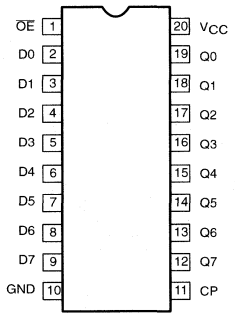
Octal D-type flip-flop with 5-volt tolerant inputs/outputs; positive edge-trigger (3-State)

74LVC574A

PIN DESCRIPTION

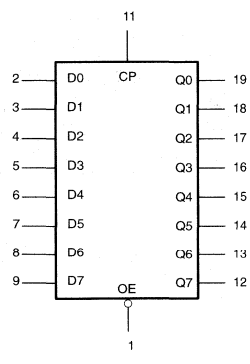
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
10	GND	Ground (0V)
11	CP	Clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION



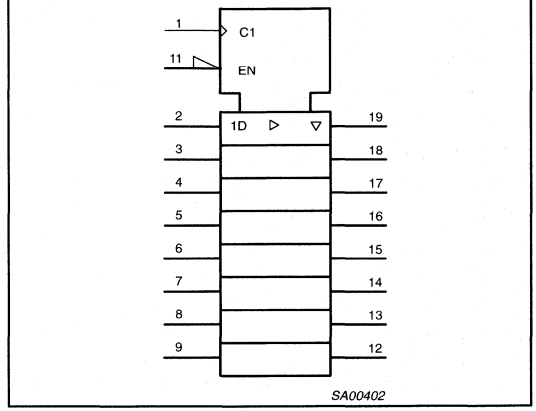
SA00400

LOGIC SYMBOL



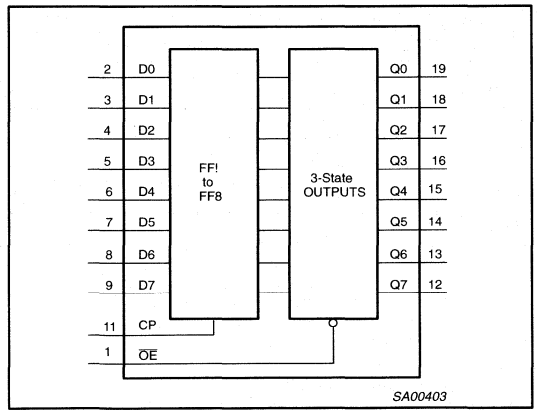
SA00401

LOGIC SYMBOL (IEEE/IEC)



SA00402

FUNCTIONAL DIAGRAM

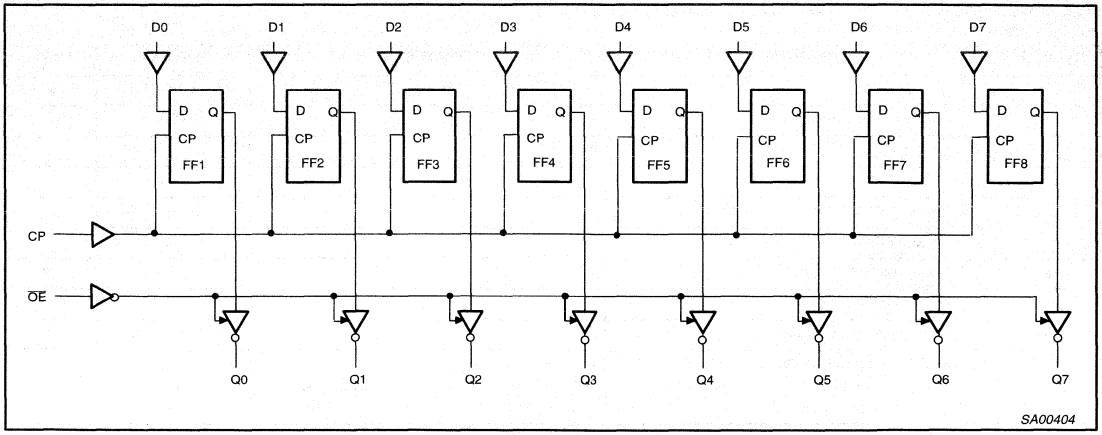


SA00403

Octal D-type flip-flop with 5-volt tolerant inputs/outputs; positive edge-trigger (3-State)

74LVC574A

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH CP transition
Z = High impedance OFF-state
↑ = LOW-to-HIGH clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		−40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	−0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	−0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current[2]	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

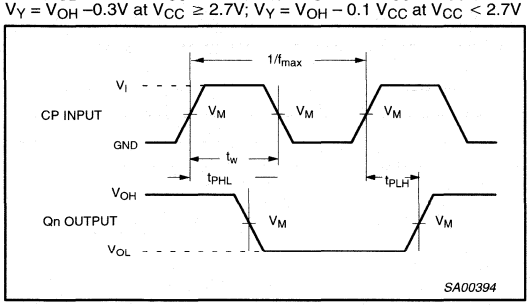
GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay CP to Q_n	1, 4	1.5	4.8	7.0	1.5	8.0	21	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	2, 4	1.5	4.0	7.5	1.5	8.5	17	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	2, 4	1.5	3.5	6.0	1.5	6.5	11	ns
t_W	Clock pulse width HIGH or LOW	1	3.4	1.7	–	3.4	–	–	ns
t_{SU}	Setup time D_n to CP	3	2.0	0.3	–	2.0	–	–	ns
t_h	Hold time D_n to CP	3	1.5	–0.2	–	1.5	–	–	ns
f_{max}	Maximum clock pulse frequency	1	100		–	80	–	–	MHz

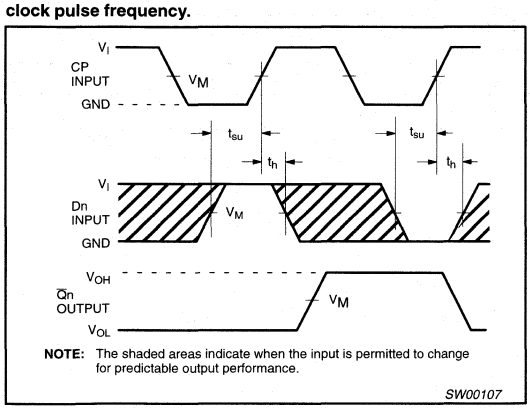
NOTE:
1. Unless otherwise stated, all typical values are at $V_{CC} = 3.3$V and $T_{amb} = 25°C$.

AC WAVEFORMS

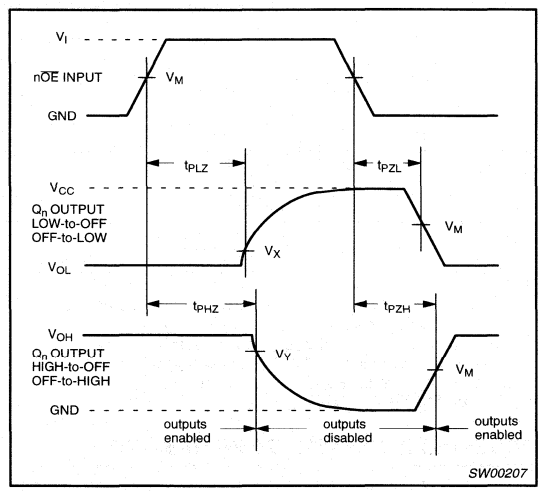
$V_M = 1.5$V at $V_{CC} \geq 2.7$V; $V_M = 0.5\ V_{CC}$ at $V_{CC} < 2.7$V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$V at $V_{CC} \geq 2.7$V; $V_X = V_{OL} + 0.1\ V_{CC}$ at $V_{CC} < 2.7$V
$V_Y = V_{OH} - 0.3$V at $V_{CC} \geq 2.7$V; $V_Y = V_{OH} - 0.1\ V_{CC}$ at $V_{CC} < 2.7$V



Waveform 1. Clock (CP) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

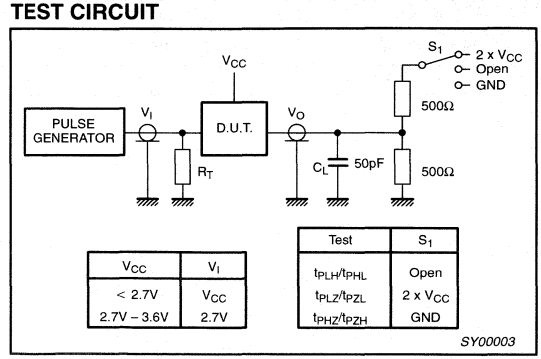


Waveform 2. Data setup and hold times for the D_n input to the CP input.



Waveform 3. 3-State enable and disable times.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Waveform 4. Load circuitry for switching times.

Octal transceiver with dual enable (3-State) 74LVC623A

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- Flow-through pin-out architecture
- CMOS low power consumption
- Inputs accept voltages up to 5.5V
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74LVC623A is a high performance, low-power, low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC623A is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. This octal bus transceiver is designed for asynchronous two-way communication between data buses.

The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the levels at the enable inputs (OEAB, $\overline{OE}$BA). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OEAB and $\overline{OE}$BA. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.

The '623A' is identical to the '620A' but has true (non-inverting) outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 50pF V_{CC} = 3.3V	3.3	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	32	pF

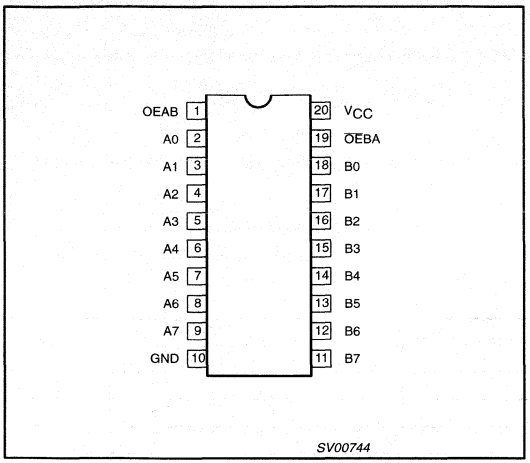
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic SO	–40°C to +85°C	74LVC623A D	74LVC623A D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC623A DB	74LVC623A DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC623A PW	7LVC623APW DH	SOT360-1

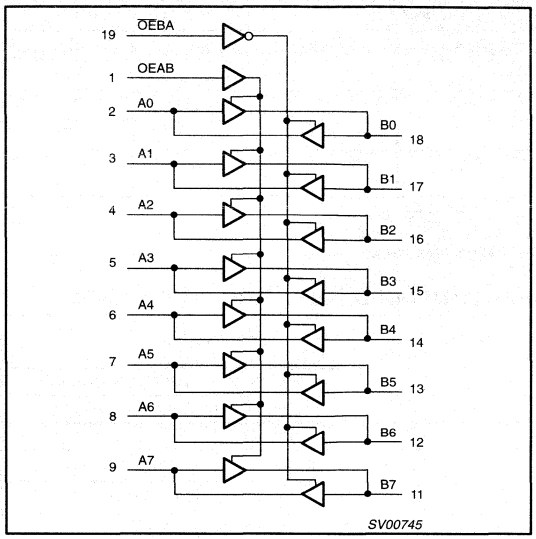
PIN CONFIGURATION



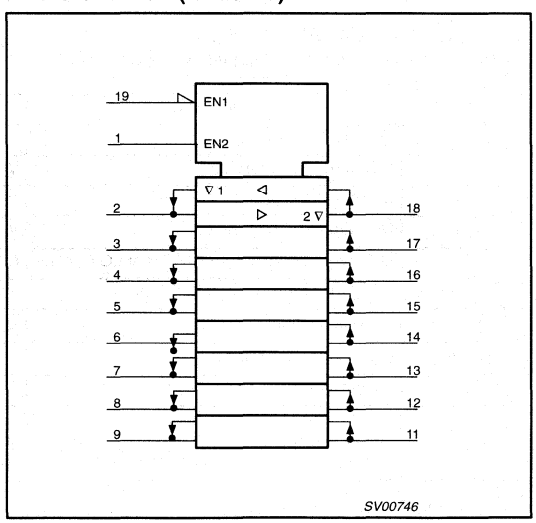
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Direction control
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs
10	GND	Ground (0V)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs
19	$\overline{OE}BA$	Output enable input (active LOW)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
OEAB	**$\overline{OEBA}$**	**An**	**Bn**
L	L	A=B	Inputs
H	H	Inputs	B=A
L	H	Z	Z
H	L	A=B Inputs	Inputs B=A

H = High voltage level
L = Low voltage level
Z = High impedance

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		−40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	−0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	−0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay An to Bn, Bn to An	Figures 1, 4	1.5	2.3	6	1.5	7	ns
t_{PZH}/t_{PZL}	3-State output enable time OEAB to Bn	Figures 3, 4	1.5	4.6	7.6	1.5	8.6	ns
t_{PHZ}/t_{PLZ}	3-State output disable time OEAB to Bn	Figures 3, 4	1.5	4.0	6.5	1.5	7.5	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$BA to An	Figures 2, 4	1.5	4.4	7.9	1.5	8.9	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$BA to An	Figures 2, 4	1.5	3.7	6.5	1.5	7.5	ns

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ at 0.3V $\geq$ 2.7V
$V_X = V_{OL} + 0.1V_{CC}$ at V_{CC} < 2.7V
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH} - 0.1V_{CC}$ at V_{CC} < 2.7V

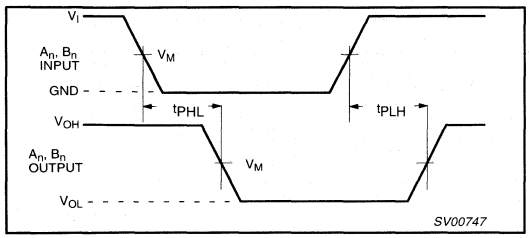


Figure 1. Input (An, Bn) to output (Bn, An) propagation delays.

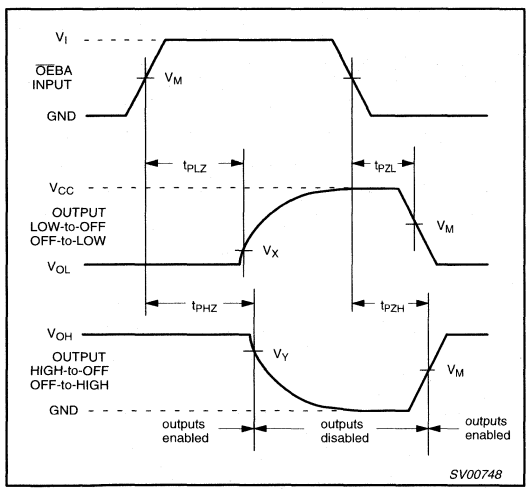


Figure 2. 3-State enable and disable times for $\overline{OE}$BA input

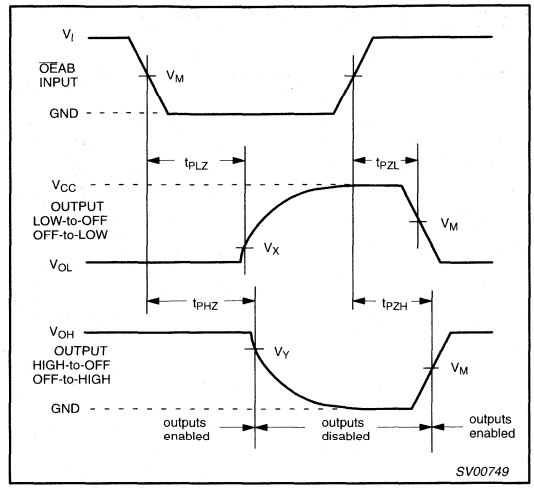
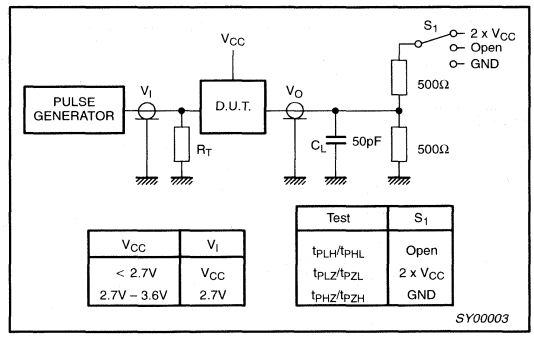


Figure 3. 3-State enable and disable times for OEAB input

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 4. Load circuitry for switching times

Octal bus transceiver/register (3-State) 74LVC646A

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Flow-through pin-out architecture
- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC646A is a high performance, low-power, low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC646A consist of non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropriate clock (CPAB or CPBA) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both. The select source inputs (SAB and SBA) can multiplex stored and real-time (transparent mode) data.

The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode (OE = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '646A' is functionally identical to the '648A' but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Yn	C_L = 50pF V_{CC} = 3.3V	3.9	ns
f_{max}	Maximum clock frequency		250	MHz
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1, 2	26	pF

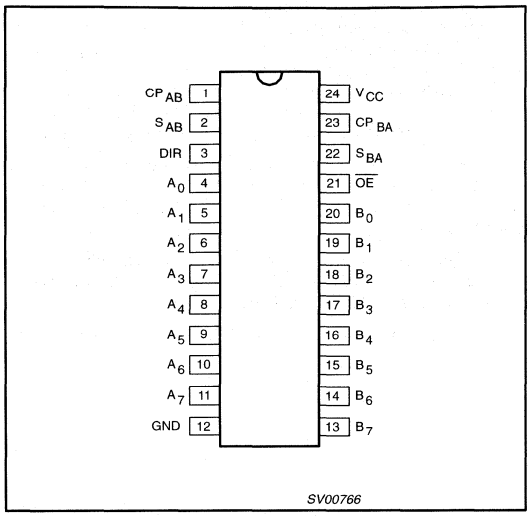
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74LVC646A D	74LVC646A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC646A DB	74LVC646A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC646A PW	7LVC646APW DH	SOT355-1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	CP_{AB}	'A' to 'B' clock input (LOW-to-HIGH, edge-triggered)
2	S_{AB}	Select 'A' to 'B' source input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_7	'A' data inputs/outputs
12	GND	Ground (0V)
20, 19, 18, 17, 16, 15, 14, 13	B_0 to B_7	'B' data inputs/outputs
21	$\overline{OE}$	Output enable input (active LOW)
22	S_{BA}	Select 'B' to 'A' source input
23	CP_{BA}	'B' to 'A' clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	Positive supply voltage

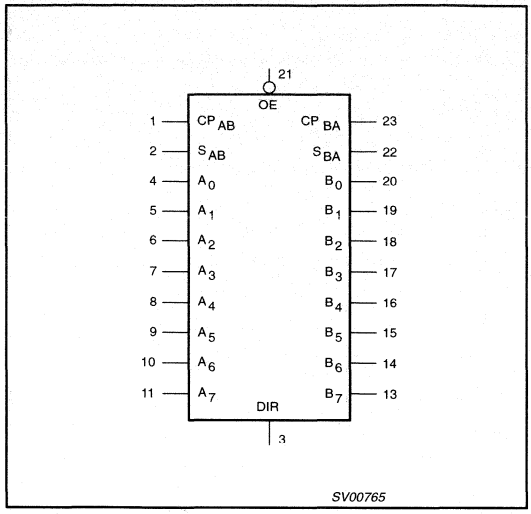
FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
X X	X X	↑ X	X ↑	X X	X X	input un *	un * input	store A, B unspecified * store B, A unspecified *
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

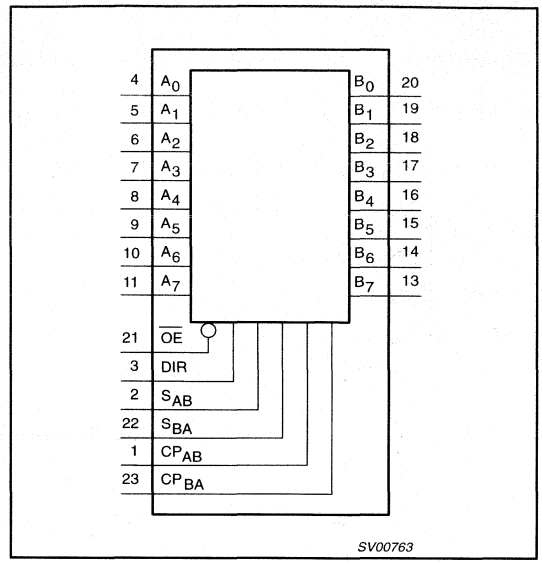
* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH level transition

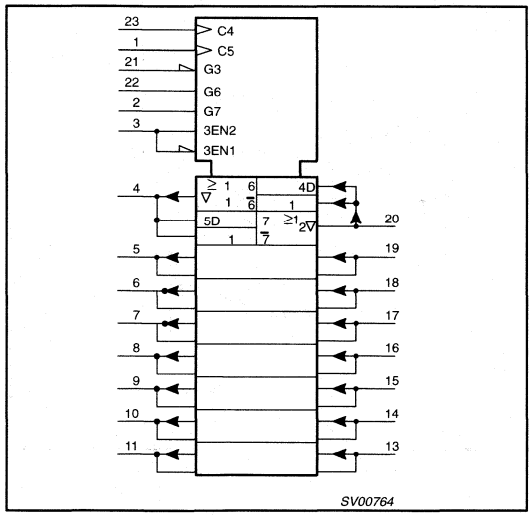
LOGIC SYMBOL



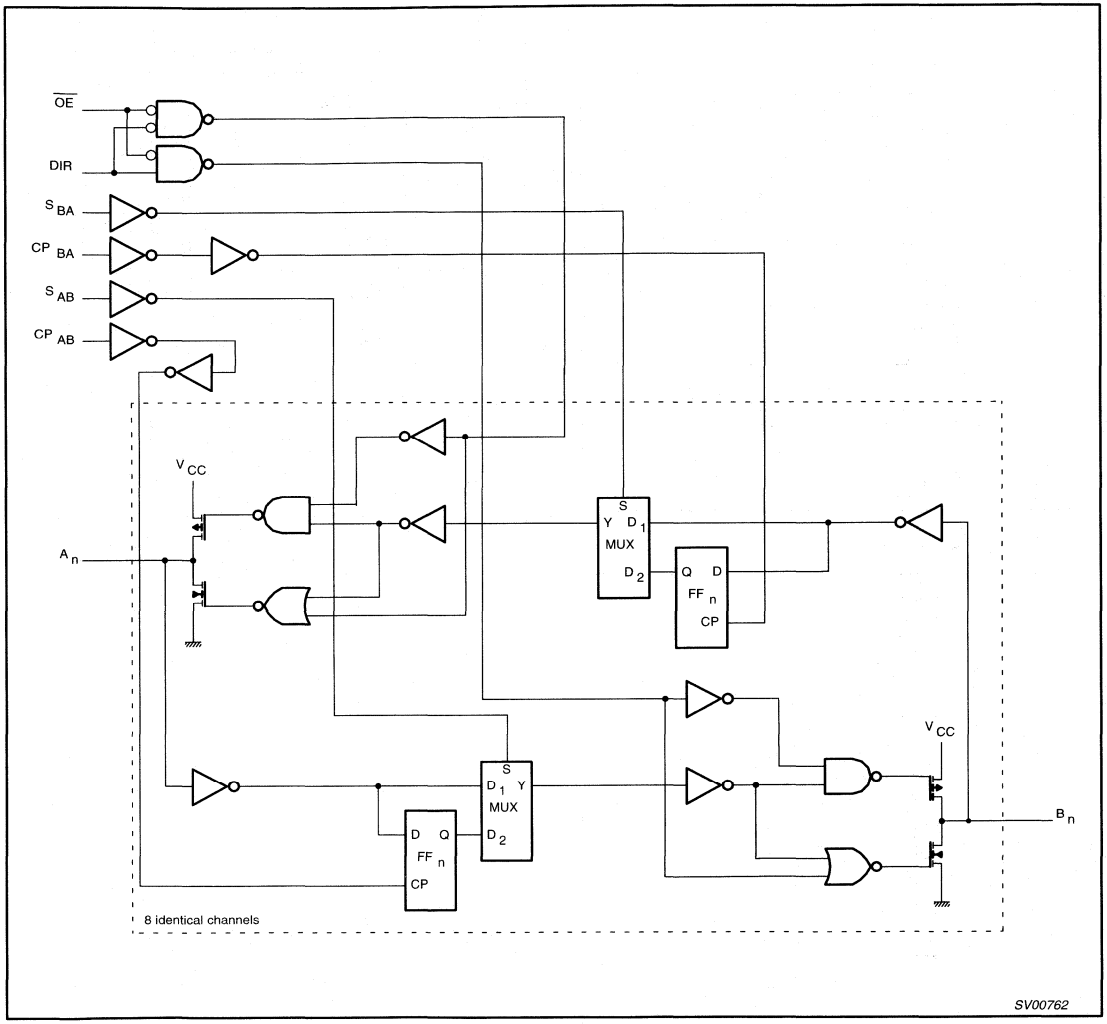
FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output diode current	V_O = 0 to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND; Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; V_I = V_{CC} or GND		±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{OFF}	Power off leakage current	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay An, Bn to Bn, An	Figures 1, 6	1.5	3.9	6.8	1.5	7.8	15	ns
t_{PHL}/t_{PLH}	Propagation delay CP_{AB}, CP_{BA} to B_n, A_n	Figures 2, 6	1.5	4.6	7.6	1.5	8.6	19	ns
t_{PHL}/t_{PLH}	Propagation delay S_{AB}, S_{BA} to B_n, A_n	Figures 3, 6	1.5	4.9	8.5	1.5	9.5	19	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}n$ to An, Bn	Figures 4, 6	1.5	4.5	7.8	1.5	8.8	20	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}n$ to An, Bn	Figures 4, 6	1.5	3.9	6.1	1.5	7.1	10	ns
t_{PZH}/t_{PZL}	3-State output enable time DIR to An, Bn	Figures 5, 6	1.5	4.6	7.9	1.5	8.9	20	ns
t_{PHZ}/t_{PLZ}	3-State output disable time DIR to An, Bn	Figures 5, 6	1.5	3.5	6.0	1.5	7.0	12	ns
t_W	Clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	Figure 1, 3	3.3	1.9	–	3.3	–	–	ns
t_{su}	Set-up time An, Bn to CP_{AB}, CP_{BA}	Figure 2	1.6	0.35	–	1.6	–	–	ns
t_h	Hold time An, Bn to CP_{AB}, CP_{BA}	Figure 2	1.0	–0.3	–	1.0	–	–	ns
f_{max}	Maximum clock pulse frequency	Figure 2	150	250	–	125	–	–	ns

NOTE:

1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$
$V_X = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7V$
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$
$V_Y = V_{OH} - 0.1V_{CC}$ at $V_{CC} < 2.7V$

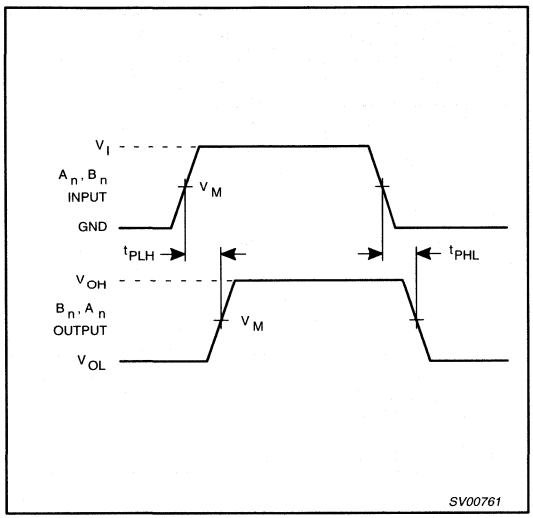


Figure 1. Input An, Bn to output Bn, An propagation delays.

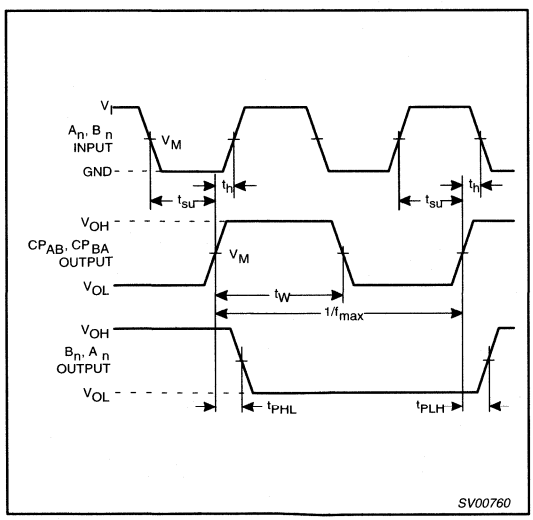


Figure 2. A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

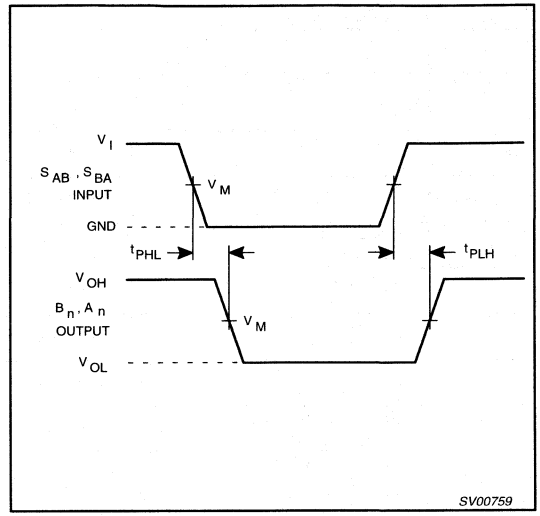


Figure 3. Input S_{AB}, S_{BA} to output B_n, A_n propagation delay times.

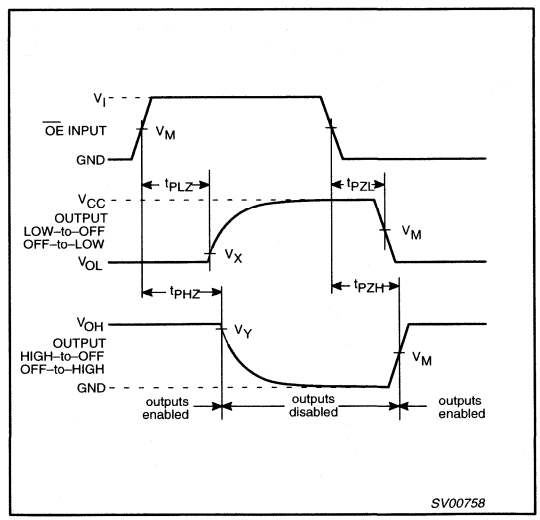


Figure 4. Input $\overline{OE}$ to output A_n, B_n 3-State enable and disable times.

AC WAVEFORMS (*Continued*)

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V
$V_X = V_{OL}$ + 0.1V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH}$ – 0.1V_{CC} at V_{CC} < 2.7V

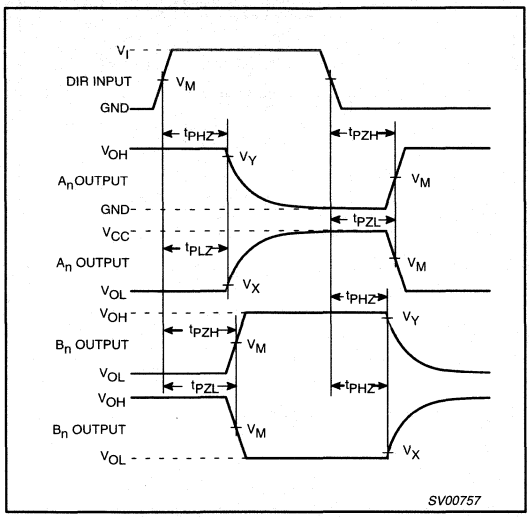
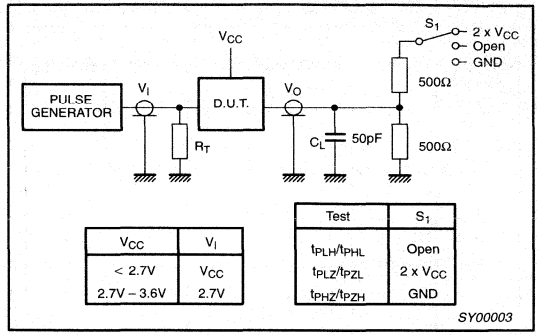


Figure 5. Input DIR to output A_n, B_n 3-State enable and disable times.

TEST CIRCUIT



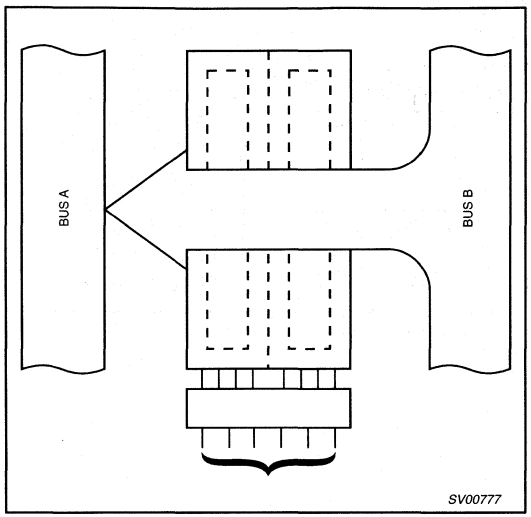
V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 6. Load circuitry for switching times.

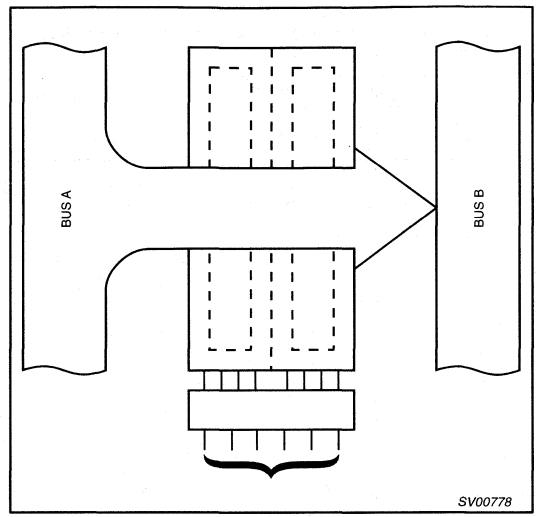
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



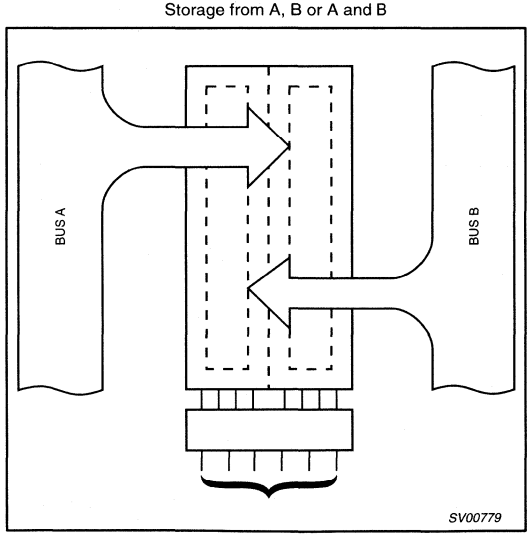
(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



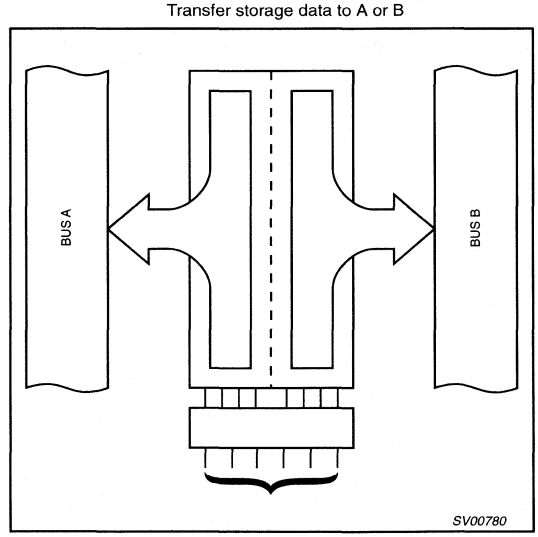
(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	X	↑	X	X	X
X	X	X	↑	X	L
H	X	↑	↑	X	X

Transfer storage data to A or B



(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X

Octal transceiver/register with dual enable (3-State) 74LVC652

*FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC652 is a high performance, low-power, low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC652 consist of 8 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' or both buses, will be stored in the internal registers, at the appropriate clock inputs (CPAB or CPBA) regardless of the select inputs (SAB and SBA) or output enable (OEAB and $\overline{OE}$BA) control inputs. Depending on the select inputs SAB and SBA data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OEn inputs this operating mode permits. The output enable inputs OEAB and OEBA determine the operation mode of the transceiver.

When OEAB is LOW, no data transmission from An to Bn is possible and when $\overline{OE}$BA is HIGH, there is no data transmission from Bn to An possible. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OE}$BA. In this configuration each output reinforces its input.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n; B_n to A_n	C_L = 50pF V_{CC} = 3.3V	5.0	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	45	pF

NOTES:

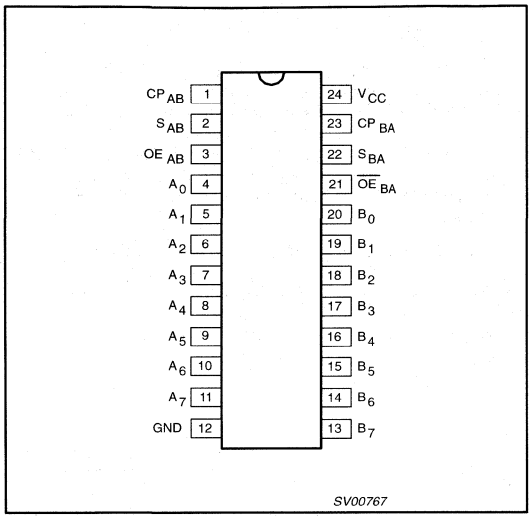
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74LVC652 D	74LVC652 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC652 DB	74LVC652 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC652 PW	4LVC652PW DH	SOT355-1

Octal transceiver/register with dual enable (3-State) 74LVC652

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	CP_{AB}	'A' to 'B' clock input (LOW-to-HIGH, edge-triggered)
2	S_{AB}	Select 'A' to 'B' source input
3	OE_{AB}	Output enable B to A input (active LOW)
4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_7	'A' data inputs/outputs
12	GND	Ground (0V)
20, 19, 18, 17, 16, 15, 14, 13	B_0 to B_7	'B' data inputs/outputs
21	$\overline{OE}_{BA}$	Output enable A to B input
22	S_{BA}	Select 'B' to 'A' source input
23	CP_{BA}	'B' to 'A' clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	Positive supply voltage

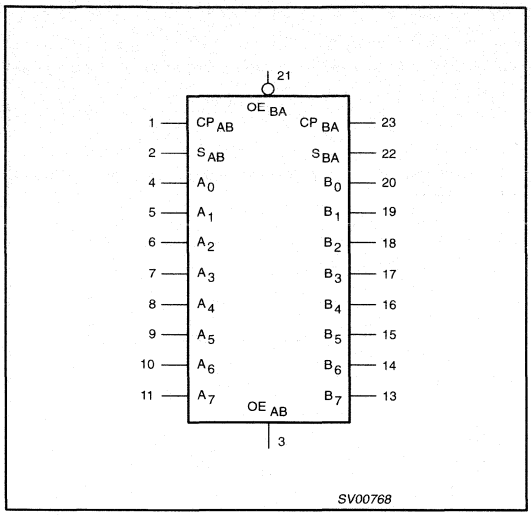
FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un * output	store A, hold B, store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un * output	input input	hold A, store B, store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

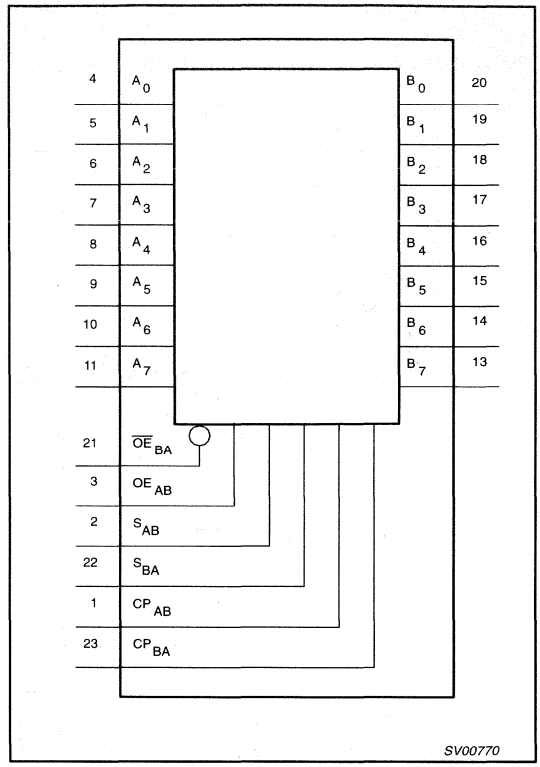
* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW–to–HIGH level transition

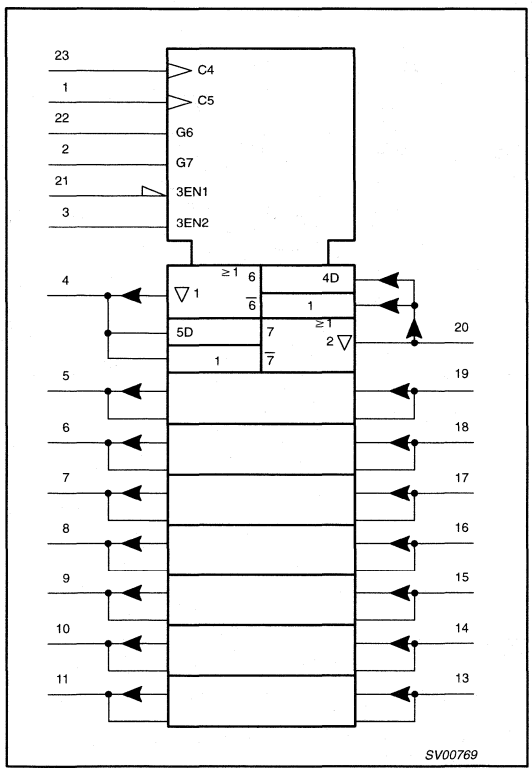
LOGIC SYMBOL



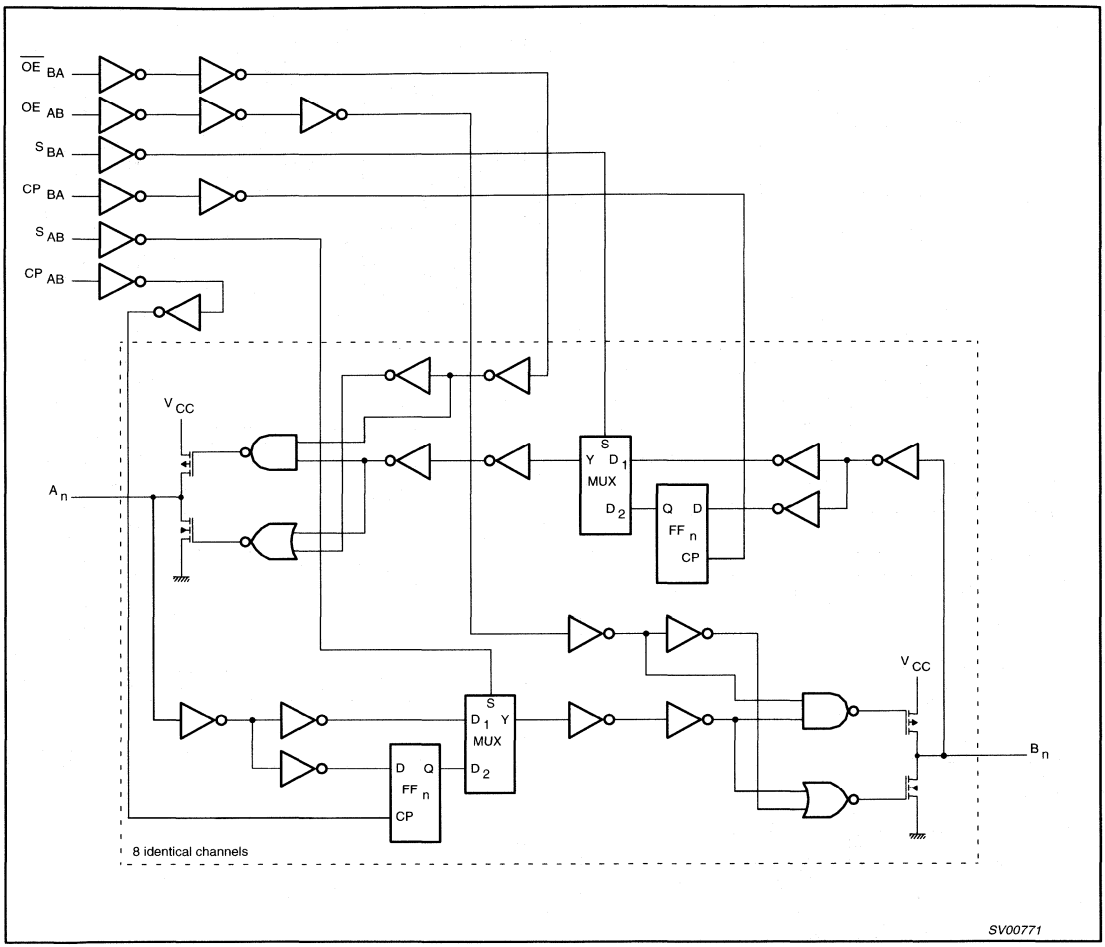
FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input voltage range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output diode current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND | Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{OFF}	Power off leakage current	V_{CC} = 0.0V; V_I = 5.5V; V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V		
			MIN	TYP[1]	MAX	MIN	MAX	MIN	TYP	
t_{PHL}/t_{PLH}	Propagation delay An to Bn, Bn to An	Figures 1, 5	1.5	4.6	7.9	1.5	9.2	1.5	24	ns
t_{PHL}/t_{PLH}	Propagation delay CP_{AB}, CP_{BA} to B_n, A_n	Figures 2, 5	1.5	5.2	8.9	1.5	11	1.5	26	ns
t_{PHL}/t_{PLH}	Propagation delay S_{AB}, S_{BA} to B_n, A_n	Figures 3, 5	1.5	5.2	8.8	1.5	11	1.5	27	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}_{AB}$ to Bn	Figures 4, 5	1.5	4.8	8.0	1.5	10	1.5	20	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}_{AB}$ to Bn	Figures 4, 5	1.5	4.4	8.0	1.5	10	1.5	10	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An	Figures 4, 5	1.5	4.8	8.0	1.5	10	1.5	20	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}_{BA}$ to An	Figures 4, 5	1.5	4.4	8.0	1.5	10	1.5	10	ns
t_W	Clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	Figures 4, 5	–	3.0	–	3.0	–	–	–	ns
t_{su}	Set-up time An, Bn to CP_{AB}, CP_{BA}	Figure 2	1.5	0.5	–	1.5	–	–	–	ns
t_h	Hold time An, Bn to CP_{AB}, CP_{BA}	Figure 2	1.0	0	–	1.0	–	–	–	ns
f_{max}	Maximum clock pulse frequency	Figure 2	7.5	150	–	–	–	–	–	MHz

NOTE:

1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V

V_M = 0.5V * V_{CC} at V_{CC} < 2.7V

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$

$V_X = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7V$

$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$

$V_Y = V_{OH} - 0.1V_{CC}$ at $V_{CC} < 2.7V$

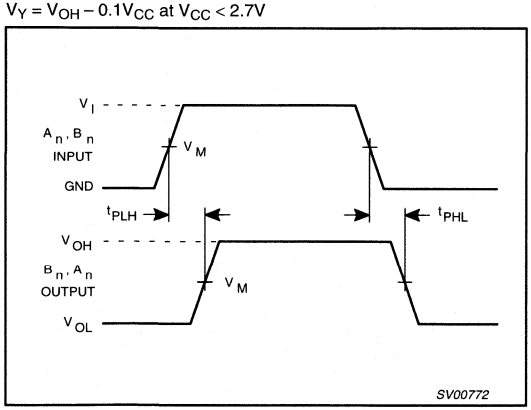


Figure 1. Input An, Bn to output Bn, An propagation delays.

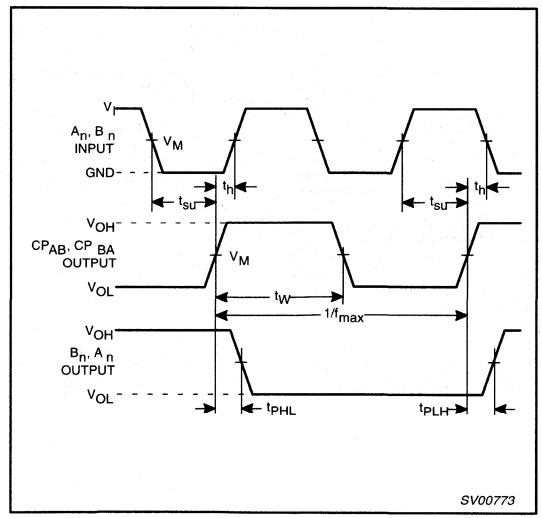


Figure 2. A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

AC WAVEFORMS (Continued)

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V
$V_X = V_{OL}$ + 0.1V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH}$ – 0.1V_{CC} at V_{CC} < 2.7V

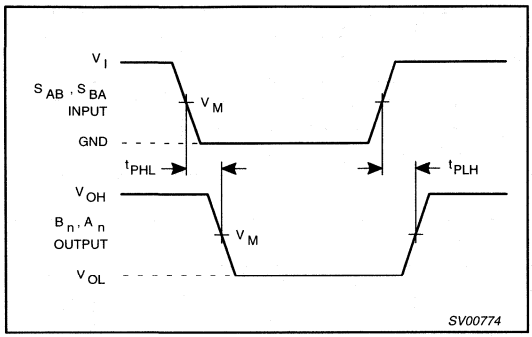


Figure 3. Input S_{AB}, S_{BA} to output B_n, A_n propagation delay times.

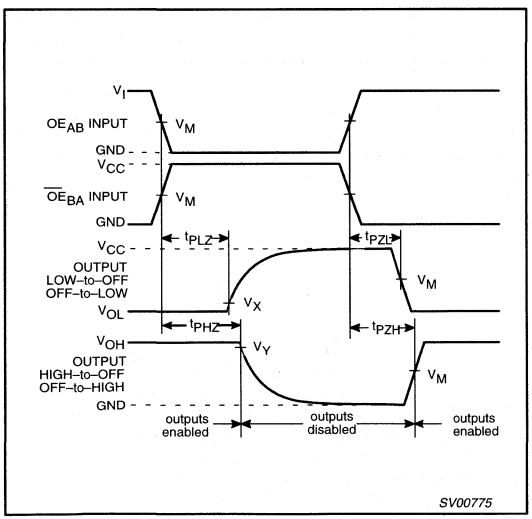
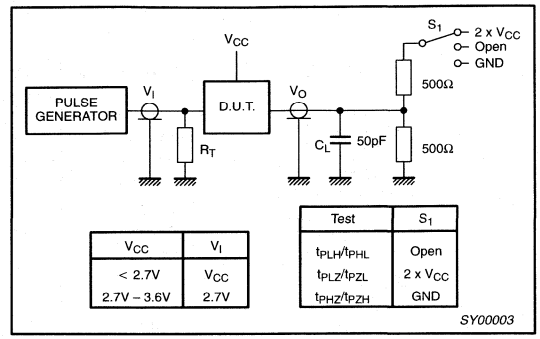


Figure 4. OE inputs (OE_{AB}, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times.

TEST CIRCUIT



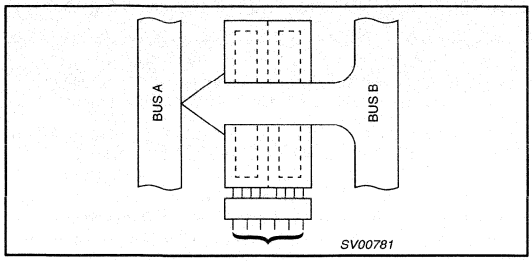
V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 5. Load circuitry for switching times.

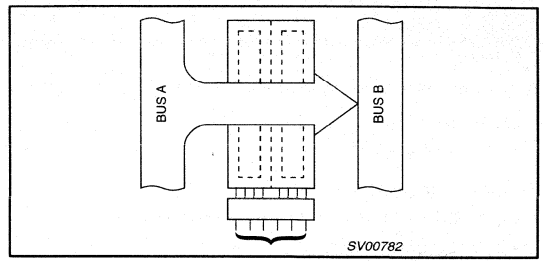
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



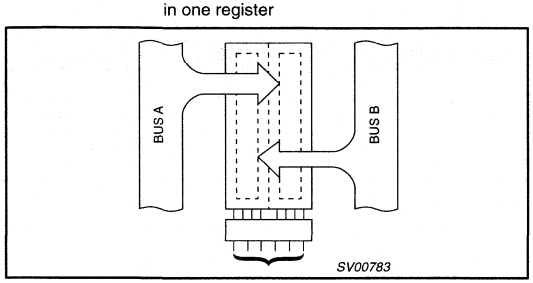
OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



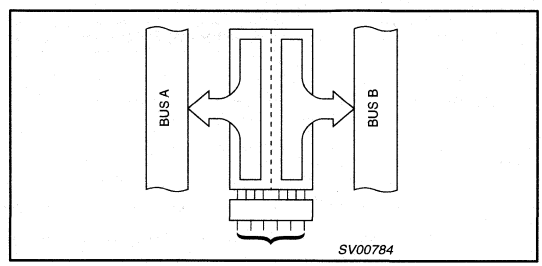
OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	X	X	L	X

Store A, B or A and B in one register



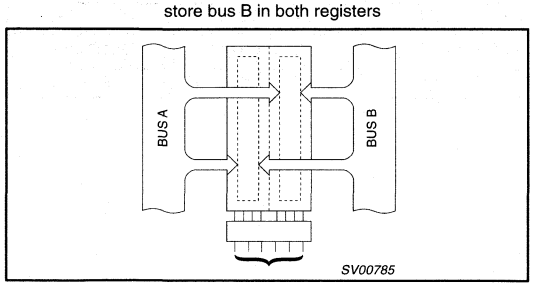
OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	H	↑	↑	L	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer A stored data to B bus or B stored data to A bus or both at the same time



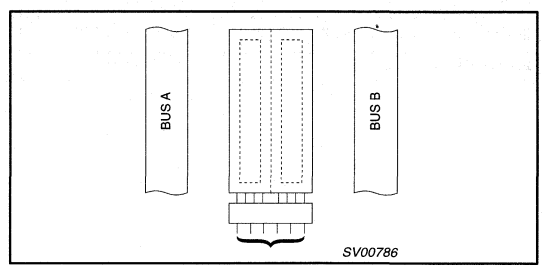
OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store bus A in both registers or store bus B in both registers



OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	H or L	H or L	X	X

10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC821A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 10-bit positive edge-triggered register
- Independent register and 3-State buffer operation
- Flow-through pin-out architecture

DESCRIPTION

The 74LVC821A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-state operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC821A is a10-bit D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus-oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops. The ten flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition. When $\overline{OE}$ is LOW, the contents of the ten flip-flops is available at the outputs.

When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	4.8	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	28	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74LVC821A D	74LVC821A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC821A DB	74LVC821A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC821A PW	7LVC821APW DH	SOT355-1

10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State) 74LVC821A

PIN DESCRIPTION

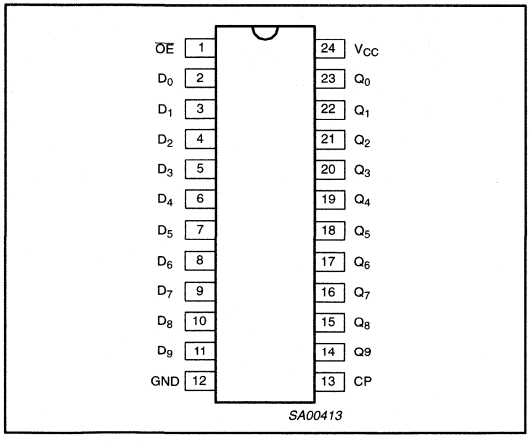
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D_0 to D_9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q_0 to Q_9	3-State flip-flop outputs
12	GND	Ground (0 V)
13	CP	Clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

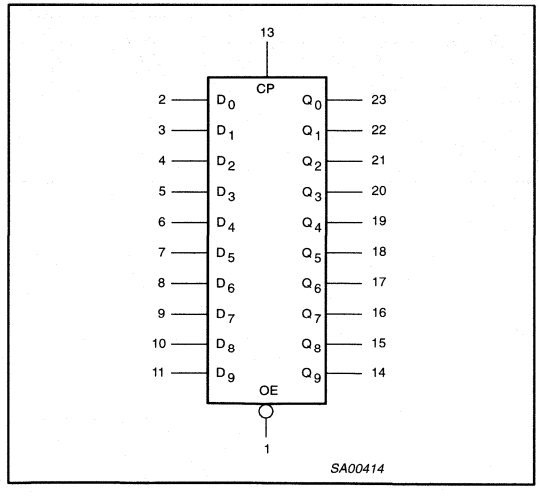
OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_9
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	Z Z
Hold	L	H or L	X	NC	NC

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW–to–HIGH clock transition
NC= no change

PIN CONFIGURATION



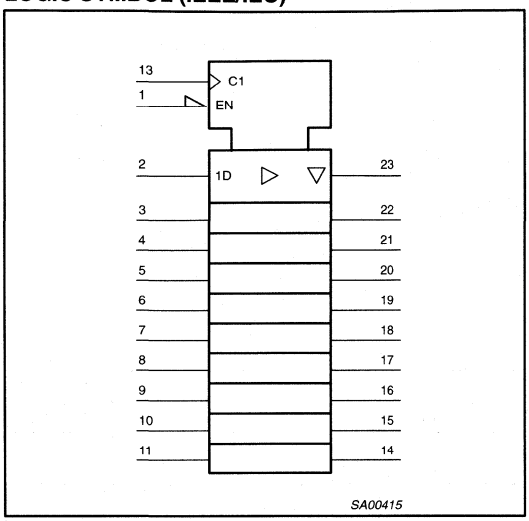
LOGIC SYMBOL



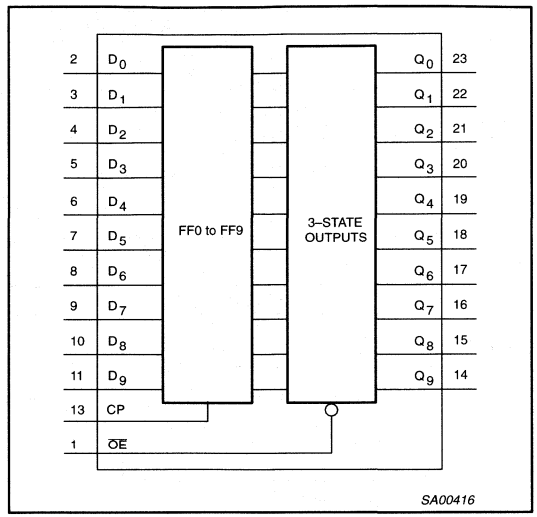
10-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC821A

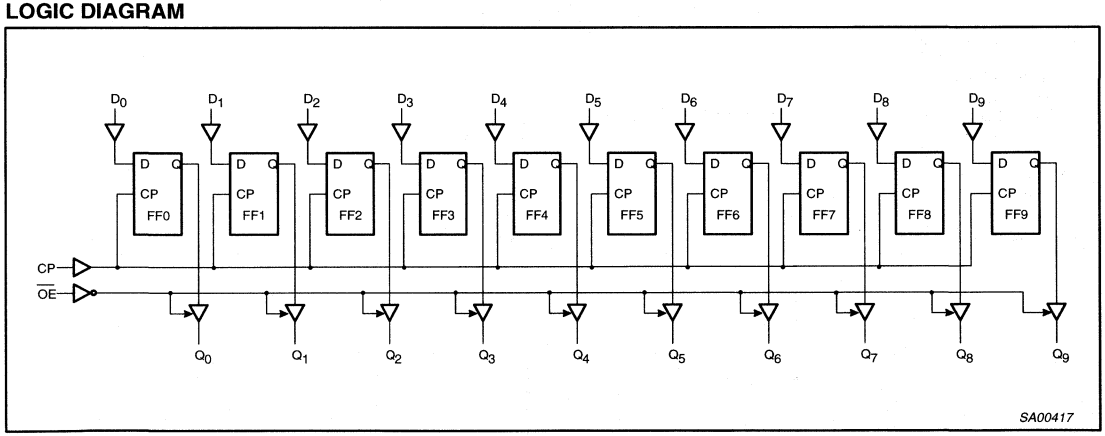
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq$ 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay CP to Q_n	Figures 1, 4	–	–	7.0	–	8.0	–	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	Figures 2, 4	–	–	8.0	–	8.5	–	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	Figures 2, 4	–	–	7.0	–	7.5	–	ns
t_W	Clock pulse width HIGH or LOW	Figure 1	5.0	3.0	–	5.0	–	–	ns
t_{SU}	Setup time D_n to CP	Figure 3	1.0	0.3	–	1.0	–	–	ns
t_h	Hold time D_n to CP	Figure 3	1.0	–0.2	–	1.0	–	–	ns
f_{max}	Maximum clock pulse frequency	Figure 1	75	150	–	–	–	–	MHz

NOTE:
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ −0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ − 0.1 V_{CC} at V_{CC} < 2.7V

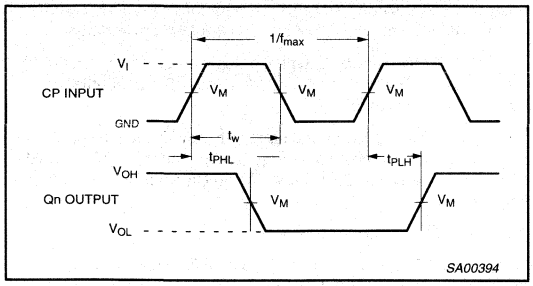


Figure 1. Clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

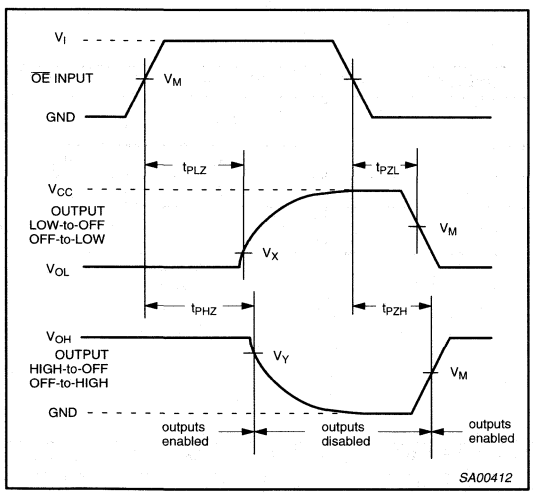


Figure 2. 3-State enable and disable times.

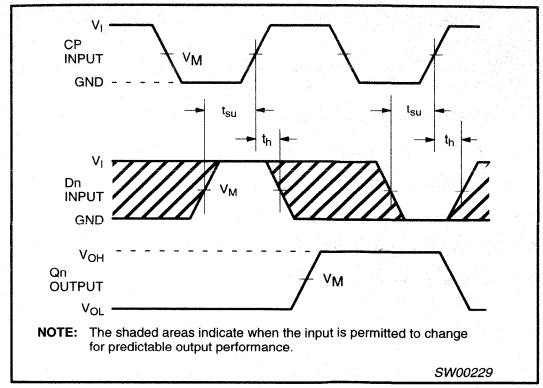


Figure 3. Data setup and hold times for the D_n input to the CP input.

TEST CIRCUIT

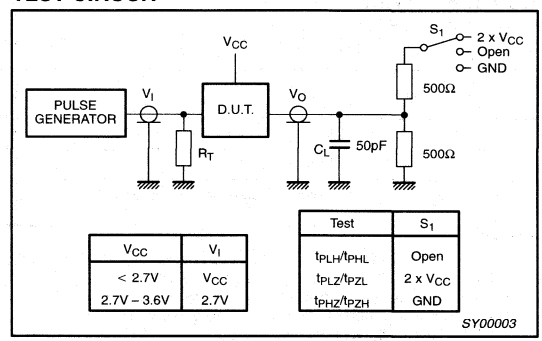


Figure 4. Load circuitry for switching times.

9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC823A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 9-bit positive edge-triggered register
- Independent register and 3-State buffer operation
- Flow-through pin-out architecture

DESCRIPTION

The 74LVC823A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-state operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC823A is a 9-bit D-type flip-flop with common clock (CP), Clock Enable ($\overline{CE}$), Master Reset ($\overline{MR}$) and 3-State outputs for bus-oriented applications.

The nine flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition provided $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH the flip-flops hold their data.

A LOW on $\overline{MR}$ resets all flip-flops.

When $\overline{OE}$ is LOW, the contents of the nine flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	4.8	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	Notes 1 and 2	28	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74LVC823A D	74LVC823A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC823A DB	74LVC823A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC823A PW	7LVC823APW DH	SOT355-1

9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC823A

PIN DESCRIPTION

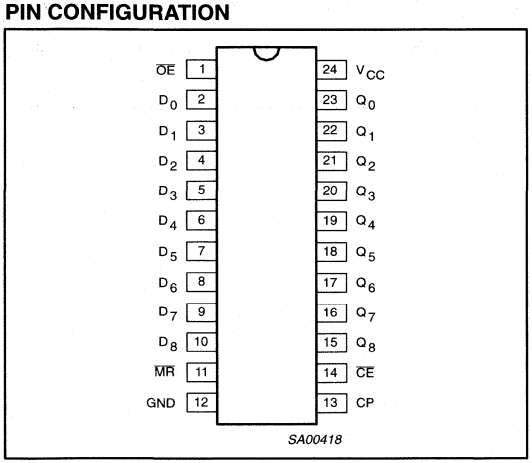
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10	D_0 to D_8	Data inputs
11	$\overline{MR}$	Master reset (active LOW)
12	GND	Ground (0 V)
13	CP	Clock pulse (active rising)
14	$\overline{CE}$	Clock enable (active LOW)
23, 22, 21, 20, 19, 18, 17, 16, 15	Q_0 to Q_8	3-State flip-flop outputs
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS					INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	D_n		Q_0 to Q_8
Clear	L	L	X	X	X	L	L
Load and read register	L L	H H	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	H H	L L	X X	l h	L H	Z Z
Hold	L	H	H	NC	X	NC	NC

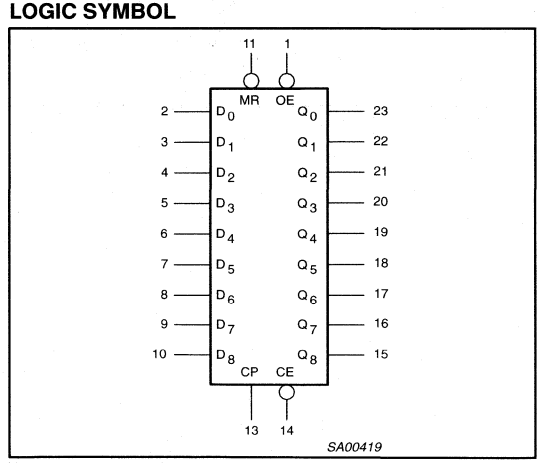
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW–to–HIGH clock transition
NC= no change

PIN CONFIGURATION



SA00418

LOGIC SYMBOL

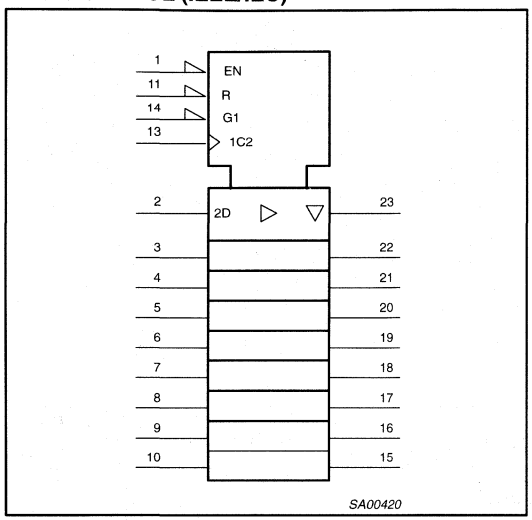


SA00419

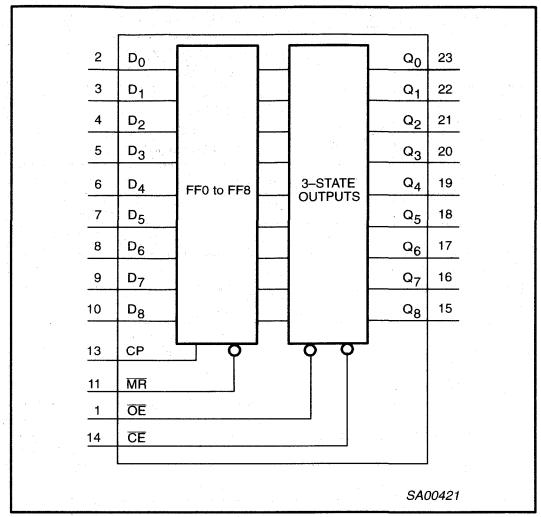
9-bit D-type flip-flop with 5-volt tolerant inputs/outputs; positive-edge trigger (3-State)

74LVC823A

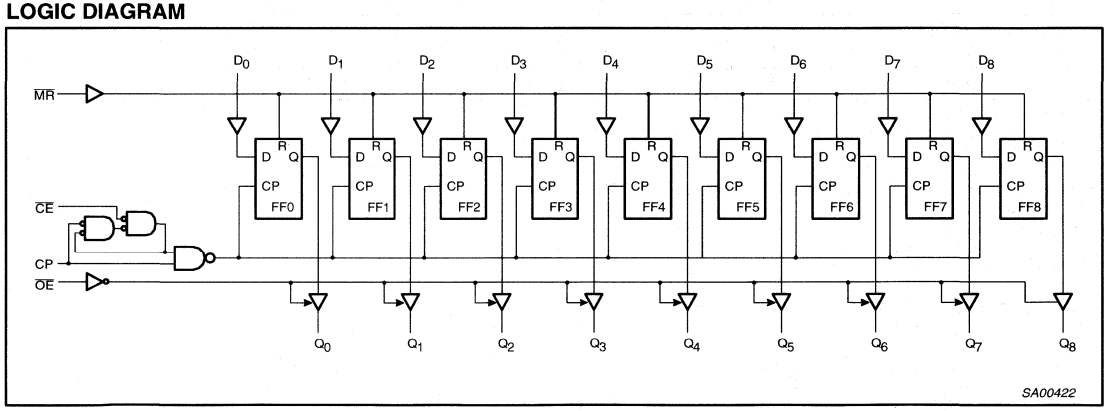
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq$ 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay CP to Q_n	Figures 1, 4	–	–	8.5	–	9.5	–	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Q_n	Figures 2, 4	–	–	8.0	–	8.5	–	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Q_n	Figures 2, 4	–	–	7.0	–	7.5	–	ns
t_W	Clock pulse width HIGH or LOW	Figure 1	–	3.0	–	–	–	–	ns
t_{SU}	Setup time D_n to CP	Figure 3	1.0	0.3	–	1.0	–	–	ns
t_h	Hold time D_n to CP	Figure 3	1.0	–0.2	–	1.0	–	–	ns
f_{max}	Maximum clock pulse frequency	Figure 1	75	150	–	–	–	–	MHz

NOTE:
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at V_{CC} ≥ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ −0.3V at V_{CC} ≥ 2.7V; $V_Y = V_{OH}$ − 0.1 V_{CC} at V_{CC} < 2.7V

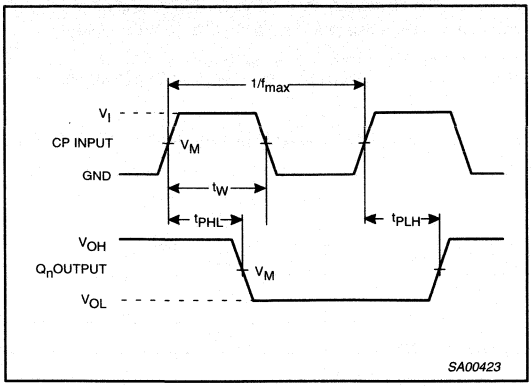


Figure 1. Clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

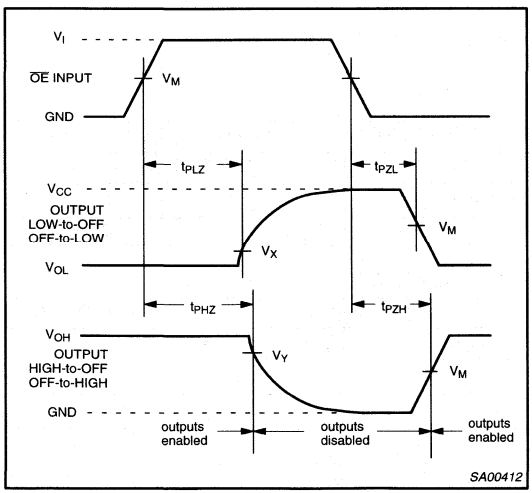


Figure 2. 3-State enable and disable times.

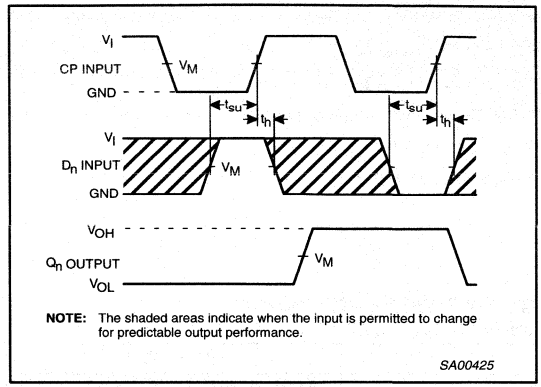
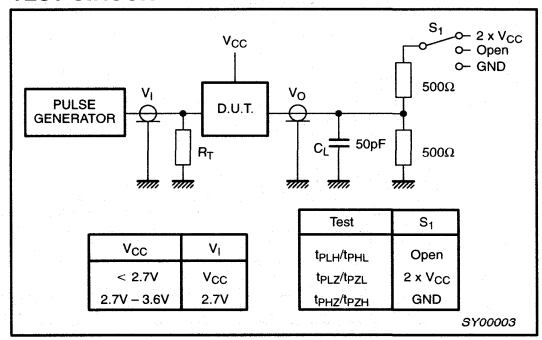


Figure 3. Data setup and hold times for the D_n input to the CP input.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 4. Load circuitry for switching times.

10-bit buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC827A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when V_{CC} = 0V

DESCRIPTION

The 74LVC827A is a high performance, low-power, low-voltage Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-state operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC827A is a10-bit buffer/line driver with 3-State outputs The 3-State outputs are controlled by the output enable inputs $\overline{OE}_1$ and $\overline{OE}_2$.

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n to Y_n	C_L = 50 pF; V_{CC} = 3.3 V	4	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1 and 2	24	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74LVC827A D	74LVC827A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC827A DB	74LVC827A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC827A PW	7LVC827APW DH	SOT355-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{OE}_1$, $\overline{OE}_2$	Output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_9	Data inputs
12	GND	Ground (0 V)
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Y_0 to Y_9	Bus outputs
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

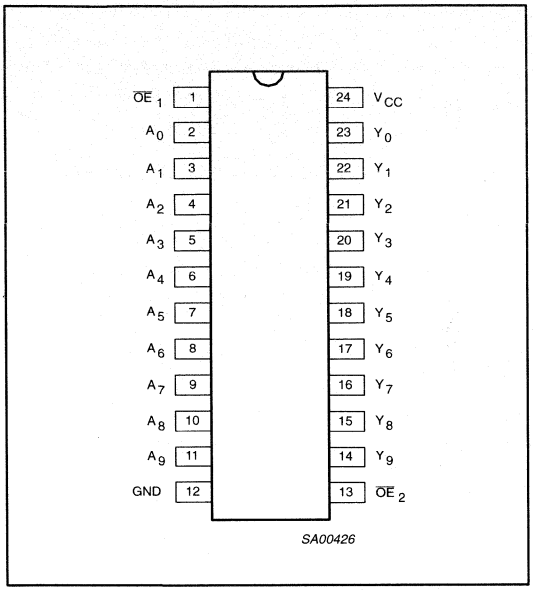
INPUTS			OUTPUTS
$\overline{OE}_1$	$\overline{OE}_2$	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = high impedance OFF-state

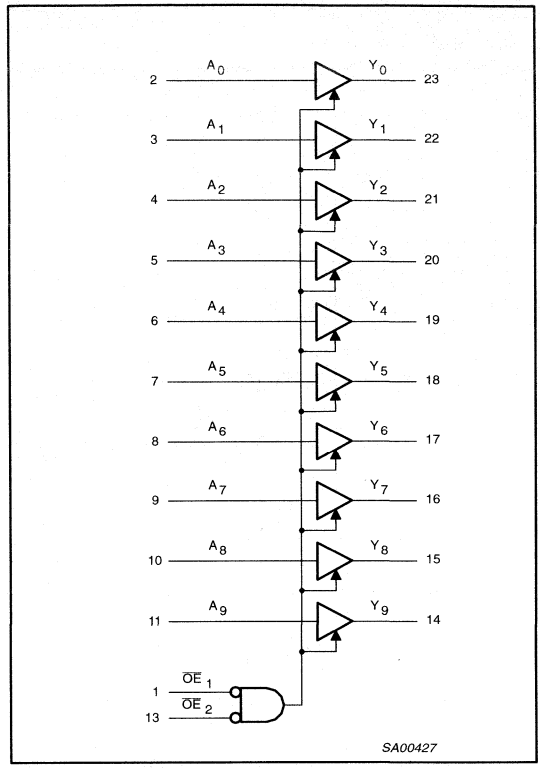
10-bit buffer/line driver with 5-volt tolerant inputs/outputs (3-State)

74LVC827A

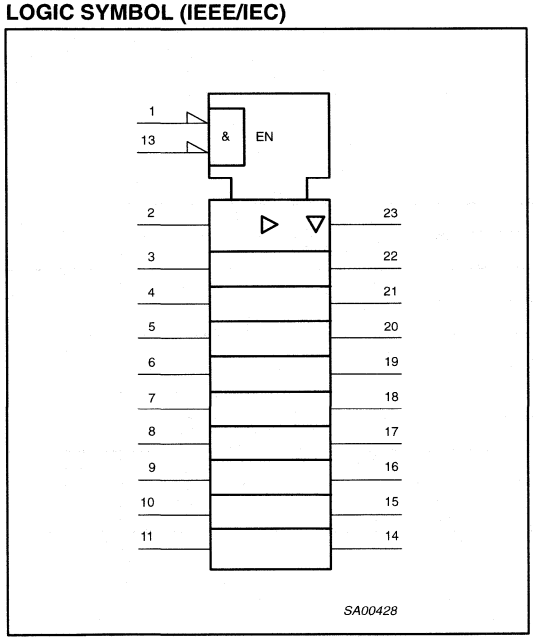
PIN CONFIGURATION



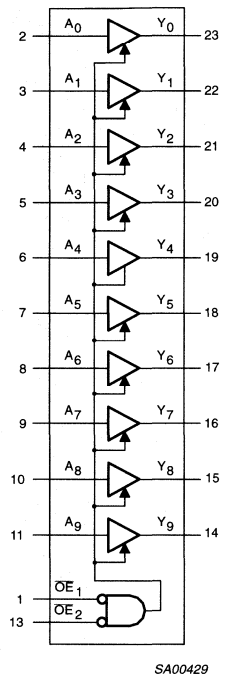
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free-air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	−0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	−0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

DC ELECTRICAL CHARACTERISTICS *(Continued)*

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND	Not for I/O pins		±0.1	±5	μA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND			0.1	±5	μA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V			0.1	±10	μA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0			0.1	10	μA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0			5	500	μA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq$ 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	Figures 1, 3	1.5	4.0	6.7	1.5	7.1	15	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_1$ to $1Y_n$; $\overline{OE}_2$ to $2Y_n$	Figures 2, 3	1.5	5.4	8.5	1.5	9.5	25	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}_1$ to $1Y_n$; $\overline{OE}_2$ to $2Y_n$	Figures 2, 3	1.5	4.0	6.7	1.5	7.3	11	ns

NOTE:
1. Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V

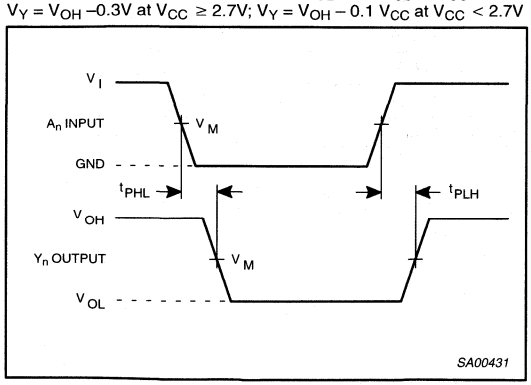


Figure 1. The input (A_n) to output (Y_n) propagation delays.

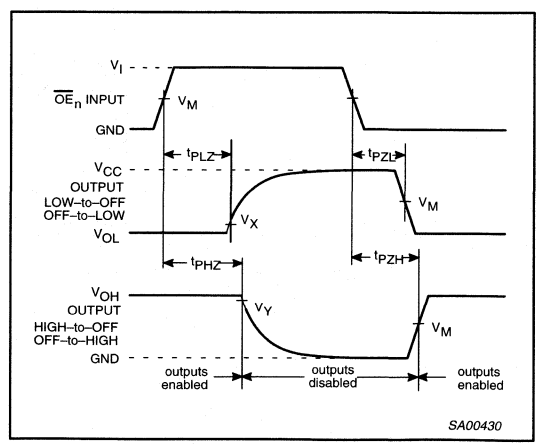
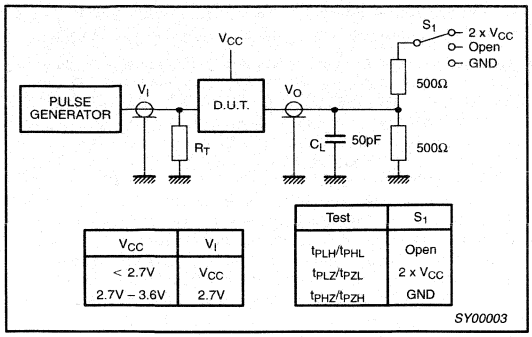


Figure 2. 3-State enable and disable times.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 3. Load circuitry for switching times.

10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State)

74LVC841A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with the JEDEC standard no. 8-1 A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Flow-through pin-out architecture

DESCRIPTION

The 74LVC841A is a low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-State operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment. The 74LVC841A is a 10-bit transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches. The 74LVC841A consists of ten transparent latches with 3-State true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the ten latches are available at the outputs.

When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n; LE to Q_n	C_L = 50 pF; V_{CC} = 3.3 V	 4.5 5.0	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	22	pF

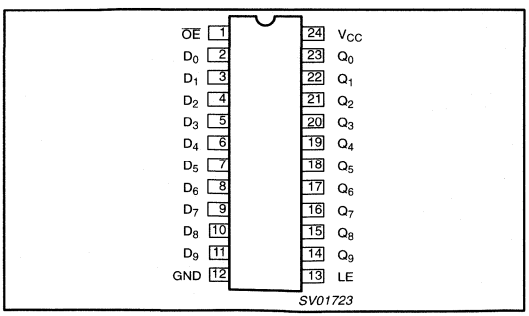
NOTE:

1 C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +125°C	74LVC841A D	74LVC841A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +125°C	74LVC841A DB	74LVC841A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +125°C	74LVC841A PW	7LVC841APW DH	SOT355-1

PIN CONFIGURATION

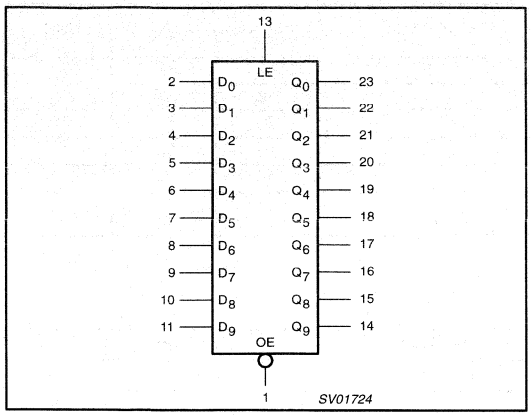


PIN DESCRIPTION

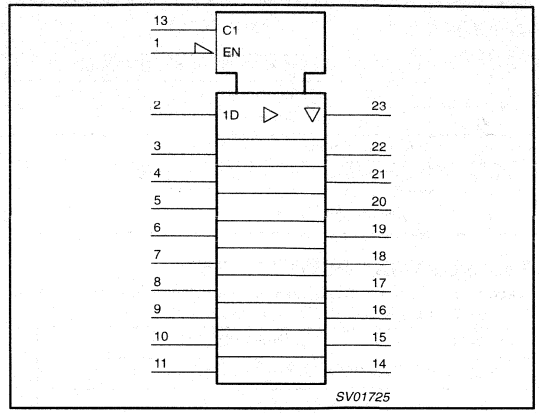
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	D_0 to D_9	Data inputs
23, 22, 21, 20, 19, 18, 17, 16, 15, 14	Q_0 to Q_9	3-state latch outputs
12	GND	Ground (0 V)
13	LE	Latch enable input (active HIGH)
24	V_{CC}	Positive supply voltage

10-bit transparent latch with 5-volt tolerant inputs/outputs (3-State) 74LVC841A

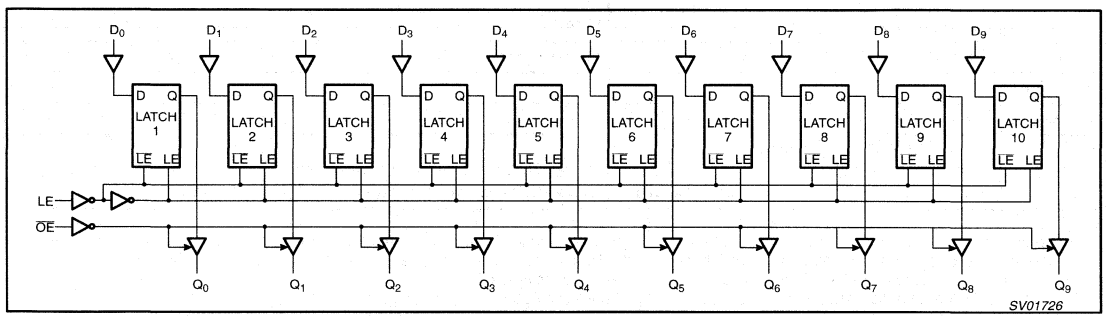
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE for register A_n or B_n

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 TO Q_9
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register	L L	↓ ↓	l h	L H	L H
latch register and disable outputs	H H	X X	l h	L H	Z Z
Hold	L	L	X	NC	NC

NOTES:

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state
NC = no change

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	±5	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTE:
1 All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500Ω; T_{amb} = –40°C to +85°C

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay D_n to Q_n	Figures 1, 5	1.5	4.5	6.7	1.5	7.5	ns
t_{PHL}/t_{PLH}	Propagation delay LE to Q_n	Figures 2, 5	1.5	4.9	7.6	1.5	8.6	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	Figures 3, 5	1.5	5.4	7.9	1.5	8.9	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	Figures 3, 5	1.5	3.8	5.9	1.5	6.9	ns
t_w	LE pulse width, HIGH	Figure 4	2.0	0.7	–	2.0		ns
t_{su}	Set-up time D_n to LE	Figure 4	2.0	0.5	–	2.0		ns
t_h	Hold time D_n to LE	Figure 4	1.0	–0.5	–	1.0		ns

NOTE:
1 All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V
V_M = 0.5 V × V_{CC} at V_{CC} < 2.7 V
V_M = 1.5 V at V_{CC} = 3.0 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V
$V_X = V_{OL}$ + 0.1 × V_{CC} at V_{CC} < 2.7 V
$V_Y = V_{OH}$ – 0.3 V at $V_{CC} \geq$ 2.7 V
$V_Y = V_{OH}$ – 0.1 × V_{CC} at V_{CC} < 2.7 V

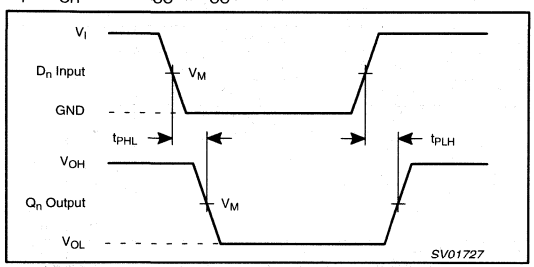


Figure 1. Input (D_n) to output (Q_n) propagation delays.

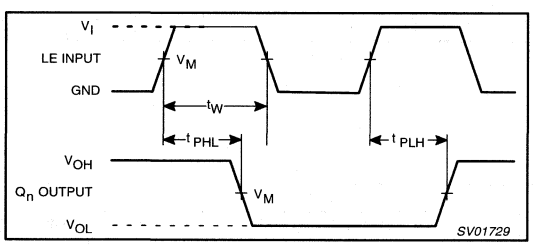


Figure 2. Latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays.

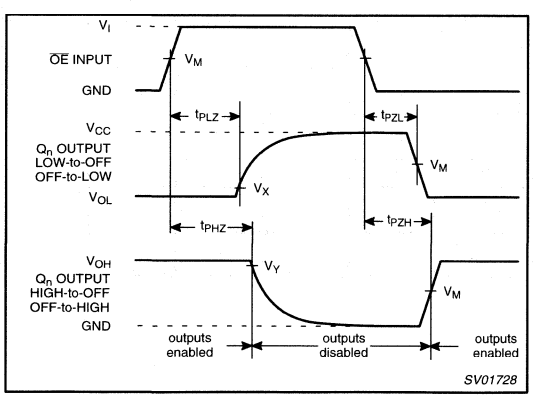


Figure 3. 3-State enable and disable times.

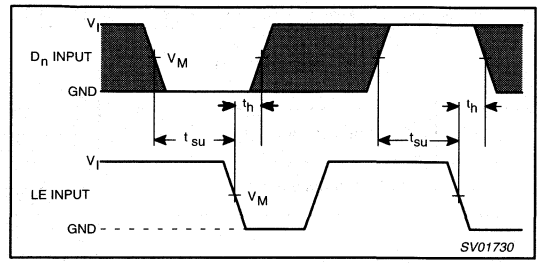
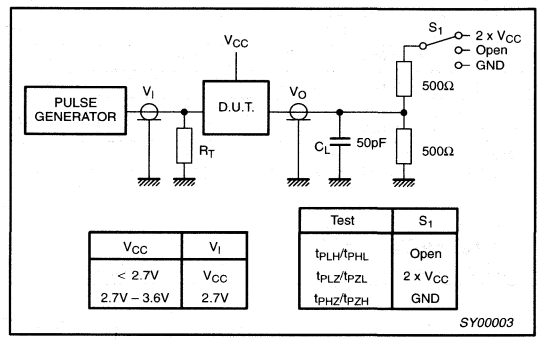


Figure 4. Data set-up and hold times for the D_n input to LE input.

Note to Figure 4: The shaded areas indicate when the input is permitted to change for predictable output performance

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 5. Load circuitry for switching times.

3.3V Parallel printer interface transceiver/buffer 74LVC1284

FEATURES

- Asynchronous operation
- 4-Bit transceivers
- 3 additional buffer/driver lines
- TTL compatible inputs
- ESD protection exceeds 1000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Input Hysteresis
- Low Noise Operation
- Center Pin V_{CC} & GND
- IEEE 1284 Compliant Level 1 & 2
- Overvoltage Protection on B side

DESCRIPTION

The 74LVC1284 parallel interface chip is designed to provide an asynchronous, 4-bit, bi-directional, parallel printer interface for personal computers. Three additional lines are included to provide handshaking signals between the host and the peripheral. The part is designed to match IEEE 1284 standard.

The 4 transceiver pins (A/B 1-4) allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending on the state of the direction pin DIR.

The B bus and the Y5-Y7 lines have totem pole or open drain style outputs depending on the state of the high drive enable pin HD. The A bus only has totem pole style outputs. All inputs are TTL compatible with at least 300mV of input hysteresis at V_{CC} = 3.3V.

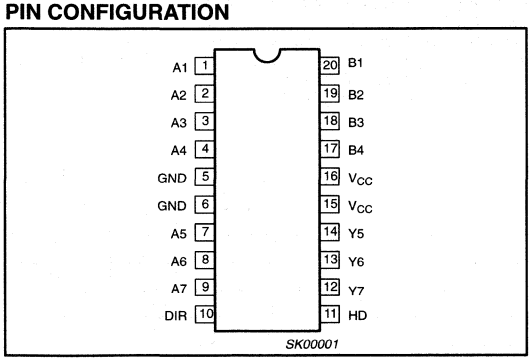
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
R_D	B/Y Side output resistance	V_{CC} = 3.3V; V_O = 1.65V ±0.2V (See Figure 2)	45	Ω
SR	B/Y Side slew rate	R_L = 62Ω; C_L = 50pF (See Waveform 4)	0.2	V/ns
I_{CC}	Total static current	V_I = V_{CC}/GND; I_O = 0	5	µA
V_{HYS}	Input hysteresis	V_{CC}= 3.3V	0.4	V
t_{PLH}/t_{PHL} A –B/Y	Propagation delay to the B/Y side outputs	V_{CC} = 3.3V	12.6/12.4	ns

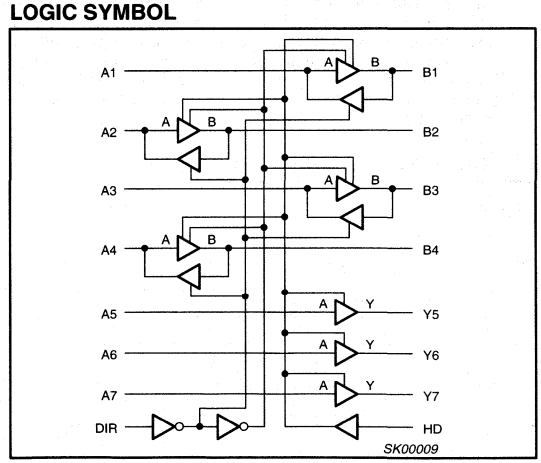
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-pin plastic SO	0°C to +70°C	7LVC1284 D	SOT163-1
20-pin plastic SSOP Type II	0°C to +70°C	74LVC1284 DB	SOT339-1
20-pin plastic TSSOP Type I	0°C to +70°C	74LVC1284 PW	SOT360-1

PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1,2,3,4	A1 - A4	Data inputs/outputs
20,19,18,17	B1 - B4	IEEE 1284 Std. outputs/inputs
7,8,9	A5 - A7	Data inputs
14,13,12	Y5 - Y7	IEEE 1284 Std. outputs
10	DIR	Direction selection
11	HD	B/Y–side high drive enable/disable
5,6	GND	Ground (0V)
15,16	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	INPUTS/OUTPUTS	
DIR	HD	A5-7	Y5-7	A1-4	B1-4
L	L	L	L	A = B	Inputs
L	L	H	Z	A = B	Inputs
L	H	L	L	A = B	Inputs
L	H	H	H	A = B	Inputs
H	L	L	L	Inputs Low	Outputs Low
H	L	H	Z	Inputs High	Outputs Z
H	H	L	L	Inputs	B = A
H	H	H	H	Inputs	B = A

H = High Voltage
L = Low Voltage
Z = High Impedance, Off-State

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
	ESD Immunity, per Mil Std 883C method 3015		±2	kV
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	±20	mA
I_{OK}	DC output diode current	$V_O < 0$	±50	mA
V_{IN}	DC input voltage[3]		–0.5 to +5.5	V
V_{OUT} B/Y_{DC}	DC output voltage on B/Y side[3]		–0.5 to +5.5	V
V_{OUT} B/Y (tr)	Transient output voltage on B/Y side[4]	40ns transient	–2 to +7	V
V_{OUT} A side	DC output voltage on A side		–0.5 to V_{CC} +0.5	V
I_O	DC output current	Outputs in High or Low state	±50	mA
T_{stg}	Storage temperature range		–60 to +150	°C
I_{CC}/I_{GND}	Continuous current through V_{CC} or GND		±200	mA

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. V_{OUT} B/Y (tr) guarantees only that this part will not be damaged by reflections in application so long as the voltage levels remain in the specified range.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	3.0	3.6	V
V_I	Input voltage	0	V_{CC}	V
V_{OUT}	B/Y output voltage	–0.5	5.5	V
V_{OUT}	A side output voltage	0	V_{CC}	V
I_{OH}	B/Y side output current High		–14	mA
I_{OL}	B/Y side output current Low		14	mA
T_{amb}	Operating free-air temperature range	0	+70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = 25°C			T_{amb} = 0°C to +70°C		
				MIN	TYP	MAX	MIN	MAX	
V_{OH}	High-level output voltage	An	V_{CC} = Min to Max; I_{OH} = –50µA	V_{CC}–0.2	V_{CC}		V_{CC}–0.2		V
			V_{CC} = 3.0V; I_{OH} = –4mA	2.4			2.4		V
		Bn or Yn	V_{CC} = 3.0V; I_{OH} = 14mA	2.2	2.4		2.1		V
V_{OL}	Low-level output voltage	An	V_{CC} = Min to Max; I_{OL} = 50µA; V_I = V_{IL} or V_{IH}			0.2		0.2	V
			V_{CC} = 3.0V; I_{OL} = 4mA; V_I = V_{IL} or V_{IH}			0.4		0.4	V
		Bn or Yn	V_{CC} = 3.0V; I_{OL} = –14mA; V_I = V_{IL} or V_{IH}			0.8		0.9	V
V_{IH}	High-level input voltage		V_{CC} = Min to Max			0.8		0.8	
V_{IL}	Low-level input voltage		V_{CC} = Min to Max	2.0			2.0		
V_{HYS}	Input Hysteresis		V_{CC} = 3.3V		0.4		0.3		V
R_D	B/Y side Output Impedance		See Figure 2	38	45	53	35	55	Ω
I_I	Input leakage current (A5-A7 DIR, HD)		V_{CC} = 3.6V; V_O = V_{CC} or GND; Not for I/O pins			±1.0		±5.0	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins		V_{CC} = 3.6V;V_I = 5.5V or GND		± 0.1	± 15			µA
I_{OFF}	B/Y Side Power-off leakage current		V_{CC} = 0.0V; V_O = 0 to 5.5V			±10		±100	µA
I_{OZH}	3-State output High current Yn		V_{CC} = 3.6V; V_O = V_{CC}; V_I = V_{IL} or V_{IH}			5		20	µA
I_{OZL}	3-State output Low current Yn		V_{CC} = 3.6V; V_O = GND; V_I = V_{IL} or V_{IH}			–5		–20	µA
$I_{IH}+I_{OZH}$	current (A1 – A4, Bn)		V_{CC} = 3.6V; $V_{I/O}$ = V_{CC}			5		25	µA
$I_{IL}+I_{OZL}$	current (A1 – A4, Bn)		V_{CC} = 3.6V; $V_{I/O}$ = GND			–5		–25	µA
I_{CC}	Quiescent Supply Current		V_{CC} = 3.6V; I_O = 0; V_I = GND or V_{CC}		5	10		50	µA

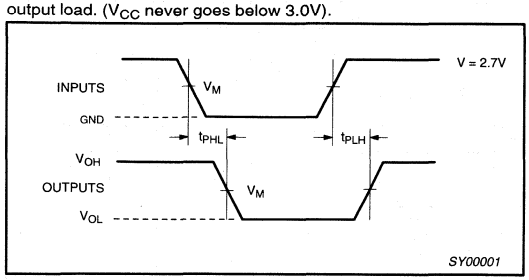
AC CHARACTERISTICS

GND = 0V, t_R = t_F = 3.0ns, C_L = 50pF, R_L = 500Ω

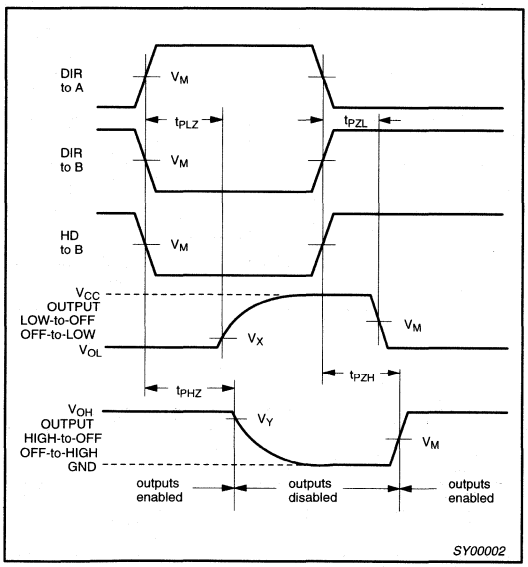
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = 25°C V_{CC} = 3.3V			T_{amb} = 0 to + 70°C V_{CC} = Min to Max		
			MIN	TYP	MAX	MIN	MAX	
SR	B-Side Slew Rate	4	0.05	0.2	0.35	0.05	0.4	V/ns
t_{PLH} t_{PHL}	Propagation delay A toY or A to B	5	6.0 6.0	12.6 12.4	18.0 18.0	5.0 5.0	19.5 20.0	ns
t_{PLH} t_{PHL}	Propagation delay B to A	1	1.5 1.5	5.5 5.6	7.9 7.6	1.5 1.5	9.5 9.0	ns
t_{PZH} t_{PHZ}	Output enable/disable time to/from High level HD to Y or HD to B	2	4.0 2.0	12.0 6.5	16.0 9.1	4.0 2.0	20.0 11.0	ns
t_{PZL} t_{PLZ}	Output enable/disable time to/from Low level A to Y or A to B	2	5.0 1.5	12.7 5.0	16.3 7.1	5.0 1.5	20.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time from DIR to B	2	8.0 8.0	12.3 12.7	18.0 18.0	4.0 4.0	20.0 20.0	ns
t_{PHZ} t_{PLZ}	Output disable time from DIR to B	2	5.0 6.0	8.9 9.1	12.5 12.0	2.0 2.0	14.5 14.0	ns
t_{PZH} t_{PZL}	Output enable time from DIR to A	2	3.5 4.0	6.9 8.6	13.0 14.0	3.0 3.0	14.5 16.0	ns
t_{PHZ} t_{PLZ}	Output disable from DIR to A	2	2.5 2.5	3.7 3.7	5.5 5.0	2.0 2.0	6.0 5.5	ns

AC WAVEFORMS

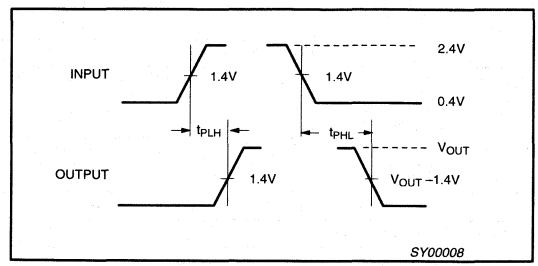
V_M = 1.5V
$V_X = V_{OL} \pm 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load. (V_{CC} never goes below 3.0V).



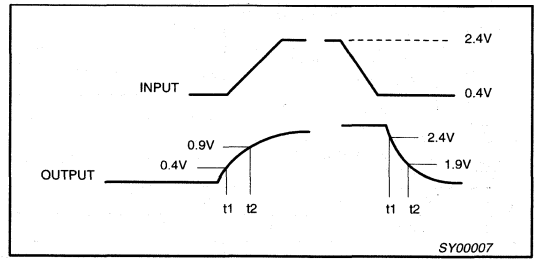
Waveform 1. Input Bn to output An propagation delays



Waveform 2. 3-State enable and disable times



Waveform 3. Voltage Waveforms Propagation Delay Times (A To B) Measured at Output Pin



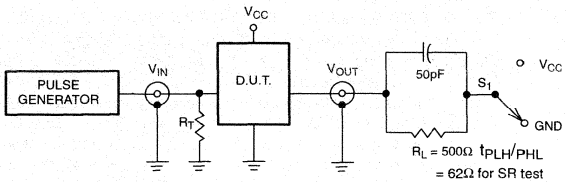
Waveform 4. Slew Rate Waveforms Voltage Waveforms

(Input pulse rise and fall time are 3ns, 150ns < pulse width < 10 µs, for both a Low to High and a High to Low transition.)

Slew Rate measured between 0.4V and 0.9V - rising.

Slew Rate measured between 2.4V and 1.9V - falling.

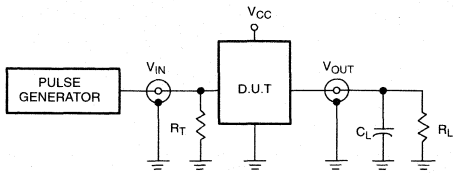
Slew Rate measured at TP1.



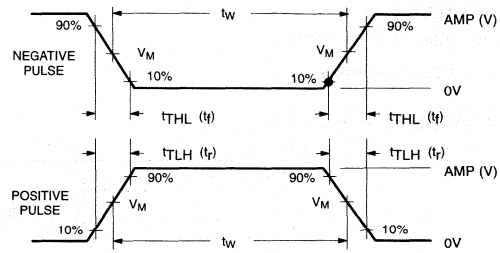
Test Circuit for B_n or Y_n Outputs

SWITCH POSITION
Bn or Yn Outputs

TEST	SWITCH
t_{PLH} t_{PHL}	GND V_{CC}



Test Circuit for A_n Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

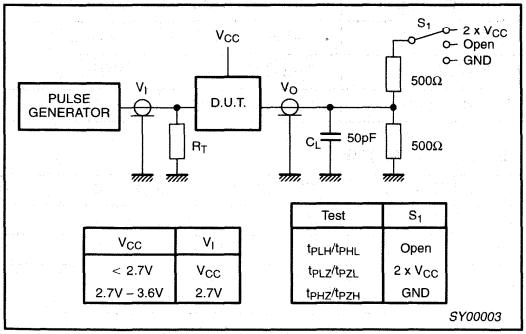
R_L = Load resistor; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_r	t_f
74LVC	3.0V	1MHz	500ns	3ns	3ns

SY00004

Waveform 5.



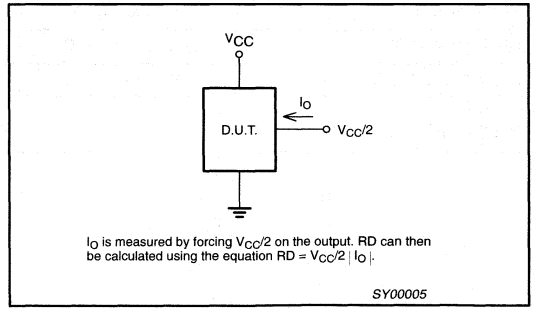
VCC	VI
< 2.7V	VCC
2.7V – 3.6V	2.7V

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x VCC
t_{PHZ}/t_{PZH}	GND

SY00003

Figure 1. Load Circuitry for Bn to An Switching Times

TEST CIRCUIT



I_O is measured by forcing $V_{CC}/2$ on the output. RD can then be calculated using the equation $RD = V_{CC}/2 \mid I_O \mid$.

SY00005

Figure 2. Output Impedance RD

Octal registered tranceiver with 5-volt tolerant inputs/ouputs (3-State)

74LVC2952A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with the JEDEC standard no. 8-1 A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Flow-through pin-out architecture
- 3-State outputs
- Direct interface with TTL levels
- Integrated 30Ω damping resistor

DESCRIPTION

The 74LVC2952A is a low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. The 74LVC2952A is an octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CPnn) provided that the clock enable ($\overline{CE}_{nn}$) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the output enable input ($\overline{OE}_{nn}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs. The 74LVC2952A is identical to the 74LVC2953A but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP_{nn} to A_n, B_n	C_L = 50 pF; V_{CC} = 3.3 V	4.3	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3V[3]	31	pF

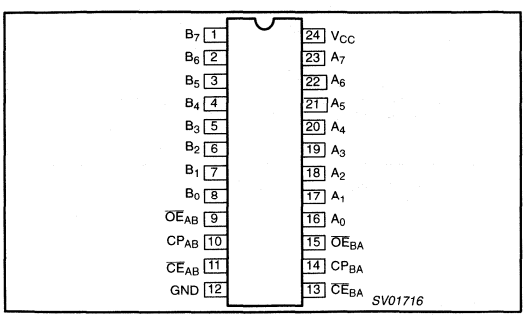
NOTE:

3 C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +125°C	74LVC2952A D	74LVC2952A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +125°C	74LVC2952A DB	74LVC2952A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +125°C	74LVC2952A PW	74LVC2952APW DH	SOT355-1

PIN CONFIGURATION

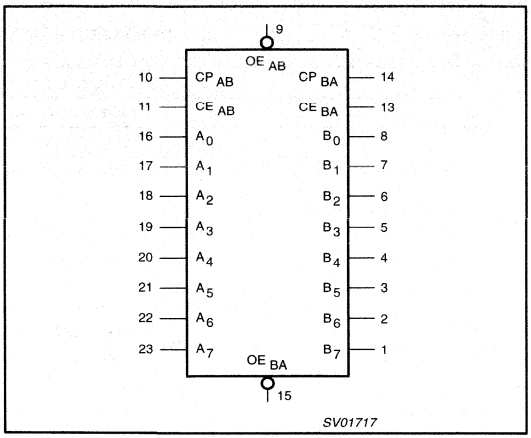


PIN DESCRIPTION

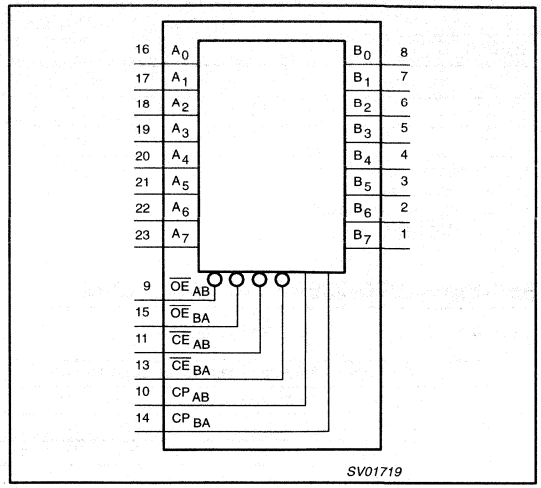
PIN NUMBER	SYMBOL	FUNCTION
8, 7, 6, 5, 4, 3, 2, 1,	B_0 to B_7	B data inputs/outputs
12	GND	Ground (0 V)
9, 15	$\overline{OE}_{AB}$,$\overline{OE}_{BA}$	Output enable inputs (active LOW)
10, 14	CP_{AB}, CP_{BA}	Clock inputs
11, 13,	$\overline{CE}_{AB}$, $\overline{CE}_{BA}$	Clock enable inputs
16, 17, 18, 19, 20, 21, 22, 23	A_0 to A_7	A data inputs/outputs
24	V_{CC}	Positive supply voltage

Octal registered tranceiver with 5-volt tolerant inputs/ouputs (3-State) 74LVC2952A

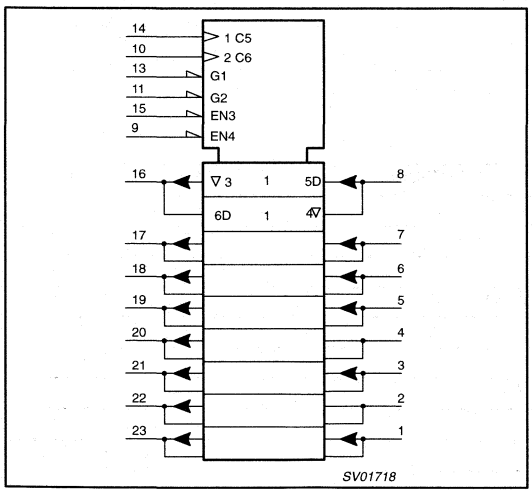
LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



LOGIC SYMBOL



FUNCTION TABLE for register A_n or B_n

INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CP_{nn}	$\overline{CE}_{nn}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	A_n or B_n OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	Enable outputs

Z = high impedance OFF-state
↑ = Low-to-High transition
NC = no change

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC input voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	–0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND; Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V			±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTES:

1 All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP	MAX	MIN	TYP	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay CP_{BA}, CP_{AB} to A_n, B_n	Figures 1, 4	1.5	4.1	7.6	1.5	4.4	8.6	16	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$, to A_n, B_n	Figures 3, 4	1.5	3.9	7.6	1.5	4.7	8.6	16	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$, $\overline{OE}_{AB}$, to A_n, B_n	Figures 3, 4	1.5	3.4	6.6	1.5	3.8	7.6	8	ns
t_w	CP_{AB}, CP_{BA} pulse width, HIGH or LOW	Figure 1	3.0	1.5	–	3.0	1.5	–	–	ns
t_{su}	Set-up time HIGH or LOW A_n, B_n to CP_{AB}, CP_{BA}	Figure 2	2.0	–0.5	–	2.0	–	–	–	ns
t_{su}	Set-up time, HIGH or LOW $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	Figure 2	2.0	0.5	–	2.0	–	–	–	ns
t_h	Hold time A_n, B_n to CP_{AB}, CP_{BA}	Figure 2	1.5	0.6	–	1.5	–	–	–	ns
t_h	Hold time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to CP_{AB}, CP_{BA}	Figure 2	1.5	0	–	1.5	–	–	–	ns
f_{max}	Maximum clock pulse frequency	Figure 2	100	150	–	80	–	–	–	MHz

NOTE:

These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 0.6 V at V_{CC} = 1.2 V
V_M = 1.0 V at V_{CC} = 2.0 V
V_M = 1.5 V at V_{CC} = 3.0 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-State output load.

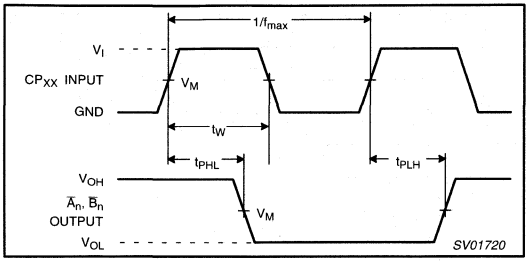


Figure 1. Clock input (CP_{BA}, CP_{AB}) to output ($\overline{B}_n$, $\overline{A}_n$) propagation delays, the clock pulse width and the maximum clock frequency.

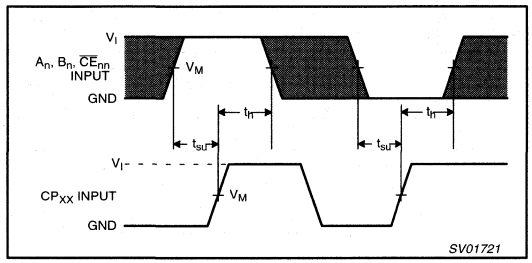


Figure 2. Set-up and hold times for the A_n, B_n and $\overline{CE}_{nn}$ inputs.

NOTE:
The shaded areas indicate when the input is permitted to change for predictable output performance

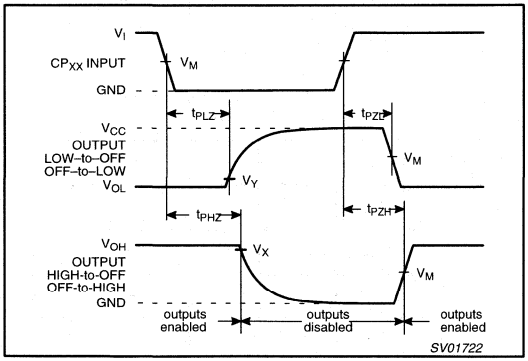
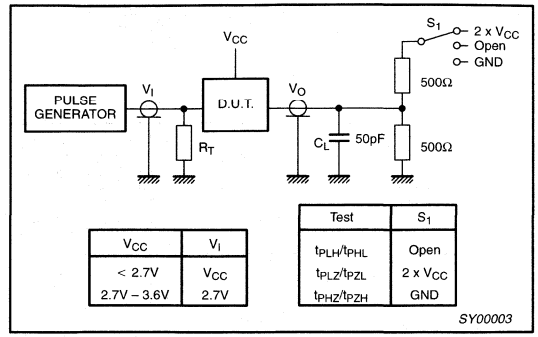


Figure 3. 3-State enable and disable times.

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 4. Load circuitry for switching times.

Octal dual supply translating transceiver (3-State) 74LVC4245A

FEATURES

- Wide supply voltage range
  3 Volt port: 1.5 to 3.6 V
  5 Volt port: 1.5 to 5.5 V
- In accordance with JEDEC standard no. 8-1A
- Control inputs accept voltages up to 5.5 V
- CMOS lower power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC4245A is a high-performance, low-power, low-voltage, Si-gate CMOS device and is superior to most advanced CMOS compatible TTL families.

The 74LVC4245A is an octal dual supply translating transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V bus and 5 V bus in a mixed 3 V/5 V supply environment.

The 74LVC4245A features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. ($\overline{OE}$) controls the outputs so that the buses are effectively isolated.

In suspend mode, when V_{CCA} is zero, there will be no current flow from one supply to the other supply. The A-outputs must be set 3-State and the voltage on the A bus must be smaller than V_{diode} (typ. 0.7 V). $V_{CCA} \geq V_{CCB}$ (except in suspend mode).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nB nB to nA	C_L = 50 pF; V_{CCA} = 5.0 V V_{CCB} = 3.3 V	 4.0 4.0	ns
$C_{I/O}$	Input/output capacitance		10	pF
C_{PDA}	A port nA to nB A port nB to NA	V_I = GND to V_{CC}[1]	7.8 27.9	pF
C_{PDB}	B port nA to nB B port nB to NA		26 10.4	

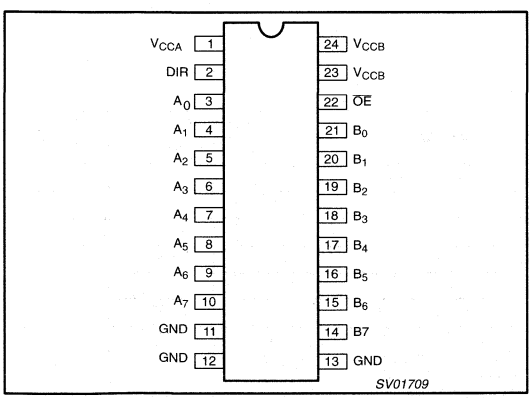
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +125°C	74LVC4245A D	74LVC4245A D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +125°C	74LVC4245A DB	74LVC4245A DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +125°C	74LVC4245A PW	74LVC4245A DH	SOT355-1

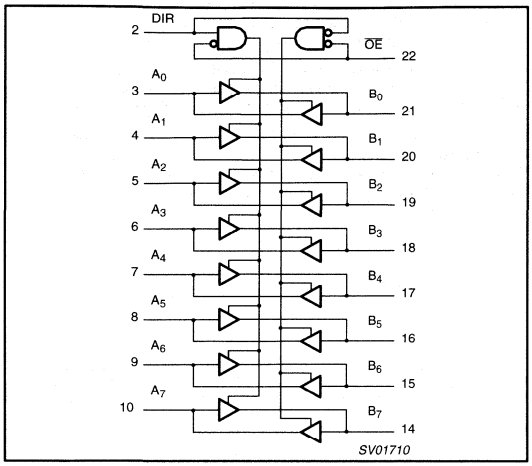
PIN CONFIGURATION



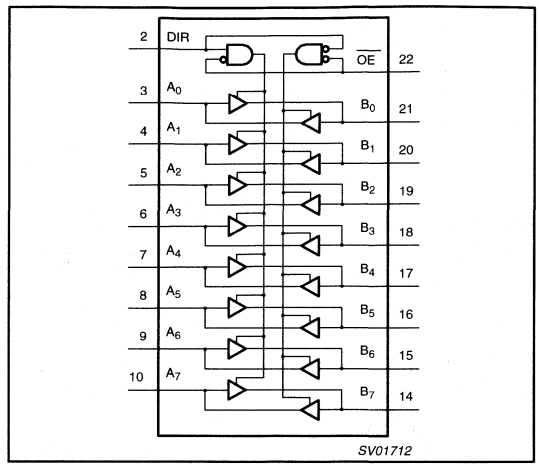
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	V_{CCA}	Positive supply voltage (5 V bus)
2	DIR	Direction control
2, 4, 5, 6, 7, 8, 9, 10	A_0 to A_7	Data inputs/outputs
11, 12, 13	GND	Ground (0 V)
14, 15, 16, 17, 18, 19, 20, 21	B_7 to B_0	Data inputs/outputs
22	$\overline{OE}$	Output enable input (active LOW)
23, 24	V_{CCB}	Positive supply voltage (3 V bus)

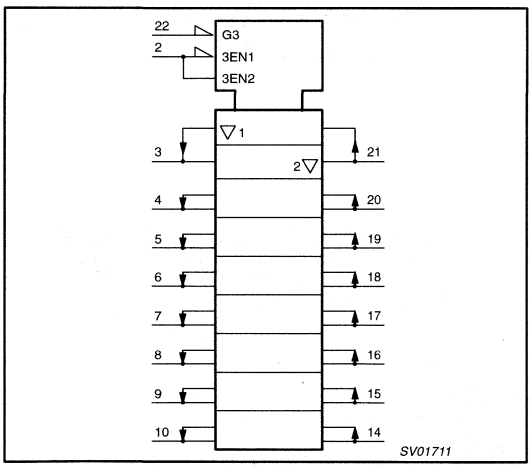
LOGIC SYMBOL



FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUTS	
$\overline{OE}$	DIR	A_n	B_N
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CCA}	DC supply voltage 5V port	$V_{CCA} \geq V_{CCB}$; Waveform 4	1.5	5.5	V
V_{CCB}	DC supply voltage 3V port	$V_{CCA} \geq V_{CCB}$; Waveform 4	1.5	3.6	V
V_I	DC input voltage range (control inputs)		0	5.5	V
$V_{I/O}$	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC input voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CCB} = 2.7 to 3.0V V_{CCB} = 3.0 to 3.6V V_{CCA} = 3.0 to 4.5V V_{CCA} = 4.5 to 5.5V	0 0 0 0	20 10 20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CCA}	DC supply voltage 5V port		−0.5 to +6.5	V
V_{CCB}	DC supply voltage 3V port		−0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +6.5	V
$V_{I/O}$	DC output voltage; output HIGH or LOW	Note 2	−0.5 to V_{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	−0.5 to 6.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−60 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage (3V port)	$V_{CCA/B}$ = 2.7 to 3.6V	2.0			V
	HIGH level Input voltage (5V port)	$V_{CCA/B}$ = 4.5 to 5.5V	2.0			V
V_{IL}	LOW level Input voltage (3V port)	$V_{CCA/B}$ = 2.7 to 3.6V			0.8	V
	LOW level Input voltage (5V port)	$V_{CCA/B}$ = 4.5 to 5.5V			0.8	V
V_{OH}	HIGH level output voltage (3V port)	$V_{CCA/B}$ = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		$V_{CCA/B}$ = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100mA	V_{CC} – 0.2	V_{CC}		
		$V_{CCA/B}$ = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24µA	V_{CC} – 1.0			
	HIGH level output voltage (5V port)	$V_{CCA/B}$ = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		$V_{CCA/B}$ = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		$V_{CCA/B}$ = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage (3V port)	$V_{CCA/B}$ = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		$V_{CCA/B}$ = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100mA			0.20	
		$V_{CCA/B}$ = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24µA			0.55	
	LOW level output voltage (5V port)	$V_{CCA/B}$ = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		$V_{CCA/B}$ = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100mA			0.20	
		$V_{CCA/B}$ = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 24µA			0.55	
I_I	Input leakage current (control inputs)	$V_{CCA/B}$ = 3.6V; V_I = 5.5V or GND; Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins (3V port)	$V_{CCA/B}$ = 3.6V; $V_I = V_{CC}$ or GND		±0.1	±15	µA
	Input current for common I/O pins (5V port)	$V_{CCA/B}$ = 5.5V; $V_I = V_{CC}$ or GND		±0.1	±15	µA
I_{OZ}	3-State output OFF-state current (3V port)	$V_{CCA/B}$ = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	±5	µA
	3-State output OFF-state current (5V port)	$V_{CCA/B}$ = 5.5V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	±5	µA
I_{CC}	Quiescent supply current (3V port)	$V_{CCA/B}$ = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
	Quiescent supply current (5V port)	$V_{CCA/B}$ = 5.5V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin (3V port)	$V_{CCA/B}$ = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA
	Additional quiescent supply current per input pin (5V port)	$V_{CCA/B}$ = 4.5V to 5.5V; $V_I = V_{CC}$ –2.1V; I_O = 0		5	500	µA

NOTES:

1. All typical values are measured at V_{CCA} = 5.0V, V_{CCB} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS									UNIT
			V_{CCA} = 5 V ± 0.5 V			V_{CCB} = 3.3 V ± 0.3 V			V_{CCB} = 2.7 V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n	Figures 1, 3	1.5	4.5	7.0	1.5	4.0	6.5*	1.5	4.5	7.0	ns
			1.5	4.0*	6.5							
t_{PHL}/t_{PLH}	Propagation delay B_n to A_n	Figures 1, 3	1.5	4.5	7.0	1.5	4.0	6.5*	1.5	4.5*	7.0	ns
			1.5	4.0*	6.5							
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to A_n	Figures 2, 3	1.5	7.0	11.0	1.5	6.2	10	1.5	7.0	11.0	ns
			1.5	6.2*	10							
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to B_n	Figures 2, 3	1.5	5.7	8.7	1.5	5.0	8.1	1.5	5.7	8.7	ns
			1.5	5.0	8.1							
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n	Figures 2, 3	1.5	5.7	8.0	1.5	5.3*	7.5	1.5	5.7	8.0	ns
			1.5	5.3*	7.5							
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to B_n	Figures 2, 3	1.5	6.2	8.5	1.5	5.8	7.8	1.5	6.2	8.5	ns
			1.5	5.8*	7.8							

NOTE:
All typical values are measured at T_{amb} = 25°C.
* Typical values are measured at V_{CCA} = 5.0 V and V_{CCB} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at 2.7 V ≤ V_{CC} ≤ 3.6 V
$V_M = 0.5 \times V_{CCA}$ at $V_{CCA} \geq 4.5$ V
$V_x = V_{OL} + 0.3$ V at $V_{CC} \leq 3.6$ V
$V_x = V_{OL} + 0.1 \times (V_{CC} - V_{OL})$ at $V_{CCA} \geq 4.5$ V
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \leq 3.6$ V
$V_Y = V_{OH} - 0.1 \times (V_{OH} - GND)$ at $V_{CCA} \geq 4.5$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

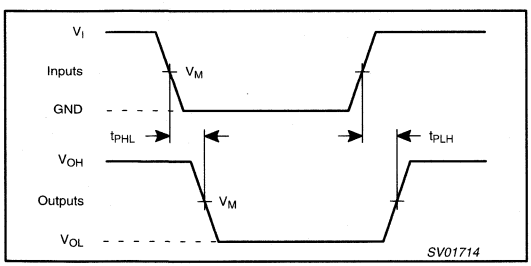


Figure 1. Input (A_n, B_n) to output (B_n, A_n) propagation delays and output transition times.

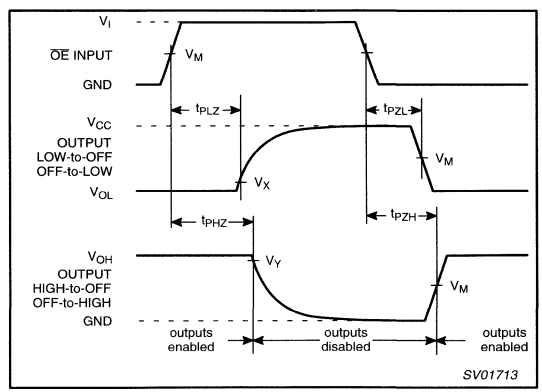


Figure 2. 3-state enable and disable times.

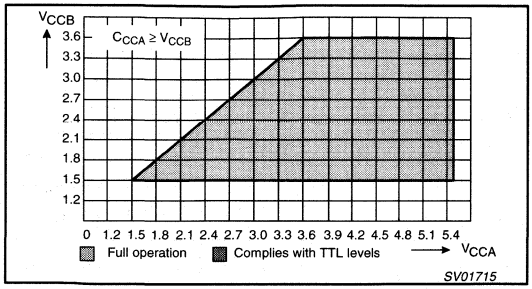


Figure 3. Supply Operation Area.

TEST CIRCUIT

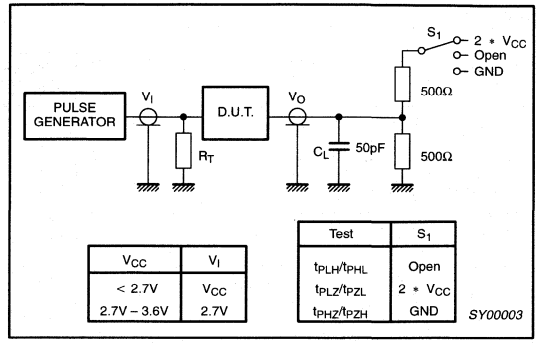


Figure 4. Load circuitry for switching times.

Section 4
Low Voltage CMOS (LVC16)

Advanced Low Voltage CMOS Logic

CONTENTS

16-bit buffer/line driver; inverting (3-State) 74LVC16240A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels

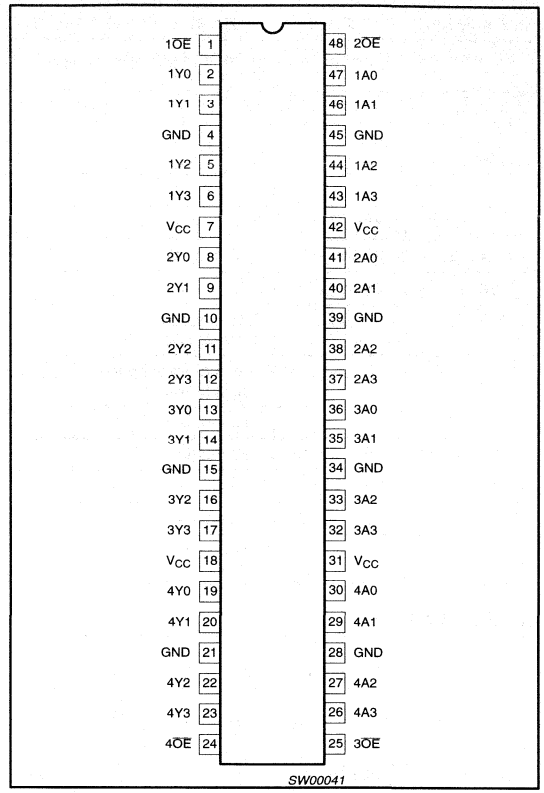
DESCRIPTION

The 74LVC16240A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC16240A is a 16-bit inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The 74LVC16240A is identical to the 74LVC16244A but has inverting outputs.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 50pF V_{CC} = 3.3V	2.7	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_{CC} = 3.3V	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

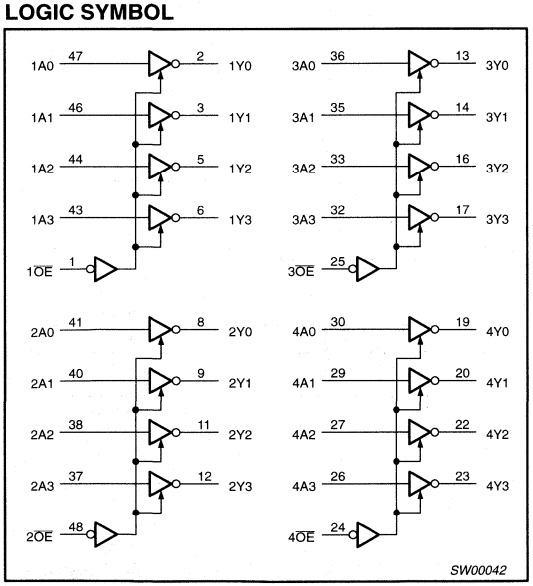
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVC16240A DL	VC16240A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVC16240A DGG	VC16240A DGG	SOT362-1

16-bit buffer/line driver; inverting (3-State) 74LVC16240A

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	Data outputs
19, 20, 22, 23	4Y0 to 4Y3	Data outputs
24	$4\overline{OE}$	Output enable input (active LOW)
25	$3\overline{OE}$	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	Data inputs
41, 40, 38, 37	2A0 to 2A3	Data inputs
47, 46, 44, 43	1A0 to 1A3	Data inputs
48	$2\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

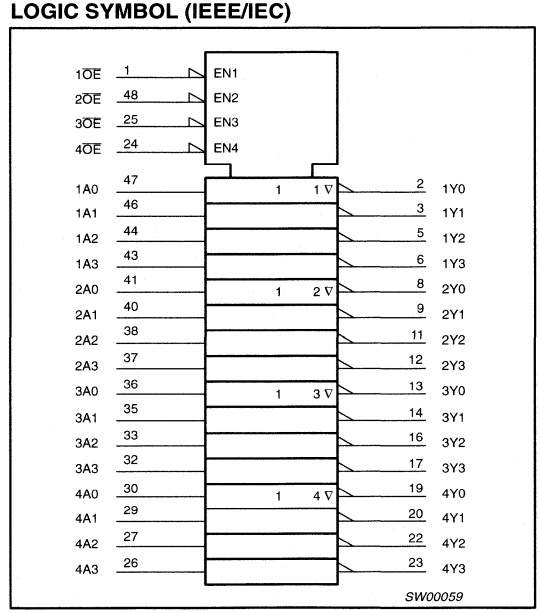


FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
V_O	DC output voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		–0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	Note 2	–0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5	V_{CC} + 0.5	V
V_O	DC output voltage; output 3-State	Note 2	–0.5	6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	Storage temperature range		–65	+150	°C
P_{tot}	Power dissipation per package – SO package – SSOP and TSSOP package	 Above +70°C derate linearly 8mW/K Above +60°C derate linearly 5.5mW/K		 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

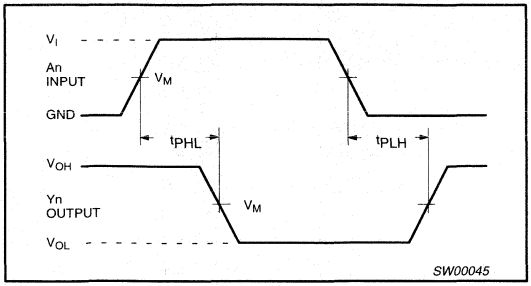
SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	1, 3	1.5	2.8	4.7	1.5	5.7	12	ns
t_{PZH} t_{PZL}	3-State output enable time 1$\overline{OE}$ to 1Yn; 2$\overline{OE}$ to 2Yn	2, 3	1.5	3.5	5.4	1.5	6.4	18	ns
t_{PHZ} t_{PLZ}	3-State output disable time 1$\overline{OE}$ to 1Yn; 2$\overline{OE}$ to 2Yn	2, 3	1.5	3.9	5.1	1.5	6.1	11	ns

NOTE:

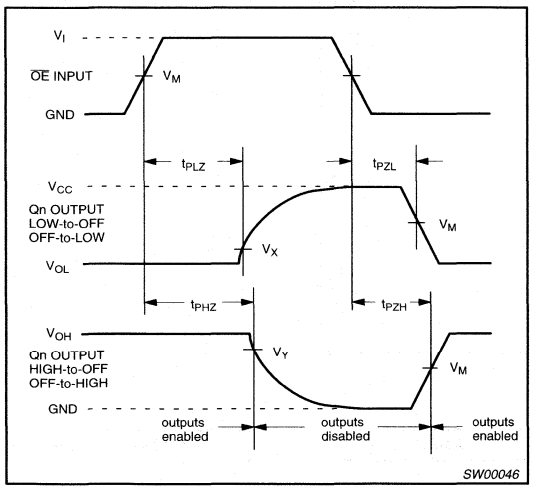
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V

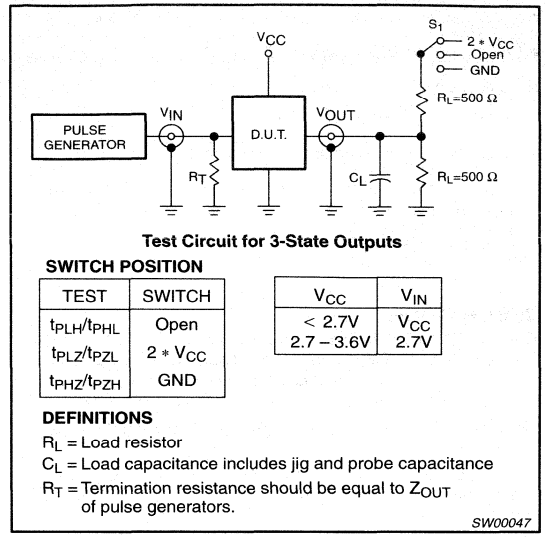


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 3. Load circuitry for switching times

16-bit buffer/line driver (3-State) 74LVC16241A

FEATURES

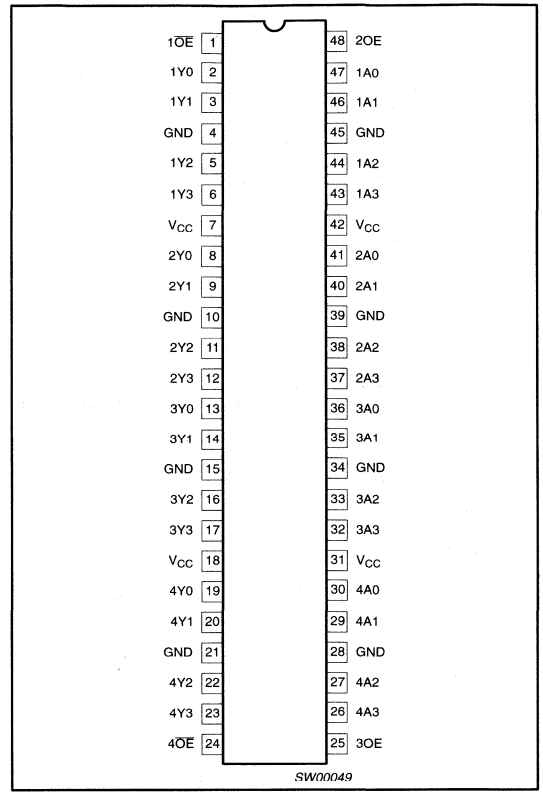
- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels

DESCRIPTION

The 74LVC16241A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC16241A is a 16-bit buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs n$\overline{OE}$ and nOE. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	C_L = 50pF V_{CC} = 3.3V	2.9	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	25	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

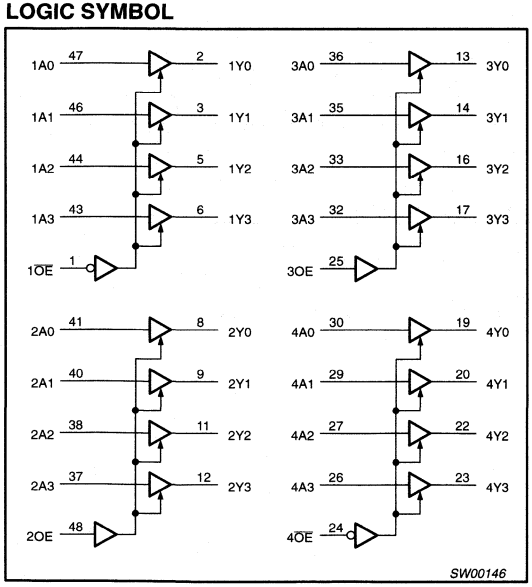
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVC16241A DL	VC16241A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVC16241A DGG	VC16241A DGG	SOT362-1

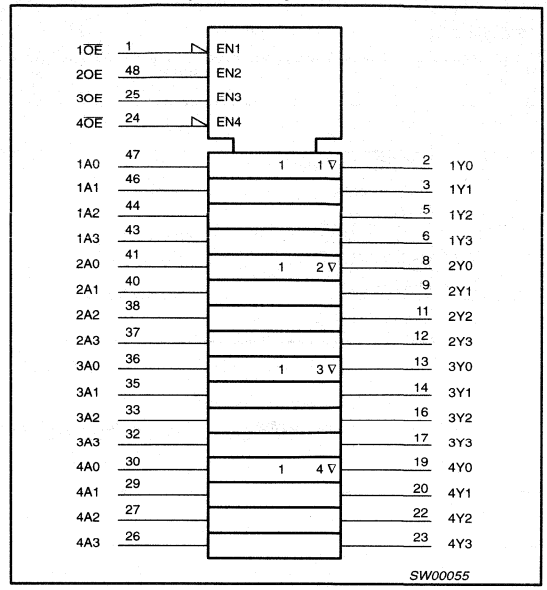
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	Data outputs
19, 20, 22, 23	4Y0 to 4Y3	Data outputs
24	$4\overline{OE}$	Output enable input (active LOW)
25	3OE	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	Data inputs
41, 40, 38, 37	2A0 to 2A3	Data inputs
47, 46, 44, 43	1A0 to 1A3	Data inputs
48	2OE	Output enable input (active LOW)

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLES

INPUTS		OUTPUT
$n\overline{OE}$	1An, 4An	1Yn, 4Yn
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
nOE	2An, 3An	2Yn, 3Yn
H	H	H
H	L	L
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
V_O	DC output voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		–0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	Note 2	–0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5	V_{CC} + 0.5	V
V_O	DC output voltage; output 3-State	Note 2	–0.5	6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	Storage temperature range		–65	+150	°C
P_{tot}	Power dissipation per package – SO package – SSOP and TSSOP package	 Above +70°C derate linearly 8mW/K Above +60°C derate linearly 5.5mW/K		 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

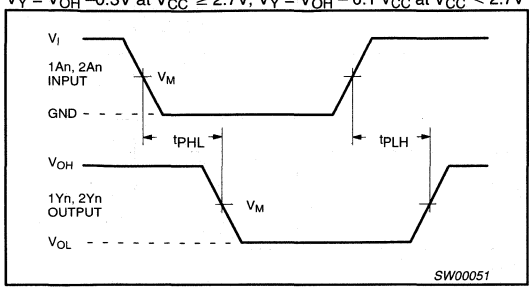
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					LIMITS	UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay nAn to nYn; nAn to nYn	1, 4	1.5	2.9	4.4	1.5	5.4	13	ns
t_{PZH} t_{PZL}	3-State output enable time 1$\overline{OE}$ to 1Yn; 4$\overline{OE}$ to 4Yn	3, 4	1.5	4.4	5.8	1.5	6.8	17	ns
t_{PHZ} t_{PLZ}	3-State output disable time 1$\overline{OE}$ to 1Yn; 4$\overline{OE}$ to 4Yn	3, 4	1.5	4.3	5.8	1.5	6.8	11	ns
t_{PZH} t_{PZL}	3-State output enable time 2OE to 2Yn; 3OE to 3Yn	2, 4	1.5	4.4	5.5	1.5	6.5	19	ns
t_{PHZ} t_{PLZ}	3-State output disable time 2OE to 2Yn; 3OE to 3Yn	2, 4	1.5	4.9	5.4	1.5	6.4	12	ns

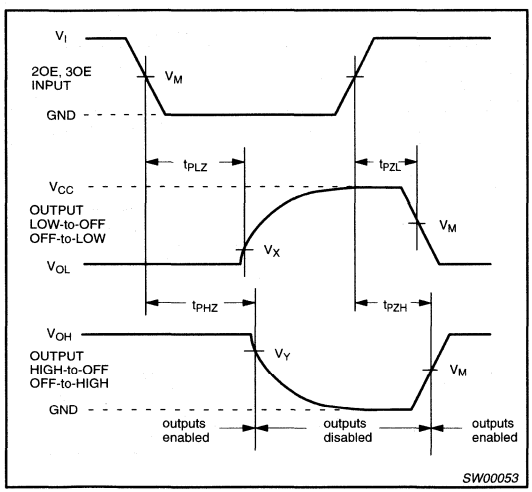
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

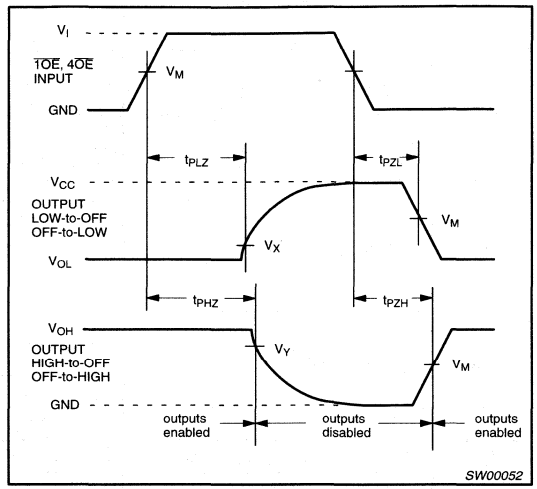
V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V



Waveform 1. Input (nAn) to output (nYn) propagation times

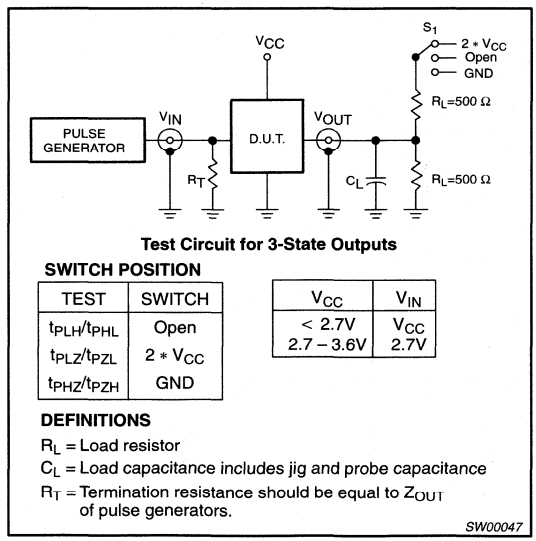


Waveform 2. 3-State enable and disable times for the input (2OE, 3OE)



Waveform 3. 3-State enable and disable times for the input (1$\overline{OE}$, 4$\overline{OE}$)

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Waveform 4. Load circuitry for switching times

16-bit buffer/line driver; 5V input/output tolerant (3-State)

74LVC16244A/ 74LVCH16244A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16244A only)

DESCRIPTION

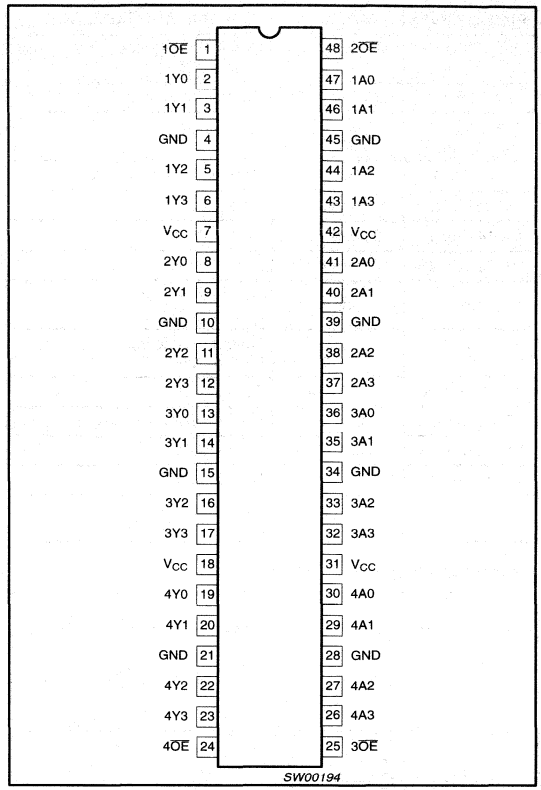
The 74LVC(H)16244A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)16244A is a 16-bit non-inverting buffer/line driver with 3-State outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer.

The 74LVC(H)16244A is identical to the 74LVC16240A but has non-inverting outputs.

The 74LVCH16244A bus hold data inputs eliminates the need for external pull up resistors to hold unused inputs.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVC16244A DL	VC16244A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVC16244A DGG	VC16244A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVCH16244A DL	VCH16244A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVCH16244A DGG	VCH16244A DGG	SOT362-1

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 50pF V_{CC} = 3.3V	3.0	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	25	pF

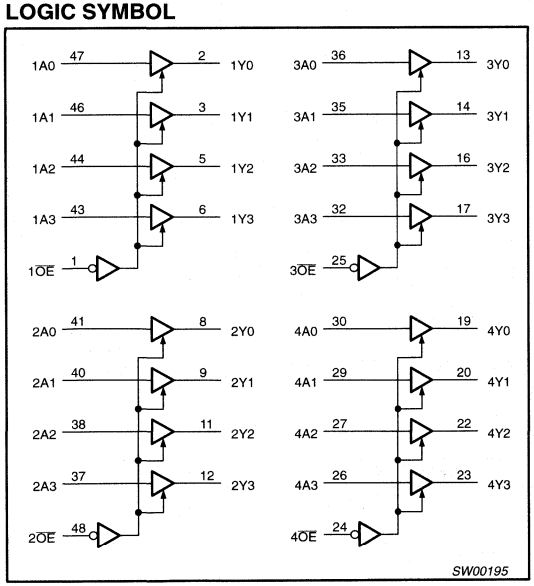
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	Data outputs
19, 20, 22, 23	4Y0 to 4Y3	Data outputs
24	$4\overline{OE}$	Output enable input (active LOW)
25	$3\overline{OE}$	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	Data inputs
41, 40, 38, 37	2A0 to 2A3	Data inputs
47, 46, 44, 43	1A0 to 1A3	Data inputs
48	$2\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

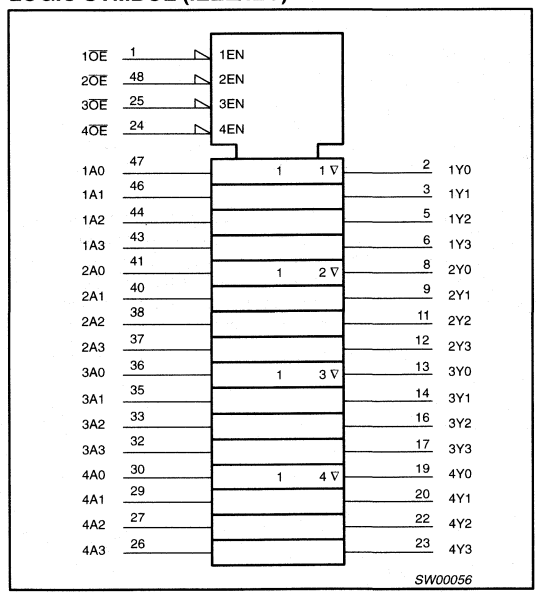


FUNCTION TABLE

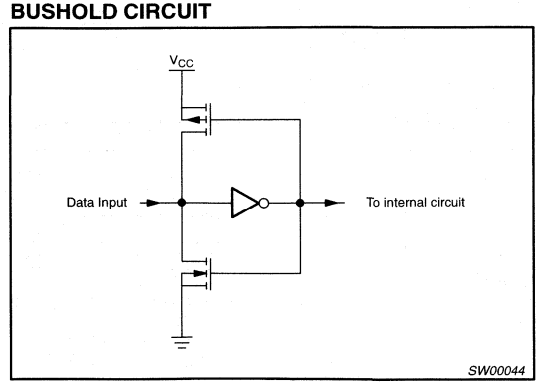
INPUTS		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		–0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	Note 2	–0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5	V_{CC} + 0.5	V
V_O	DC output voltage; output 3-State	Note 2	–0.5	6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	Storage temperature range		–65	+150	°C
P_{tot}	Power dissipation per package – SO package – SSOP and TSSOP package	 Above +70°C derate linearly 8mW/K Above +60°C derate linearly 5.5mW/K		 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
V_O	DC output voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND[6]		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 3.0V; V_I = 0.8V[2, 3, 4]	75			µA
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 3.0V; V_I = 2.0V[2, 3, 4]	−75			µA
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2, 3, 5]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2, 3, 5]	−500			µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.

AC CHARACTERISTICS

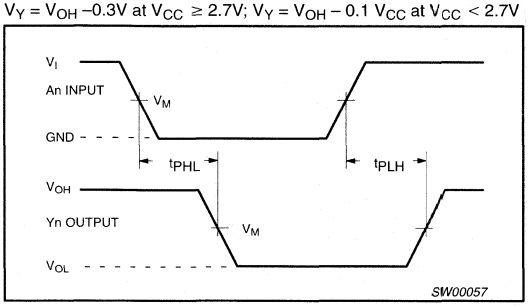
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = −40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	1	1.5	3	4.5	1.5	5.5	11.0	ns
t_{PZH} t_{PZL}	3-State output enable time $1\overline{OE}$ to 1Yn; $2\overline{OE}$ to 2Yn	2, 3	1.5	3.5	5.5	1.5	6.5	15.0	ns
t_{PHZ} t_{PLZ}	3-State output disable time $1\overline{OE}$ to 1Yn; $2\overline{OE}$ to 2Yn	2, 3	1.5	3.7	5.2	1.5	6.2	10.0	ns

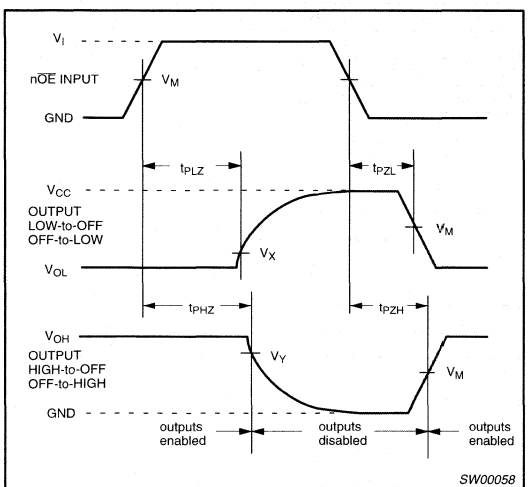
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ −0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ − 0.1 V_{CC} at V_{CC} < 2.7V

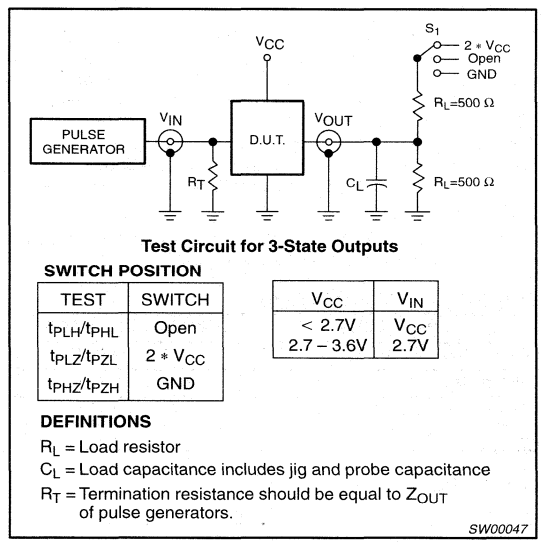


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Waveform 3. Load circuitry for switching times

16-bit buffer/line driver; with 30Ω series termination resistors; 5V input/output tolerant (3-State)

74LVC162244A/ 74LVCH162244A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus Hold on data inputs (74LVCH162244A only)
- Integrated 30Ω termination resistors

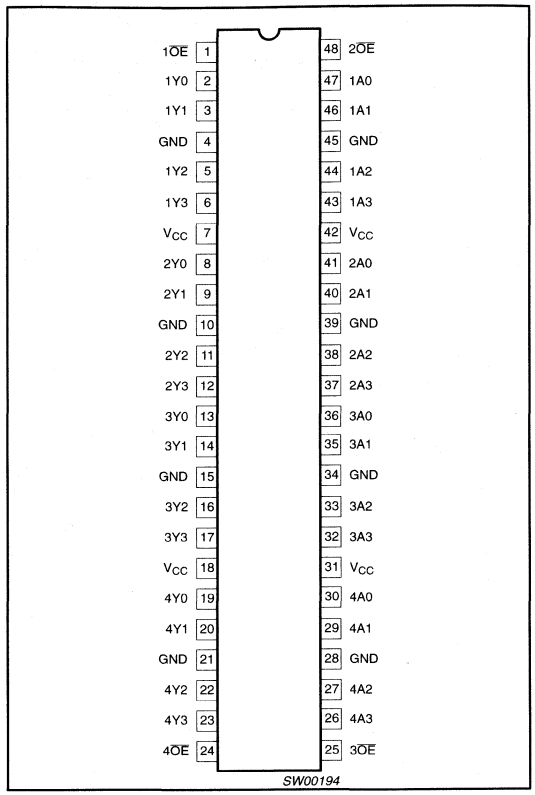
DESCRIPTION

The 74LVC(H)162244A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)162244A is a 16-bit non-inverting buffer/line driver with 3-State outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The 74LVC(H)162244A is designed with 30Ω series termination resistors in both HIGH and LOW output stages to reduce line noise. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer.

The 74LVCH162244A bus hold data inputs eliminates the need for external pull up resistors to hold unused inputs.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	−40°C to +85°C	74LVC162244A DL	VC162244A DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74LVC162244A DGG	VC162244A DGG	SOT362-1
48-Pin Plastic SSOP Type III	−40°C to +85°C	74LVCH162244A DL	VCH162244A DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74LVCH162244A DGG	VCH162244A DGG	SOT362-1

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 50pF V_{CC} = 3.3V	2.9	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	25	pF

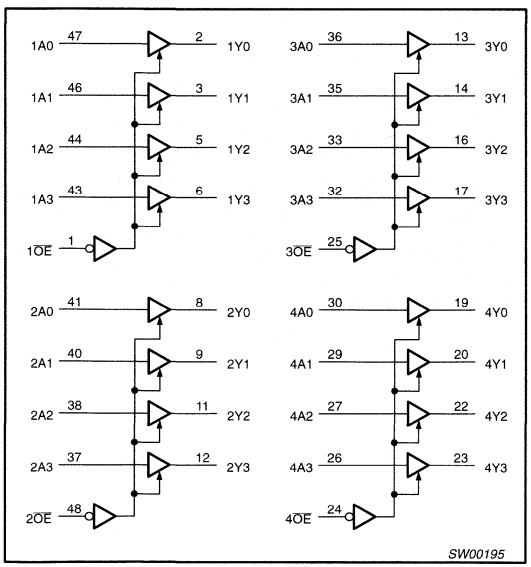
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	Data outputs
19, 20, 22, 23	4Y0 to 4Y3	Data outputs
24	$4\overline{OE}$	Output enable input (active LOW)
25	$3\overline{OE}$	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	Data inputs
41, 40, 38, 37	2A0 to 2A3	Data inputs
47, 46, 44, 43	1A0 to 1A3	Data inputs
48	$2\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

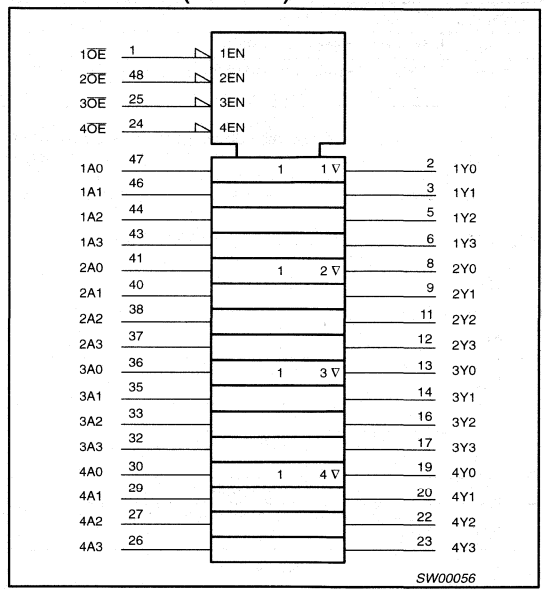


FUNCTION TABLE

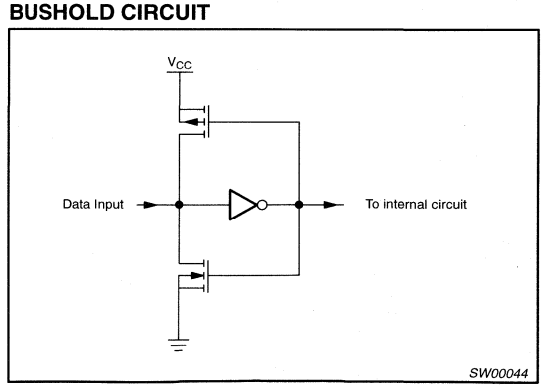
INPUTS		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		−0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−	−50	mA
V_I	DC input voltage	Note 2	−0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	−	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	−0.5	V_{CC} + 0.5	V
V_O	DC output voltage; output 3-State	Note 2	−0.5	6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	−	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		−	±100	mA
T_{stg}	Storage temperature range		−65	+150	°C
P_{tot}	Power dissipation per package – SSOP and TSSOP package	Above +60°C derate linearly 5.5mW/K		500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
V_O	DC output voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	−40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND[6]		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per control pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA
ΔI_{CC}	Additional quiescent supply current per data input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 3.0V; V_I = 0.8V[2, 3, 4]	75			µA
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 3.0V; V_I = 2.0V[2, 3, 4]	–75			µA
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2, 3 5]	450			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2, 3, 5]	–450			µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.

AC CHARACTERISTICS

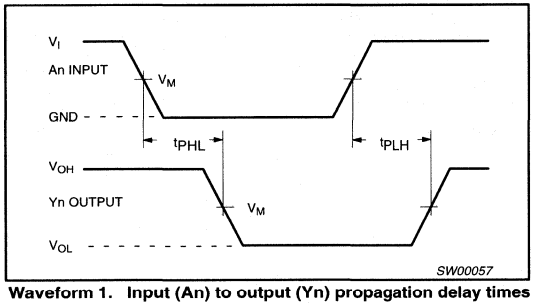
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL} t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	1	1.5	2.9	6.3	1.5	7.3	ns
t_{PZH} t_{PZL}	3-State output enable time $1\overline{OE}$ to 1Yn; $2\overline{OE}$ to 2Yn	2, 3	1.5	3.4	7.1	1.5	8.1	ns
t_{PHZ} t_{PLZ}	3-State output disable time $1\overline{OE}$ to 1Yn; $2\overline{OE}$ to 2Yn	2, 3	1.5	2.8	5.0	1.5	6.0	ns

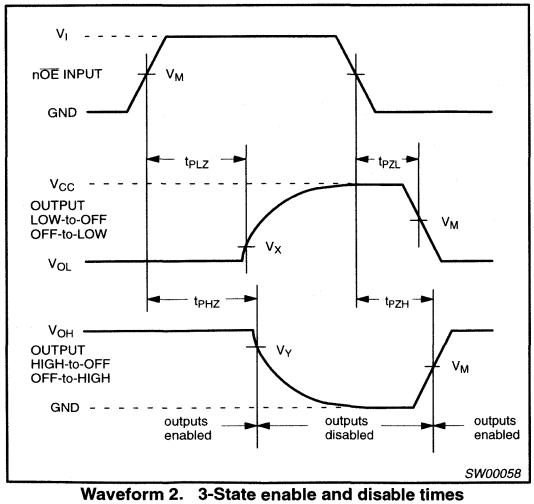
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V

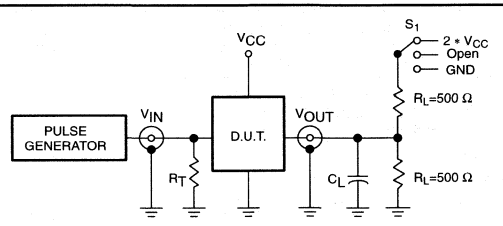


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 3. Load circuitry for switching times

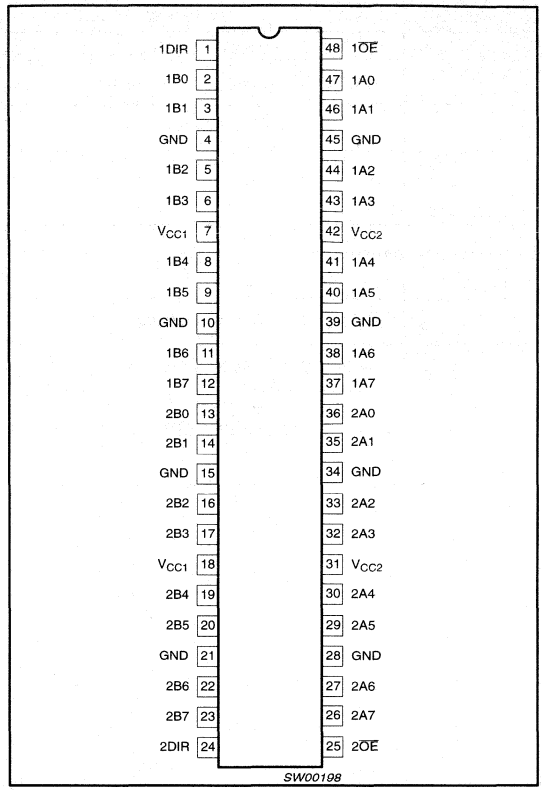
16-bit bus transceiver with direction pin; 5V tolerant (3-State)

74LVC16245A/ 74LVCH16245A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High impedance when V_{CC} = 0
- All data inputs have bus hold (74LVCH16245A only)

PIN CONFIGURATION



DESCRIPTION

The 74LVC(H)16245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)16245A is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74LVC(H)16245A features two output enable (n$\overline{OE}$) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. n$\overline{OE}$ controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVCH16245A bus hold data inputs eliminates the need for extreme pull up resistors to hold unused inputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVC16245A DL	VC16245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVC16245A DGG	VC16245A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVCH16245A DL	VCH16245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVCH16245A DGG	VCH16245A DGG	SOT362-1

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 50pF V_{CC} = 3.3V	3.0	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	30	pF

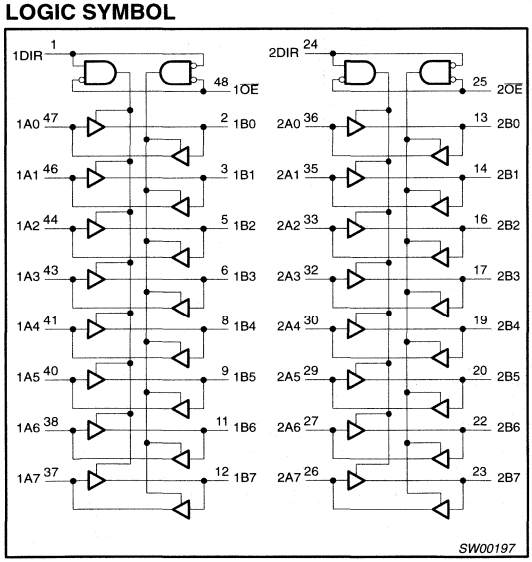
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	Direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	Data inputs/outputs
24	2DIR	Direction control
25	$2\overline{OE}$	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	Data inputs/outputs
48	$1\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

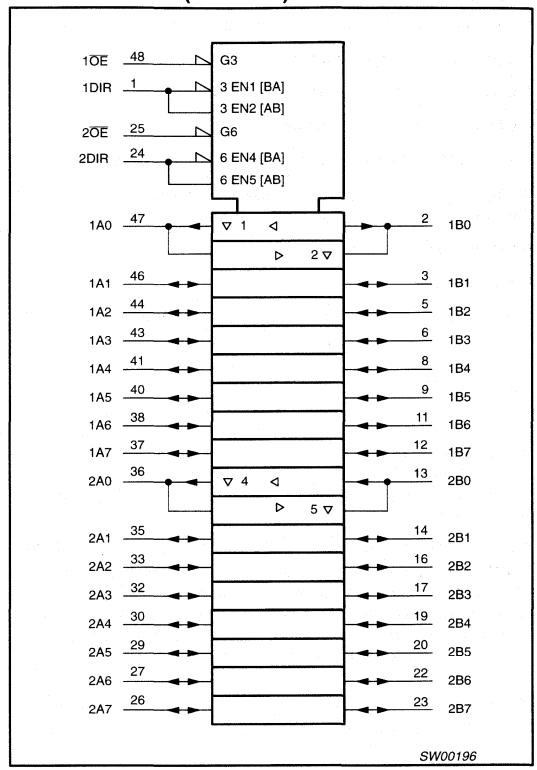


FUNCTION TABLE

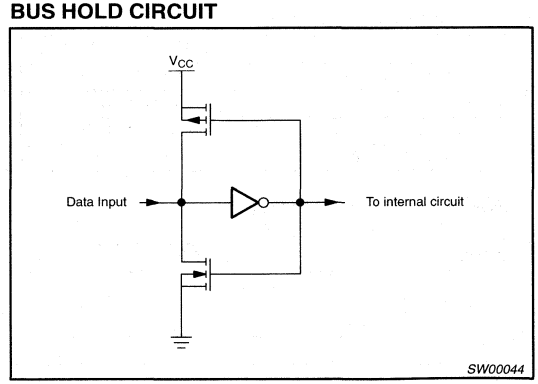
INPUTS		INPUTS/OUTPUT	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
V_O	DC output voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		–0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	Note 2	–0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5	V_{CC} + 0.5	V
V_O	DC output voltage; output 3-State	Note 2	–0.5	6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	Storage temperature range		–65	+150	°C
P_{tot}	Power dissipation per package – SO package – SSOP and TSSOP package	 Above +70°C derate linearly 8mW/K Above +60°C derate linearly 5.5mW/K		 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current[7]	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 3.0V; V_I = 0.8V[2, 3, 4]	75			µA
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 3.0V; V_I = 2.0V[2, 3, 4]	–75			µA
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2, 3, 5]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2, 3, 5]	–500			µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_i exceeds V_{CC} allowing 5.5V on the input terminal.
7. For I/O ports the parameter I_{OZ} includes the input leakage current.

AC CHARACTERISTICS

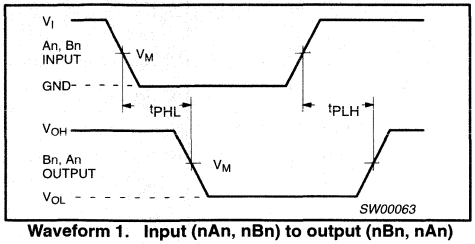
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay nAn to nBn; nBn to nAn	1	1.5	3	4.5	1.5	5.5	13	ns
t_{PZH} t_{PZL}	3-State output enable time $n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn	2, 3	1.5	4	6.1	1.5	7.1	15	ns
t_{PHZ} t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn	2, 3	1.5	4	5.6	1.5	6.6	11	ns

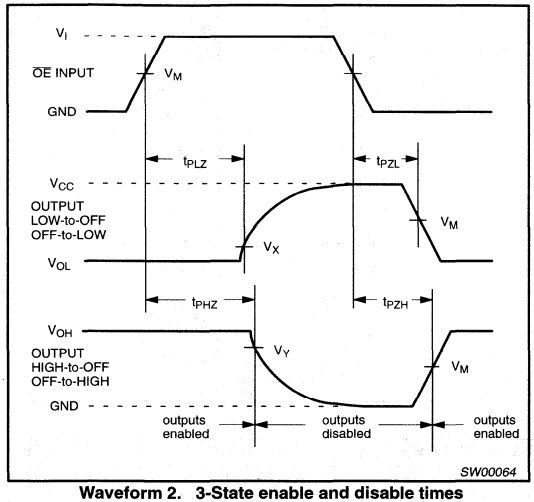
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V

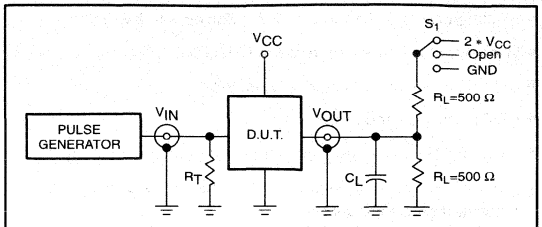


Waveform 1. Input (nAn, nBn) to output (nBn, nAn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 3. Load circuitry for switching times

16-bit bus transceiver with direction pin; 30Ω series termination resistors; 5V Input/Outputs tolerant (3-State)

74LVC162245A/ 74LVCH162245A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on data inputs (74LVCH162245A only)
- Integrated 30Ω termination resistors

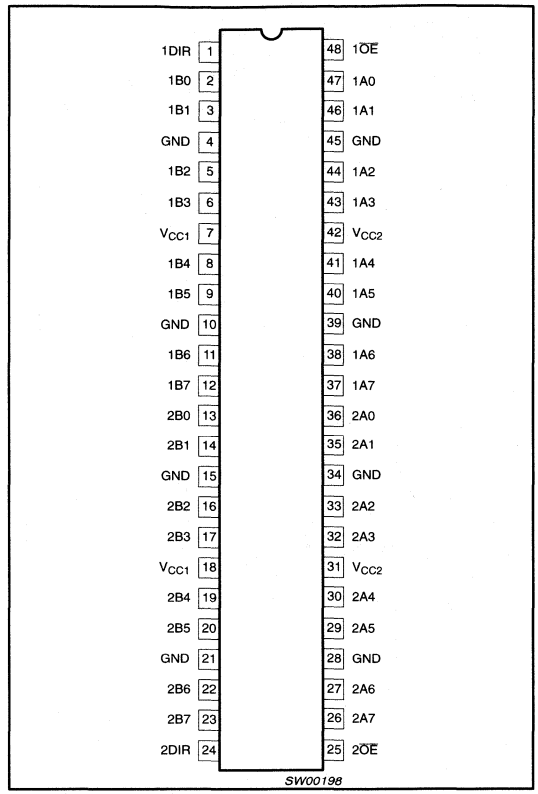
DESCRIPTION

The 74LVC(H)162245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)162245A is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74LVC(H)162245A features two output enable ($n\overline{OE}$) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. $n\overline{OE}$ controls the outputs so that the buses are effectively isolated. The 74LVC(H)162245A is design with 30Ω series termination resistors in both HIGH and LOW output stages to reduce line noise. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVCH162245A bus hold data inputs eliminates the need for extreme pull up resistors to hold unused inputs.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVC162245A DL	VC162245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVC162245A DGG	VC162245A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVCH162245A DL	VCH162245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVCH162245A DGG	VCH162245A DGG	SOT362-1

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	C_L = 50pF V_{CC} = 3.3V	3.3	ns
C_I	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	28	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

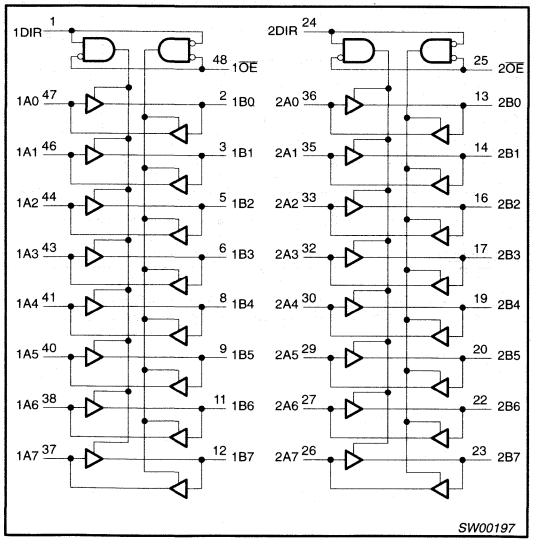
16-bit bus transceiver with direction pin; 30Ω series termination resistors; 5V Input/Outputs tolerant (3-State)

74LVC162245A/ 74LVCH162245A

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	Direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	Data inputs/outputs
24	2DIR	Direction control
25	$2\overline{OE}$	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	Data inputs/outputs
48	$1\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

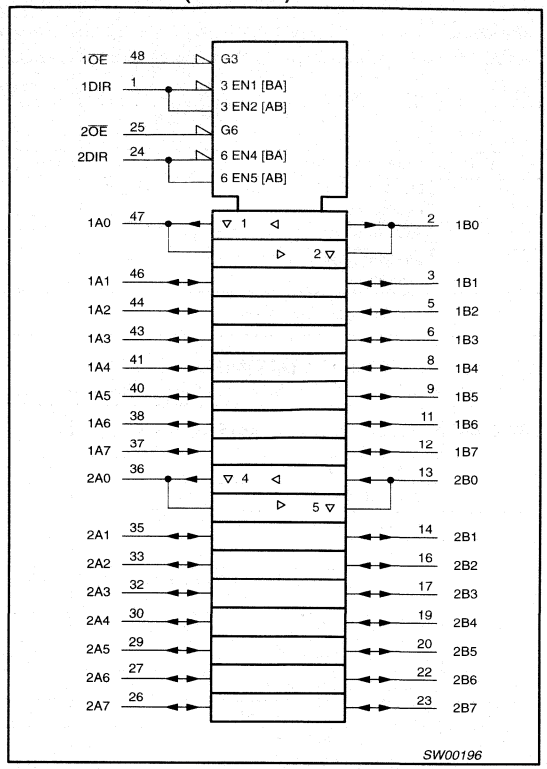


FUNCTION TABLE

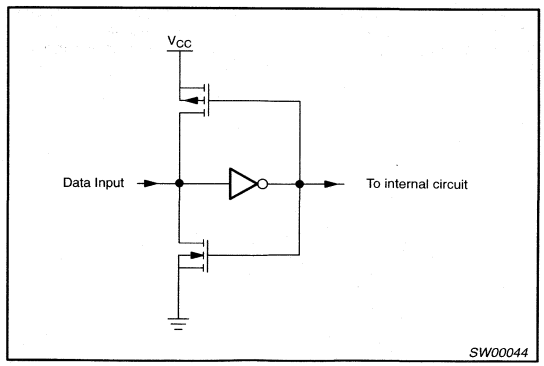
INPUTS		INPUTS/OUTPUT	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
V_O	DC output voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		–0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	Note 2	–0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	–0.5	V_{CC} + 0.5	V
V_O	DC output voltage; output 3-State	Note 2	–0.5	6.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	Storage temperature range		–65	+150	°C
P_{tot}	Power dissipation per package – SSOP and TSSOP package	Above +60°C derate linearly 5.5mW/K		500	

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 6mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND[6]		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current[7]	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per control pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		5	500	µA
ΔI_{CC}	Additional quiescent supply current per data input pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 3.0V; V_I = 0.8V[2, 3, 4]	75			µA
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 3.0V; V_I = 2.0V[2, 3, 4]	–75			µA
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2, 3, 5]	450			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2, 3, 5]	–450			µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_i exceeds V_{CC} allowing 5.5V on the input terminal.
7. For I/O ports the parameter I_{OZ} includes the input leakage current.

AC CHARACTERISTICS

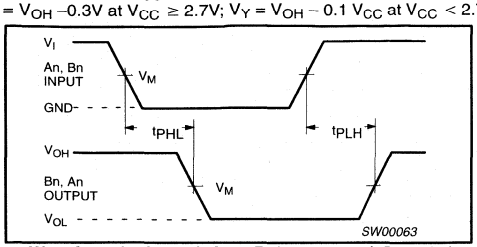
GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL} t_{PLH}	Propagation delay nAn to nBn; nBn to nAn	1	1.5	3.3	5.7	1.5	6.7	ns
t_{PZH} t_{PZL}	3-State output enable time n$\overline{OE}$ to nAn; n$\overline{OE}$ to nBn	2, 3	1.5	4.3	7.5	1.5	8.5	ns
t_{PHZ} t_{PLZ}	3-State output disable time n$\overline{OE}$ to nAn; n$\overline{OE}$ to nBn	2, 3	1.5	4.0	6.5	1.5	7.5	ns

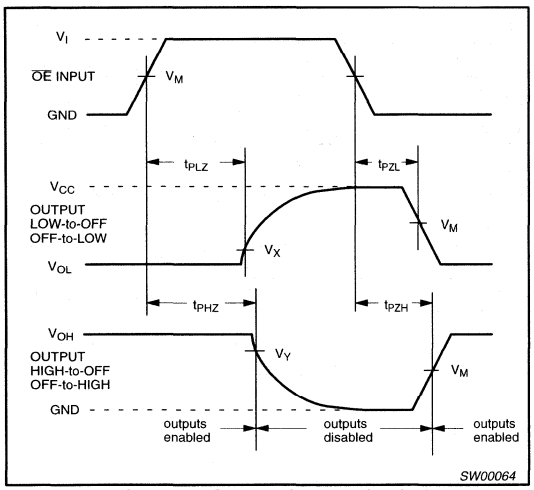
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ −0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ − 0.1 V_{CC} at V_{CC} < 2.7V

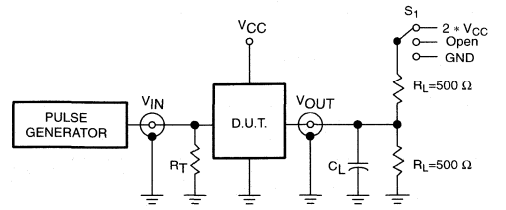


Waveform 1. Input (nAn, nBn) to output (nBn, nAn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 3. Load circuitry for switching times

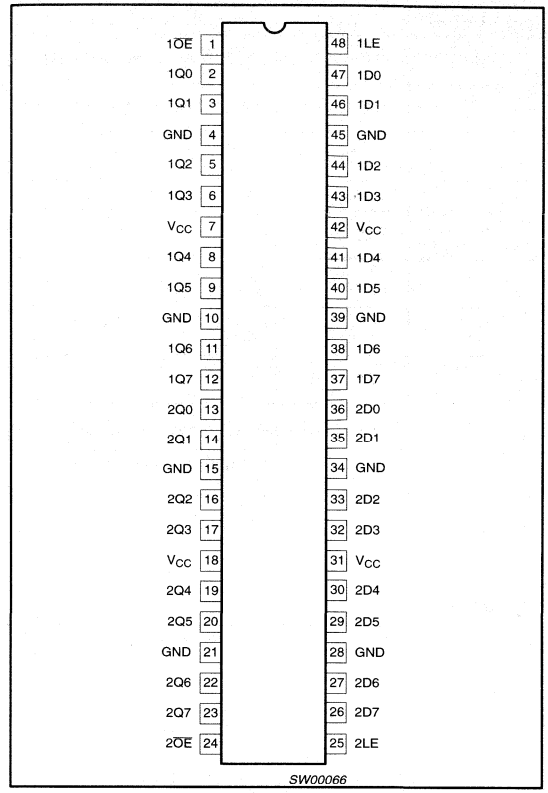
16-bit D-type transparent latch with 5 Volt tolerant inputs/outputs (3-State)

74LVC16373A/ 74LVCH16373A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH167373A only)
- High impedance when $V_{CC} = 0$

PIN CONFIGURATION



DESCRIPTION

The 74LVC(H)16373A is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. One latch enable (LE) input and one output enable ($\overline{OE}$) are provided for each octal. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)16373A consists of 2 sections of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74LVCH16373A bus hold data inputs eliminates the need for external pull up resistors to hold unused inputs.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25°C$; $t_r = t_f \leq 2.5ns$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn LE to Qn	$C_L = 50pF$ $V_{CC} = 3.3V$	3.0 3.4	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	$V_{CC} = 3.3V$	26	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

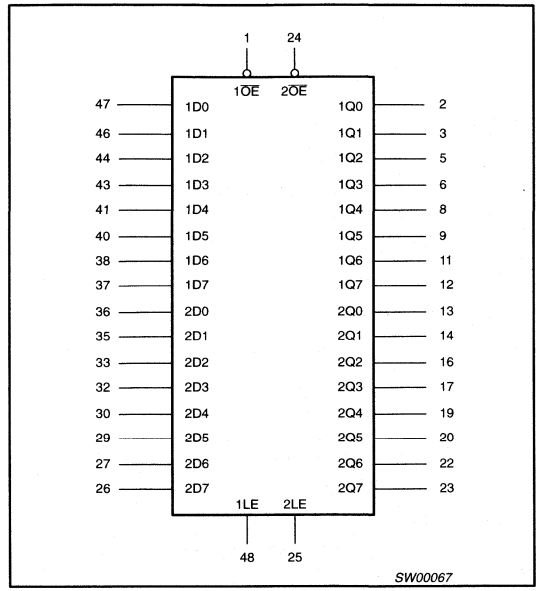
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVC16373A DL	VC16373A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVC16373A DGG	VC16373A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVCH16373A DL	VCH16373A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVCH16373A DGG	VCH16373A DGG	SOT362-1

16-bit D-type transparent latch with 5 Volt tolerant inputs/outputs (3-State)

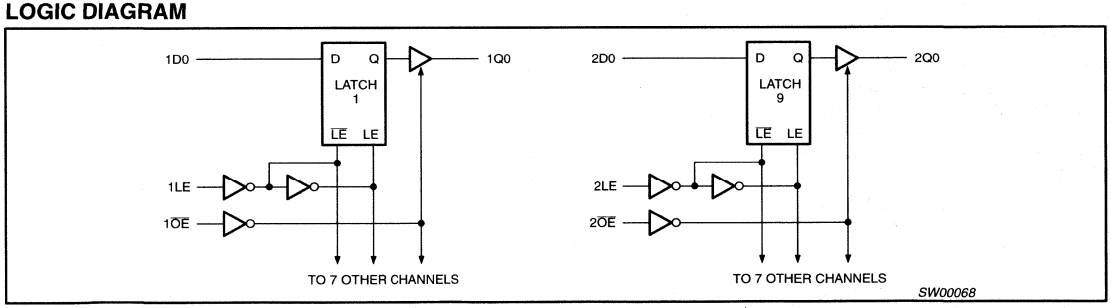
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	Data inputs/outputs
24	$2\overline{OE}$	Output enable input (active LOW)
25	2LE	Latch enable input (active HIGH)
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data inputs
48	1LE	Latch enable input (active HIGH)

LOGIC SYMBOL



LOGIC DIAGRAM

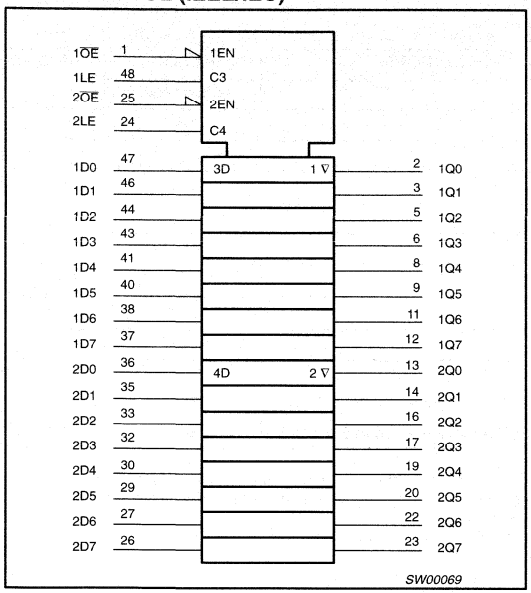


FUNCTION TABLE (per section of eight bits)

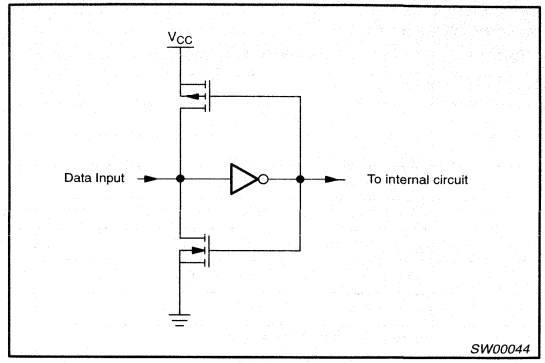
OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	Dn		Q0 to Q7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC input voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	−0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	−0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package			mW
	– plastic mini-pack (SO)	above +70°C derate linearly with 8 mW/K	500	
	– plastic shrink mini-pack (SSOP and TSSOP)	above +60°C derate linearly with 5.5 mW/K	500	

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND[6]		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V			±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 3.0V; V_I = 0.8V[2, 3, 4]	75			µA
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 3.0V; V_I = 2.0V[2, 3, 4]	–75			µA
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2, 3, 5]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2, 3, 5]	–500			µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_i exceeds V_{CC} allowing 5.5V on the input terminal.

AC CHARACTERISTICS

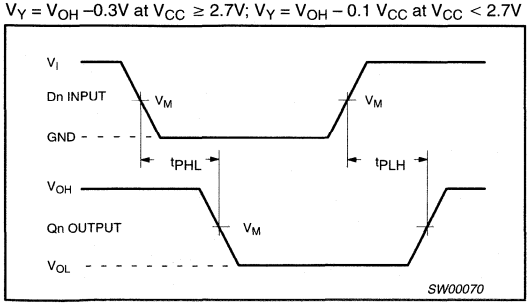
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	TYP	
t_{PHL} t_{PLH}	Propagation delay Dn to Qn	1, 5	1.5	3.0	4.7	1.5	5.7	12	ns
t_{PHL} t_{PLH}	Propagation delay LE to Qn	2, 5	1.5	3.4	4.8	1.5	5.8	14	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Qn	4, 5	1.5	3.5	5.5	1.5	6.5	18	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Qn	4, 5	1.5	3.9	5.4	1.5	6.4	11	ns
t_W	LE pulse width HIGH	2	3	2.0	–	3	–	–	ns
t_{su}	Set-up time Dn to LE	3	1.7	–0.1	–	1.7	–	–	ns
t_h	Hold time Dn to LE	3	1.2	0.1	–	1.2	–	–	ns

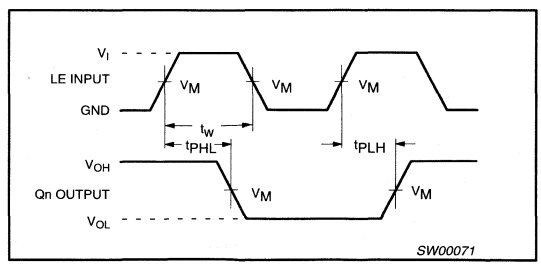
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V



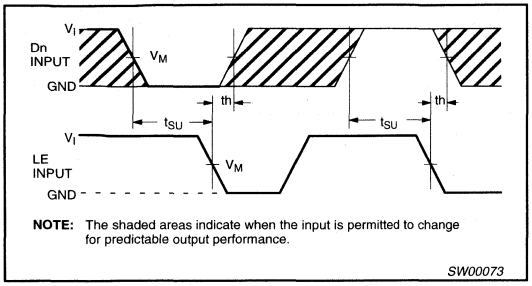
Waveform 1. Input (Dn) to output (Qn) propagation delays



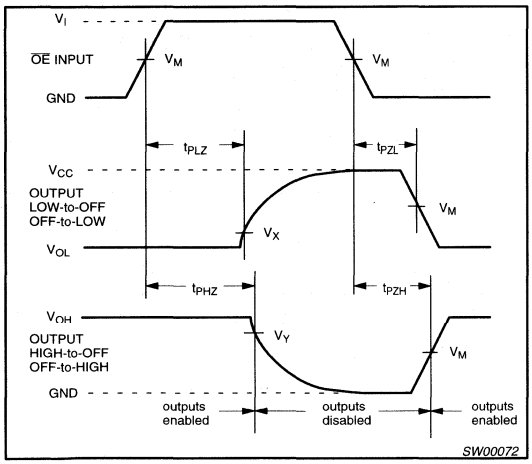
Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays

AC WAVEFORMS (Continued)

V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ – 0.1 V_{CC} at V_{CC} < 2.7V

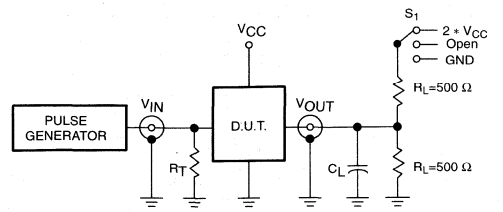


Waveform 3. Data set-up and hold times for the Dn input to the LE input



Waveform 4. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 5. Load circuitry for switching times

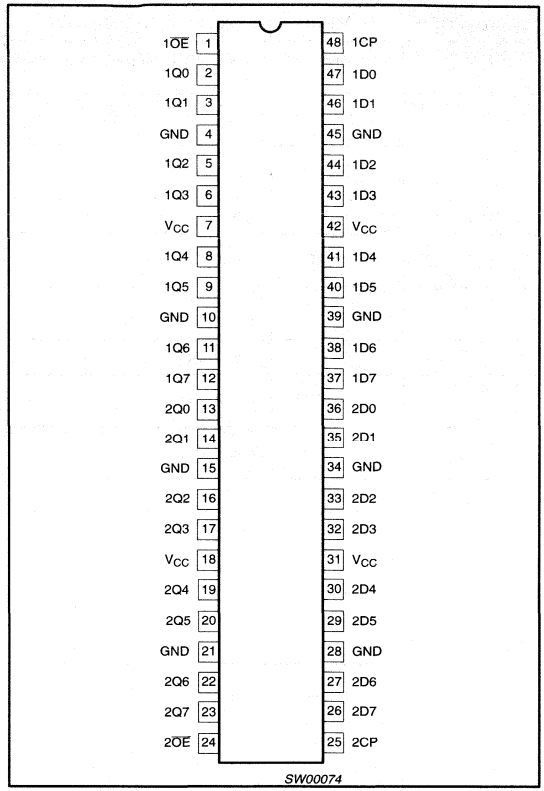
16-bit edge triggered D-type flip-flop with 5 Volt tolerant inputs/outputs (3-State)

74LVC16374A/ 74LVCH16374A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16374A only)
- High impedance when V_{CC} = 0

PIN CONFIGURATION



DESCRIPTION

The 74LVC(H)16374A is a 16-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications. The 74LVC16374A consists of 2 sections of eight positive edge-triggered flip-flops. A clock (CP) input and an output enable ($\overline{OE}$) are provided for each octal. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The 74LVCH16374A bus hold data inputs eliminates the need for external pull up resistors to hold unused inputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Cp to Qn	C_L = 50pF V_{CC} = 3.3V	3.8	ns
f_{MAX}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_{CC} = 3.3V[1]	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVC16374A DL	VC16374A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVC16374A DGG	VC16374A DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVCH16374A DL	VCH16374A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVCH16374A DGG	VCH16374A DGG	SOT362-1

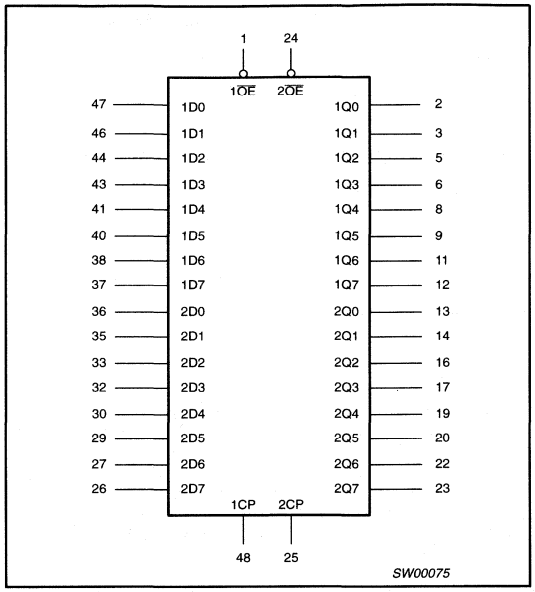
16-bit edge triggered D-type flip-flop with 5 Volt tolerant inputs/outputs (3-State)

74LVC16374A/ 74LVCH16374A

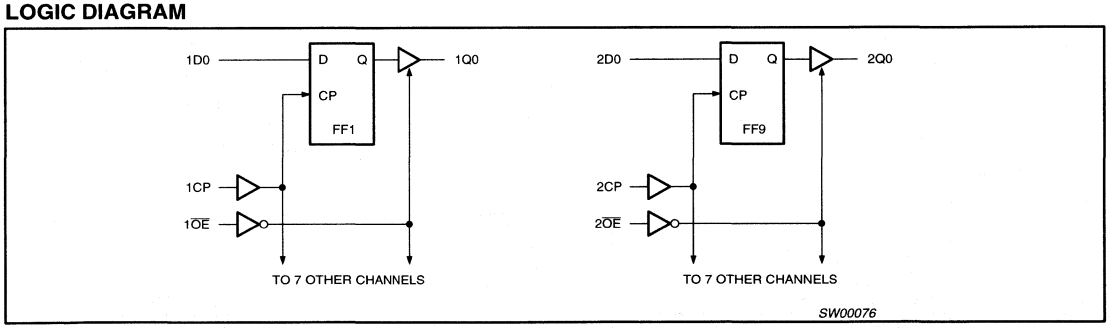
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State flip-flop outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State flip-flop outputs
24	$2\overline{OE}$	Output enable input (active LOW)
25	2CP	Clock input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data inputs
48	1CP	Clock input

LOGIC SYMBOL



LOGIC DIAGRAM

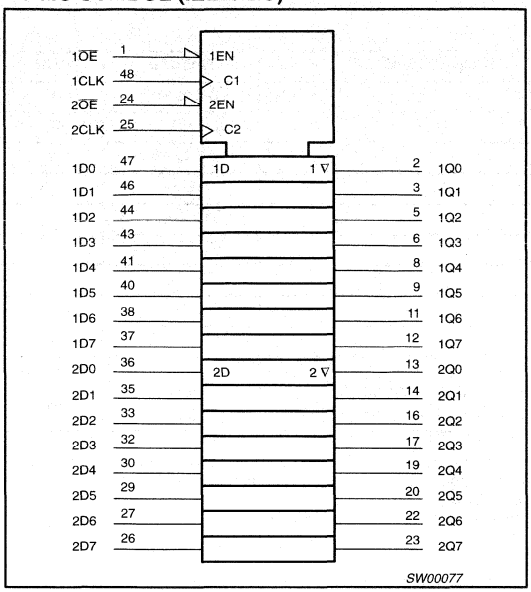


FUNCTION TABLE

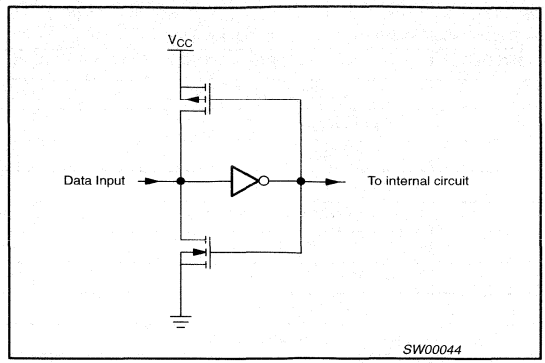
OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$n\overline{OE}$	nCP	nDx		Q0 to Q7
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
V_O	DC input voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	Note 2	−0.5 to +6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	−0.5 to V_{CC} +0.5	V
	DC output voltage; output 3-State	Note 2	−0.5 to 6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA	V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −18mA	V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA	V_{CC} − 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND[6]		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{off}	Power off leakage supply	V_{CC} = 0.0V; V_I or V_O = 5.5V			±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0		5	500	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 3.0V; V_I = 0.8V[2, 3, 4]	75			µA
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 3.0V; V_I = 2.0V[2, 3, 4]	–75			µA
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2, 3, 5]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2, 3, 5]	–500			µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_i exceeds V_{CC} allowing 5.5V on the input terminal.

AC CHARACTERISTICS

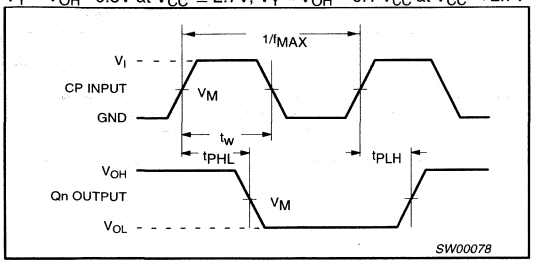
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	MAX	MAX	
t_{PHL} t_{PLH}	Propagation delay CP to Qn	1, 4	1.5	3.8	5.4	1.5	6.4	17	ns
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}$ to Qn	2, 4	1.5	3.6	5.6	1.5	6.6	20	ns
t_{PHZ} t_{PLZ}	3-State output disable time $\overline{OE}$ to Qn	2, 4	1.5	3.9	5.5	1.5	6.5	12	ns
t_W	CP pulse width HIGH or LOW	1	3.0	1.5	–	3.0	–	–	ns
t_{su}	Set-up time Dn to CP	3	2.0	0.3	–	1.9	–	–	ns
t_h	Hold time Dn to CP	3	1.5	–0.3	–	1.1	–	–	ns
f_{max}	Maximum clock pulse frequency	1	100	–	–	80	–	–	MHz

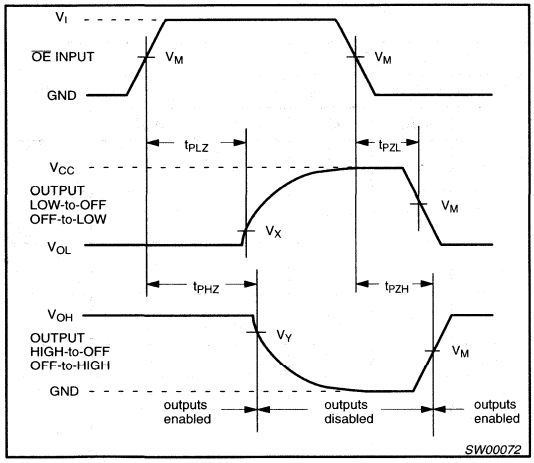
NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

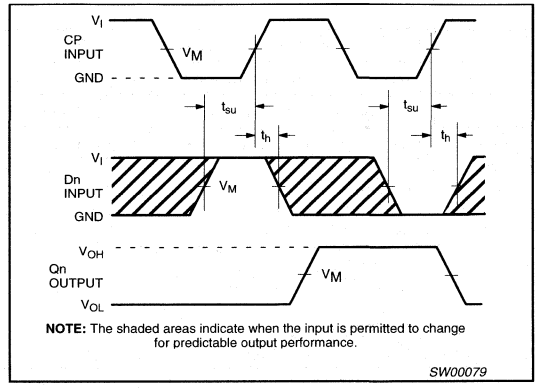
V_M = 1.5V at $V_{CC} \geq$ 2.7V; V_M = 0.5 V_{CC} at V_{CC} < 2.7V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V; $V_X = V_{OL}$ + 0.1 V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ −0.3V at $V_{CC} \geq$ 2.7V; $V_Y = V_{OH}$ − 0.1 V_{CC} at V_{CC} < 2.7V



Waveform 1. Clock (CP) to output (Qn) propagation delays, the clock pulse width and the maximum clock pulse frequency

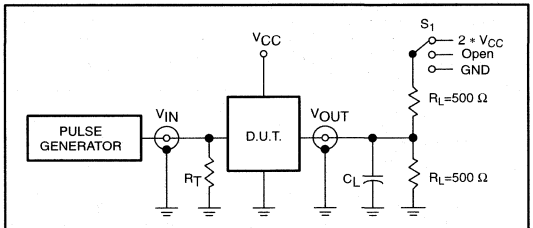


Waveform 2. 3-State enable and disable times



Waveform 3. Data set-up and hold times for the Dn input to the CP input

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 4. Load circuitry for switching times

16-bit buffer/line driver; 5V tolerant I/O (3-State) 74LVCH16541A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2 V to 3.6 V
- Drive capability ±24mA @ 3.3V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Bushold inputs eliminate the need for external pull-up resistors to hold unused inputs

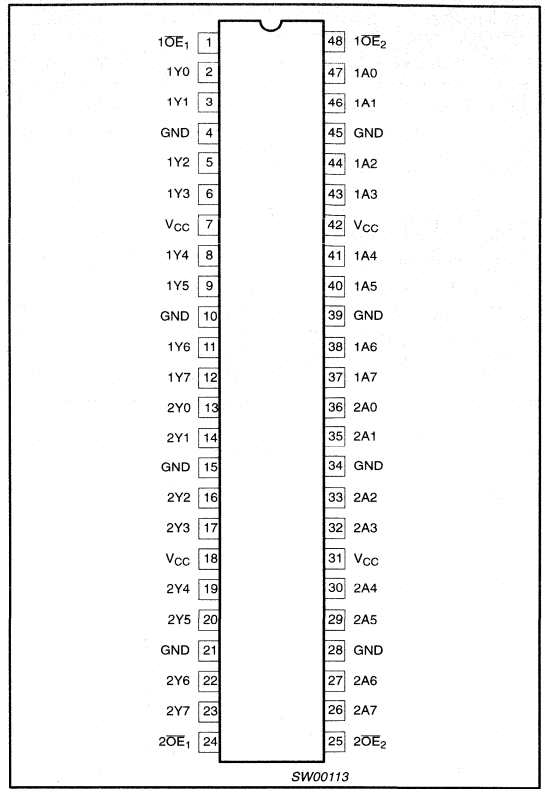
DESCRIPTION

The 74LVCH16541A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVCH16541A is a 16-bit inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}_n$ and $2\overline{OE}_n$. A HIGH on $n\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

To ensure the high impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 50pF V_{CC} = 3.3V	2.7	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1] outputs enabled output disabled	32 5	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW): $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

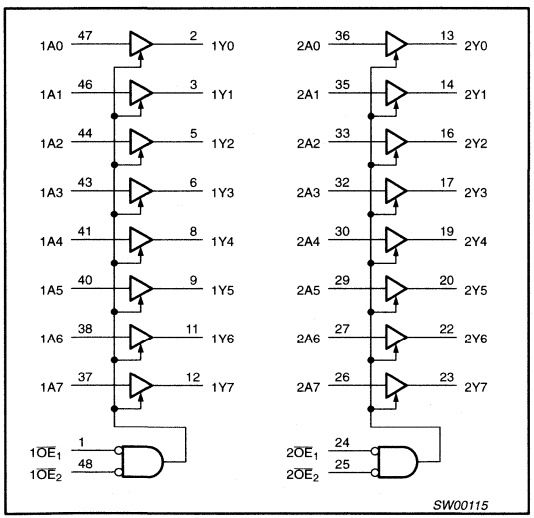
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVCH16541A DL	VCH16541A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVCH16541A DGG	VCH16541A DGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	$n\overline{OE}_1$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Y0 to 1Y7	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Y0 to 2Y7	Data outputs
25, 48	$n\overline{OE}_2$	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	Data inputs

LOGIC SYMBOL

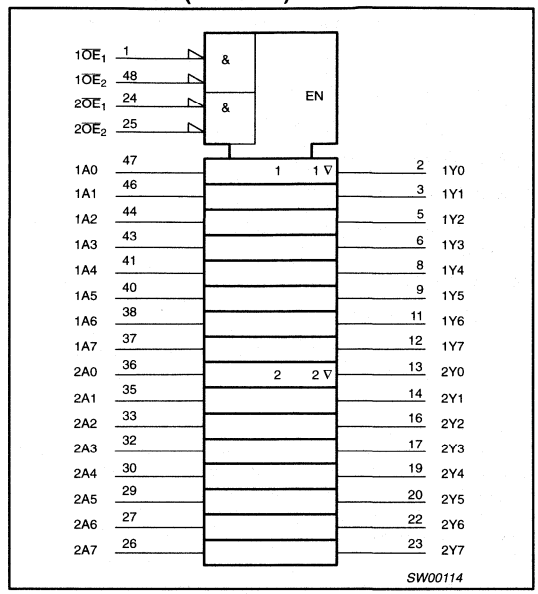


FUNCTION TABLE

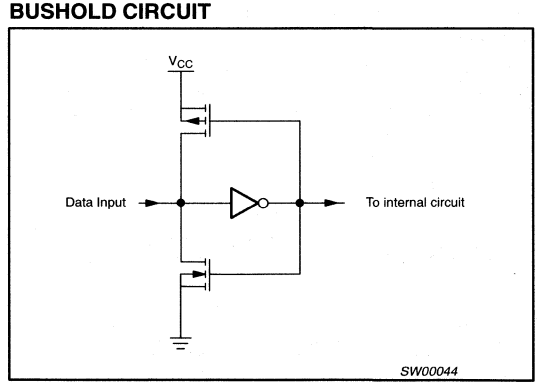
INPUTS			OUTPUT
$n\overline{OE}_1$	$n\overline{OE}_2$	nAn	nYn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage (for maximum speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range	For data input pins with bus hold	0	V_{CC}	V
		For data input pins without bus hold	0	5.5	
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
	DC output voltage range; output 3-State		0	5.5	
T_{amb}	Operating ambient temperature range in free air		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM VALUES[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage		–0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–	–50	mA
V_I	DC input voltage	Note 3	–0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 3	–0.5	V_{CC} + 0.5	V
	DC output voltage; output 3-State		–0.5	6.5	
I_O	DC output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±100	mA
T_{stg}	Storage temperature range		–65	+150	°C
P_{tot}	Power dissipation per package – SSOP (plastic medium-shrink) – TSSOP (plastic thin-medium-shrink)	For temperature range: –40 to +125°C above +70°C derate linearly 8mW/K above +60°C derate linearly 5.5mW/K		 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC}-0.5			V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC}-0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC}-0.6			
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC}-0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND[6]		±0.1	±5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = 5.5V or GND		0.1	±5	µA
I_{OFF}	Power off leakage current	V_{CC} = 0.0V; V_I or V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0		0.1	20	µA
ΔI_{CC}	Additional quiescent supply current given per input pin	V_{CC} = 2.7 to 3.6V; V_I = V_{CC} – 0.6V; I_O = 0		5	500	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 3.0V; V_I = 0.8V[2, 3, 4]	75			µA
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 3.0V; V_I = 2.0V[2, 3, 4]	–75			µA
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2, 3, 5]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2, 3, 5]	–500			µA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_i exceeds V_{CC} allowing 5.5V on the input terminal.

AC CHARACTERISTICS

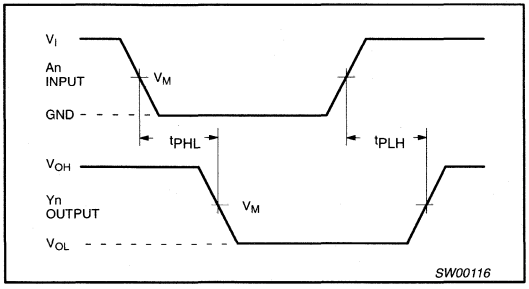
GND = 0V; $t_R = t_F \leq 2.5$ns; $C_L = 50$pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
			MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL} t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	1, 3	1.5	2.7	4.5	1.5	5.5	ns
t_{PZH} t_{PZL}	3-State output enable time $1\overline{OE}$n to 1Yn; $2\overline{OE}$n to 2Yn	2, 3	1.5	3.5	5.9	1.5	6.9	ns
t_{PHZ} t_{PLZ}	3-State output disable time $1\overline{OE}$n to 1Yn; $2\overline{OE}$n to 2Yn	2, 3	1.5	3.9	5.5	1.5	6.5	ns

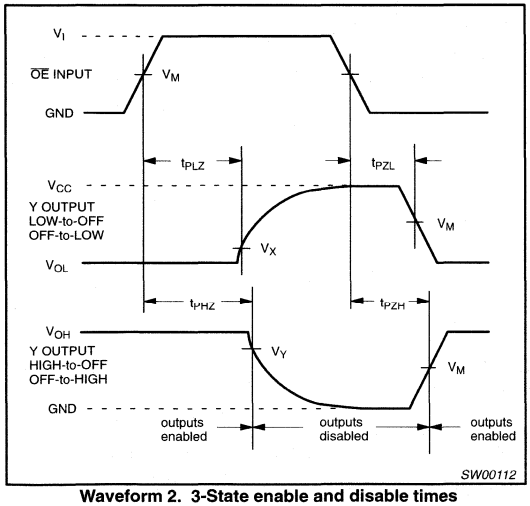
NOTE:
1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25°C$.

AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5\ V_{CC}$ at $V_{CC} < 2.7V$.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1\ V_{CC}$ at $V_{CC} < 2.7V$
$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1\ V_{CC}$ at $V_{CC} < 2.7V$

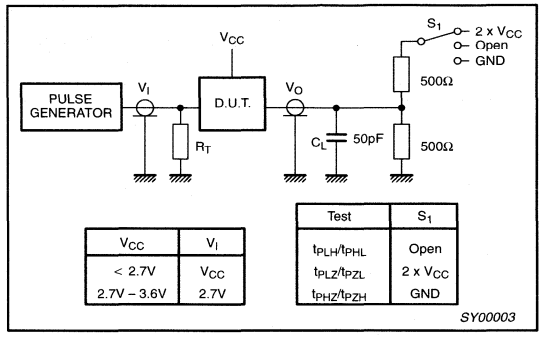


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Waveform 3. Load circuitry for switching times

Section 5
Advanced Low Voltage CMOS (ALVC)

Advanced Low Voltage CMOS Logic

CONTENTS

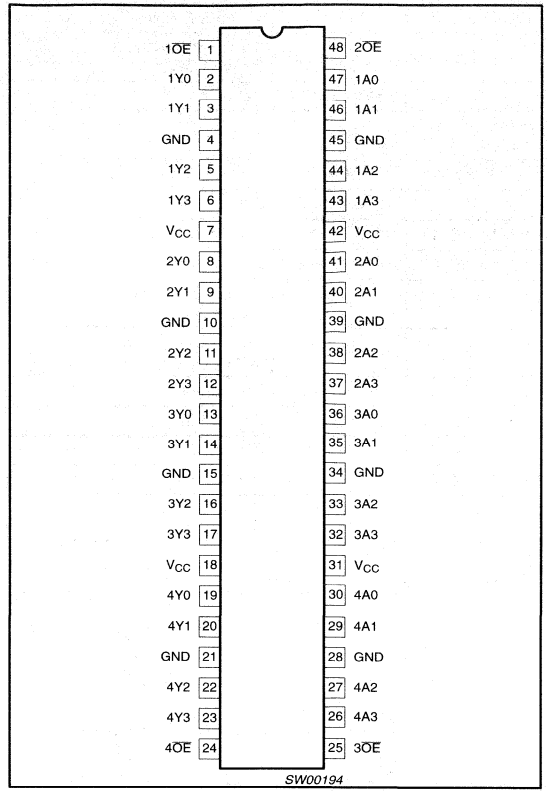
16-bit buffer/line driver (3-State)

74ALVC16244/ 74ALVCH16244

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on data inputs (74ALVCH16244 only)
- Output drive capability 50Ω transmission lines @ 85°C
- Current drive ±24 mA at 3.0 V

PIN CONFIGURATION



DESCRIPTION

The 74ALVC16244(74ALVCH16244) is a 16-bit non-inverting buffer/line driver with 3-State outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-State outputs are controlled by the output enable inputs 1$\overline{OE}$ and 2$\overline{OE}$. A HIGH on n$\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

The 74ALVCH16244 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

The 74ALVC16244 has 5V tolerant inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Yn	V_{CC} = 2.5V, CL = 30pF V_{CC} = 3.3V, CL = 50pF		1.9 1.9	ns
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	Outputs enabled	25	pF
			Outputs disabled	4	

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

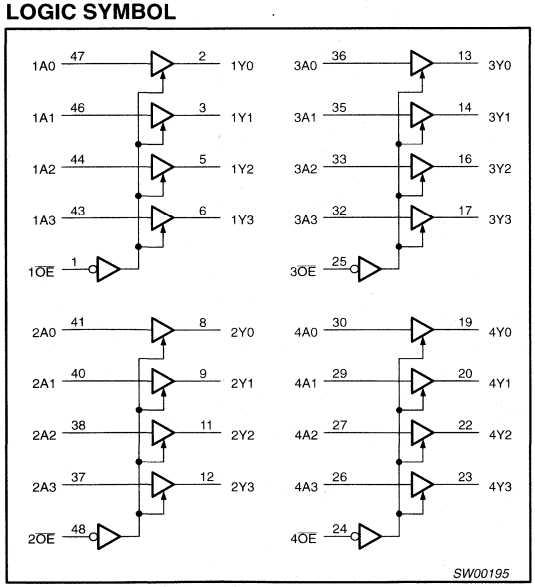
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVC16244 DL	AC16244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVC16244 DGG	AC16244 DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVCH16244 DL	ACH16244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16244 DGG	ACH16244 DGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	Data outputs
19, 20, 22, 23	4Y0 to 4Y3	Data outputs
24	$4\overline{OE}$	Output enable input (active LOW)
25	$3\overline{OE}$	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	Data inputs
41, 40, 38, 37	2A0 to 2A3	Data inputs
47, 46, 44, 43	1A0 to 1A3	Data inputs
48	$2\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

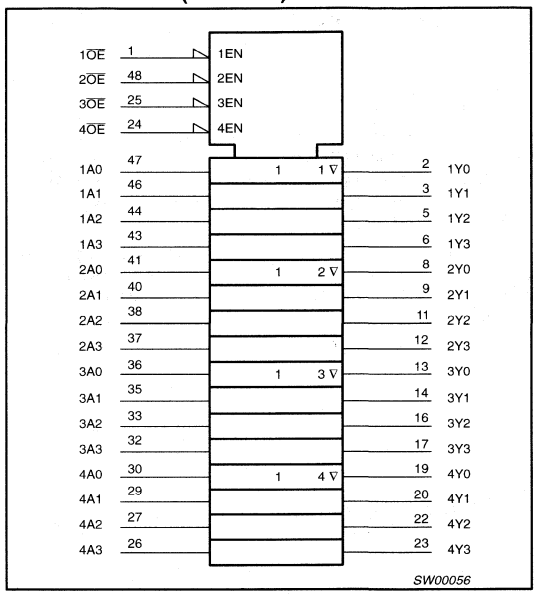


FUNCTION TABLE

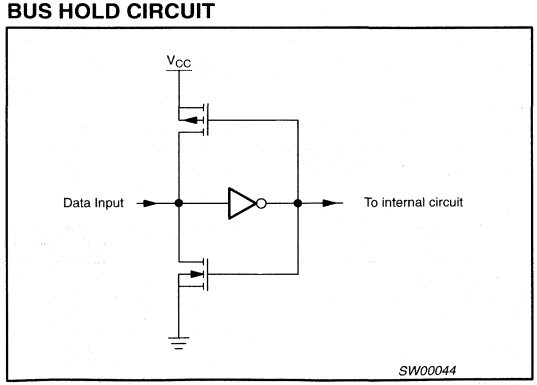
INPUTS		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range	For data input pins with bus hold	0	V_{CC}	V
		For data input pins without bus hold	0	5.5	
		For control pins	0	5.5	
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For data inputs with bus hold[2]	–0.5 to V_{CC} +0.5	V
		For data inputs without bus hold[2]	–0.5 to +5.5	
		For control pins[2]	–0.5 to +5.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 1.8V	0.7*V_{CC}	0.9		
		V_{CC} = 2.3 to 2.7V	1.7	1.2		
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 1.8V		0.9	0.2*V_{CC}	
		V_{CC} = 2.3 to 2.7V		1.2	0.7	
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 1.8 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC}–0.2	V_{CC}		V
		V_{CC} = 1.8V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC}–0.4	V_{CC}–0.10		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC}–0.3	V_{CC}–0.08		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC}–0.5	V_{CC}–0.17		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC}–0.6	V_{CC}–0.26		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC}–0.5	V_{CC}–0.14		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC}–1.0	V_{CC}–0.28		
V_{OL}	LOW level output voltage	V_{CC} = 1.8 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 1.8V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.09	0.30	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.07	0.20	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.15	0.40	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 18mA		0.23	0.60	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current per data pin with bus hold	V_{CC} = 1.8 to 3.6V; V_I = V_{CC} or GND		0.1	5	µA
	Input leakage current per data pin without bus hold	V_{CC} = 1.8 to 3.6V; V_I = 5.5 V or GND		0.1	5	
	Input leakage current per control pin	V_{CC} = 1.8 to 3.6V; V_I = 5.5 V or GND		0.1	5	
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 1.8 to 2.7V; V_I = V_{CC} or GND		0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND		0.1	15	
I_{OZ}	3-State output OFF-state current	V_{CC} = 1.8 to 2.7V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	5	µA
		V_{CC} = 2.7 to 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	10	
I_{CC}	Quiescent supply current	V_{CC} = 1.8 to 2.7V; V_I = V_{CC} or GND; I_O = 0		0.1	20	µA
		V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND; I_O = 0		0.2	40	
ΔI_{CC}	Additional quiescent supply current given per data I/O pin with bus hold	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V; I_O = 0		150	750	µA
	Additional quiescent supply current given per data I/O pin without bus hold			5	500	
	Additional quiescent supply current given per control pin			5	500	

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 2.7V	300			µA
		V_{CC} = 3.6V	450			
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 2.7V	–300			µA
		V_{CC} = 3.6V	–450			

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE AND V_{CC} < 2.3V

GND = 0V; $t_r = t_f \leq$ 2.0ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 2.3 to 2.7V			V_{CC} = 1.8V			V_{CC} = 1.2V	
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	TYP[1]	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	1.9	3.7	1.5	2.8	5.1	5.8	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nYn	2, 3	1.0	2.5	4.9	1.5	3.8	7.1	8.4	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nYn	2, 3	1.0	2.1	4.1	1.5	3.1	3.5	5.9	ns

NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 2.5V

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq$ 2.5ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	1.9	3.0	1.0	2.1	3.6	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nYn	2, 3	1.0	2.3	4.0	1.0	2.9	4.9	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nYn	2, 3	1.0	2.7	4.1	1.0	3.0	4.5	ns

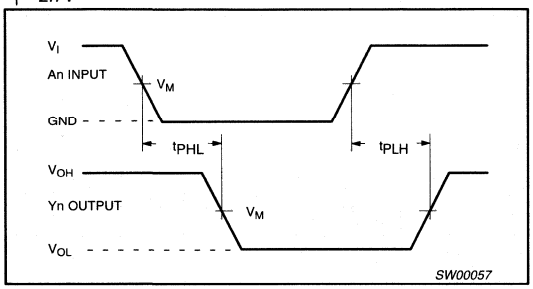
NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

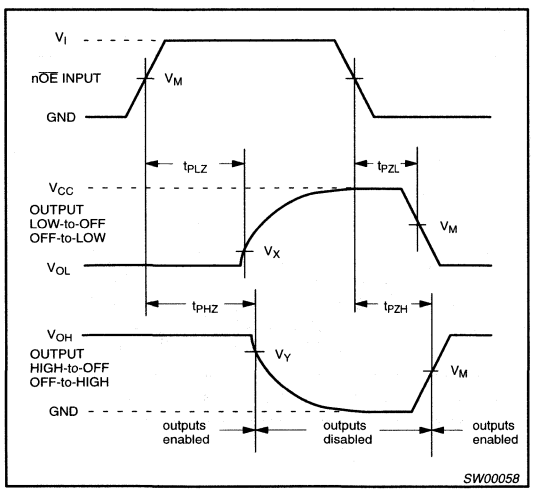
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$

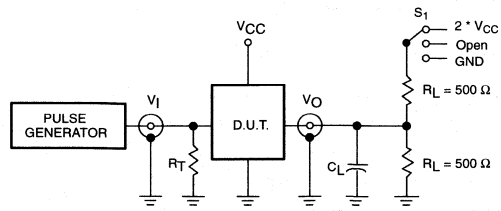


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 3. Load circuitry for switching times

16-bit buffer/line driver with 30Ω termination resistor (3-State)

74ALVCH162244

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on all data inputs
- Integrated 30Ω termination resistor

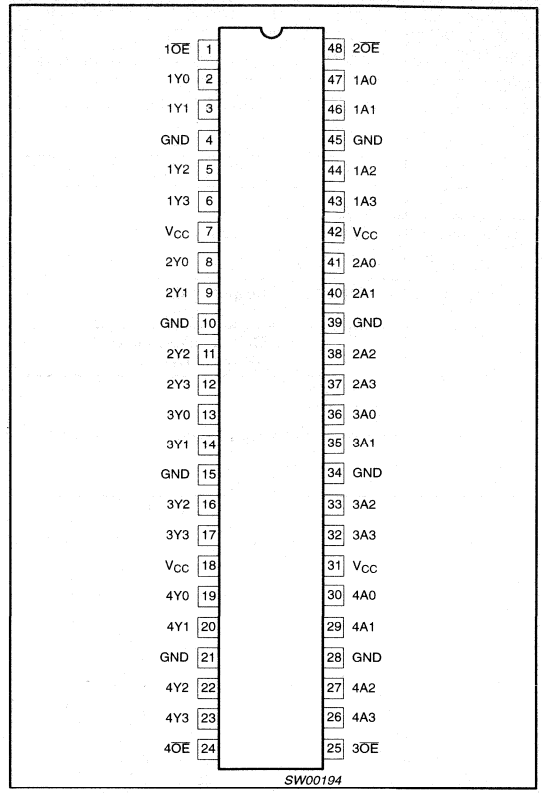
DESCRIPTION

The 74ALVCH162244 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVCH162244 is a 16-bit non-inverting buffer/line driver with 3-State outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The 74ALVCH162244 is designed with 30Ω series resistors in both HIGH and LOW output states.

The 74ALVCH162244 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Yn	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		3.0 2.7	ns
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	Outputs enabled	25	pF
			Outputs disabled	4	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

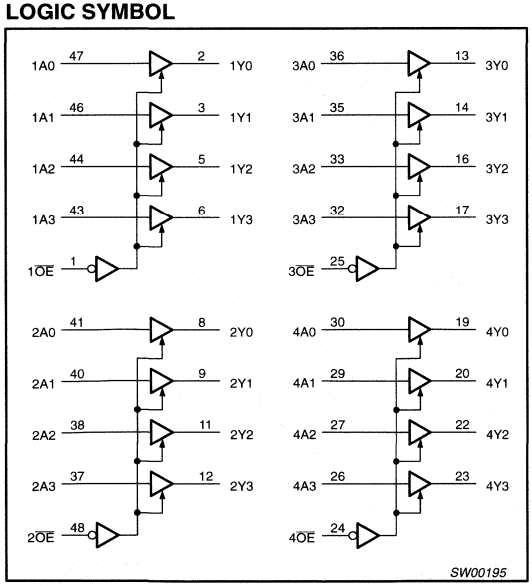
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVCH162244 DL	ACH162244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH162244 DGG	ACH162244 DGG	SOT362-1

16-bit buffer/line driver with 30Ω termination resistor (3-State) 74ALVCH162244

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	
19, 20, 22, 23	4Y0 to 4Y3	
24	$4\overline{OE}$	Output enable input (active LOW)
25	$3\overline{OE}$	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	
41, 40, 38, 37	2A0 to 2A3	
47, 46, 44, 43	1A0 to 1A3	
48	$2\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

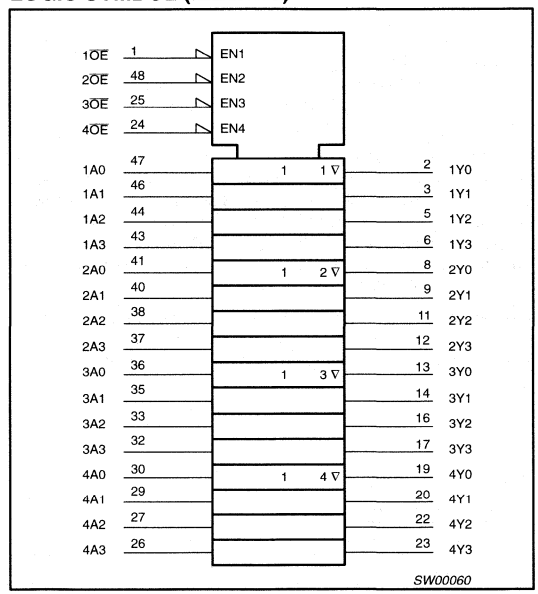


FUNCTION TABLE

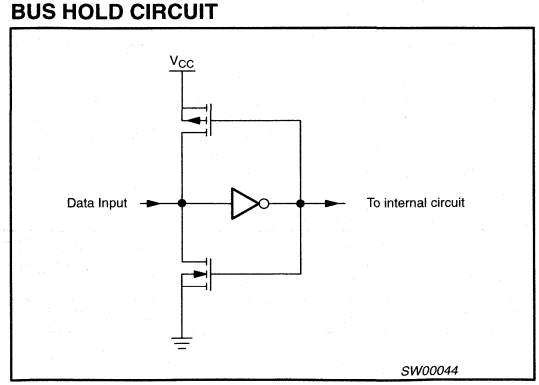
INPUTS		OUTPUT
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For data inputs with bus hold[1]	–0.5 to V_{CC} +0.5	V
		For control pins[1]	–0.5 to +4.6	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100μA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –4mA	V_{CC} – 0.4	V_{CC} – 0.11		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.6	V_{CC} – 0.17		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –4mA	V_{CC} – 0.5	V_{CC} – 0.09		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –8mA	V_{CC} – 0.7	V_{CC} – 0.19		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.6	V_{CC} – 0.13		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 1.0	V_{CC} – 0.27		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 4mA		0.07	0.40	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.11	0.55	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 4mA		0.06	0.40	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA		0.13	0.60	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.09	0.55	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.19	0.80	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	μA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	μA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	μA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	μA
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		μA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			μA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 3.6V	500			μA
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 3.6V	–500			μA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE AND V_{CC} < 2.3V

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7V			
			MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	3.0	4.9	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nYn	2, 3	1.0	4.0	6.8	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nYn	2, 3	1.0	2.3	6.3	ns

NOTES:
1. All typical values are measured at T_{amb} = 25°C and V_{CC} = 2.5V.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	2.7	4.2	1.0	3.3	4.7	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nYn	2, 3	1.0	3.5	5.6	1.0	4.6	6.7	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nYn	2, 3	1.0	2.9	5.5	1.0	3.2	5.7	ns

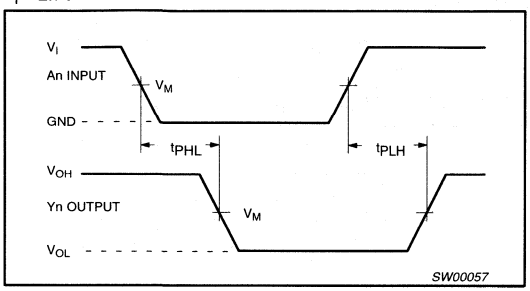
NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

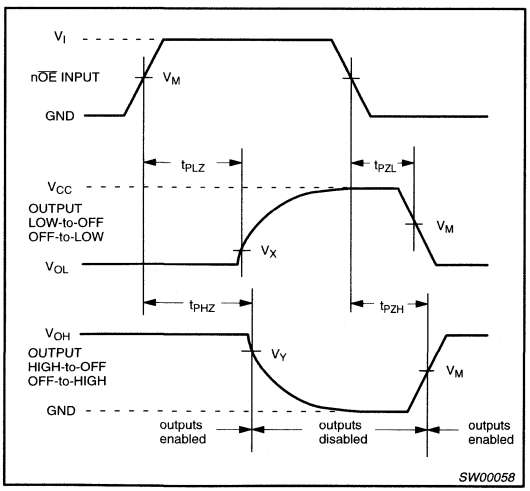
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$

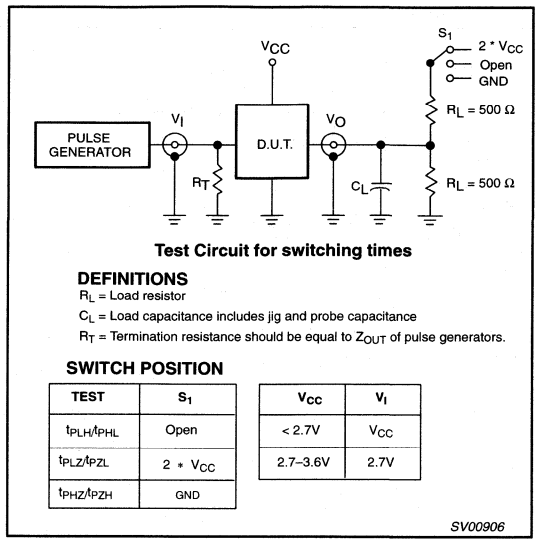


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Waveform 3. Load circuitry for switching times

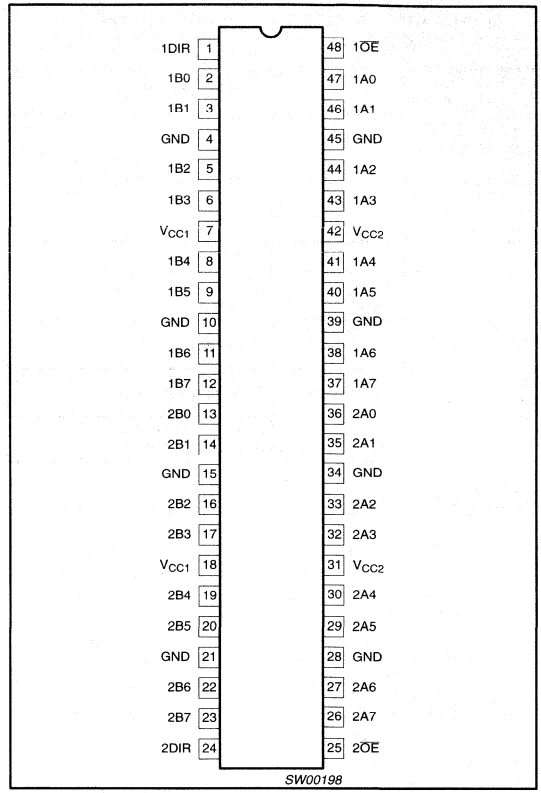
16-bit bus transceiver with direction pin (3-State)

74ALVC16245/ 74ALVCH16245

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74ALVCH16245 only)
- Output drive capability 50Ω transmission lines @ 85°C
- Current drive ±24 mA at 3.0 V

PIN CONFIGURATION



DESCRIPTION

The 74ALVC16245(74ALVCH16245) is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

The 74ALVC16245(74ALVCH16245) features two output enable ($n\overline{OE}$) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. $n\overline{OE}$ controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74ALVCH16245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

The 74ALVC16245 has 5V tolerant inputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	V_{CC} = 2.5V, CL = 30pF V_{CC} = 3.3V, CL = 50pF		1.9	ns
C_I	Input capacitance			4.0	pF
$C_{I/O}$	Input/output capacitance			8.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	Outputs enabled	29	pF
			Outputs disabled	5	

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

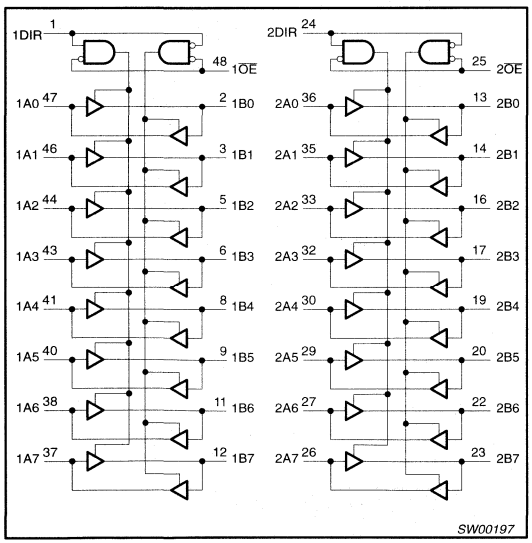
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVC16245 DL	AC16245 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVC16245 DGG	AC16245 DGG	SOT362-1
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVCH16245 DL	ACH16245 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16245 DGG	ACH16245 DGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	Direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	Data inputs/outputs
24	2DIR	Direction control
25	$2\overline{OE}$	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	Data inputs/outputs
48	$1\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

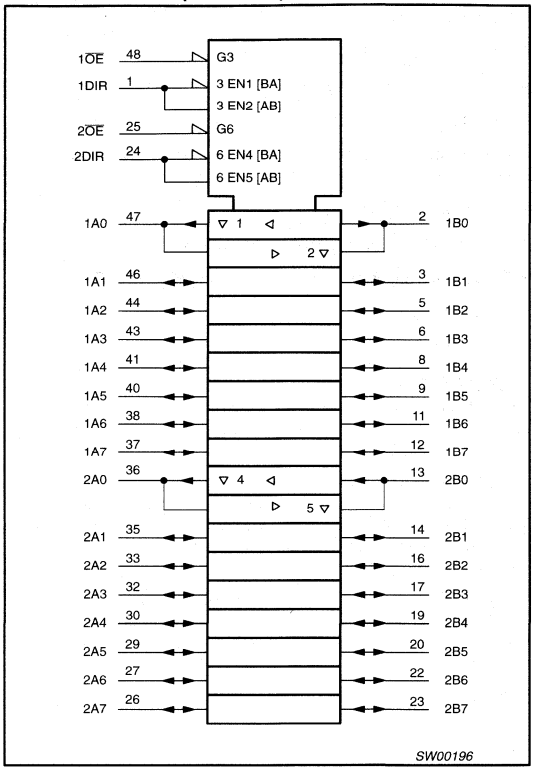


FUNCTION TABLE

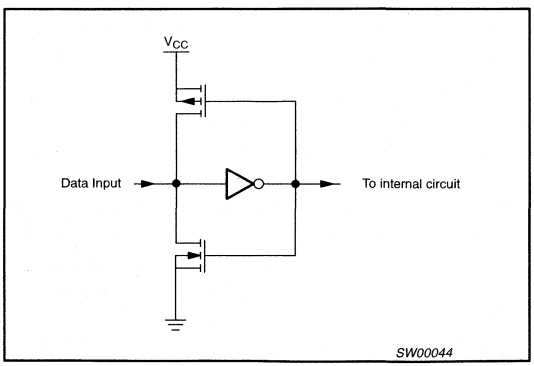
INPUTS		INPUTS/OUTPUT	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	V_I < 0	–50	mA
V_I	DC input voltage	For data inputs with bus hold[1]	–0.5 to V_{CC} +0.5	V
		For data inputs without bus hold[1]	–0.5 to +4.6	
		For control pins[1]	–0.5 to +4.6	
I_{OK}	DC output diode current	V_O > V_{CC} or V_O < 0	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC}–0.3	V_{CC}–0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC}–0.6	V_{CC}–0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC}–0.5	V_{CC}–0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC}–0.6	V_{CC}–0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC}–1.0	V_{CC}–0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current given per data I/O pin with bus hold	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 3.6V	500			µA
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 3.6V	–500			µA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq$ 2.0ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7V			
			MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nBn; nBn to nAn	1, 3	1.0	2.0	3.7	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn	2, 3	1.0	2.7	5.7	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn	2, 3	1.0	2.2	5.2	ns

NOTES:
1. All typical values are measured at T_{amb} = 25°C and V_{CC} = 2.5V.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nBn; nBn to nAn	1, 3	1.0	1.9	3.0	1.0	2.1	3.6	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn	2, 3	1.0	2.3	4.4	1.0	3.0	5.4	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn	2, 3	1.0	2.8	4.1	1.0	3.1	4.6	ns

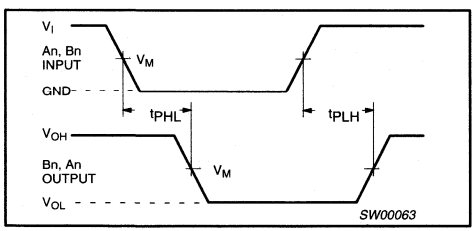
NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

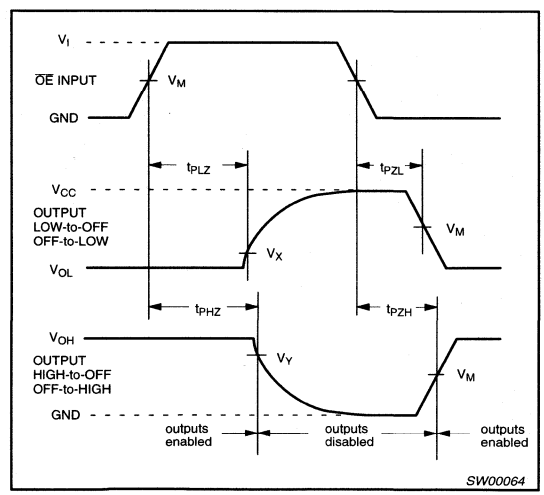
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

V_M = 1.5 V
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = 2.7V

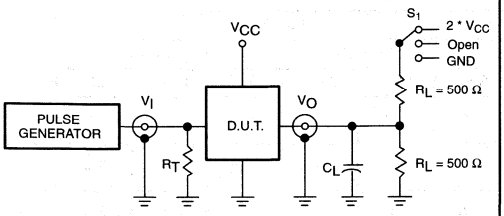


Waveform 1. Input (nAn, nBn) to output (nBn, nAn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 3. Load circuitry for switching times

16-bit bus transceiver with direction pin and 30Ω termination resistor (3-State)

74ALVCH162245

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on all data inputs
- Integrated 30Ω termination resistor

DESCRIPTION

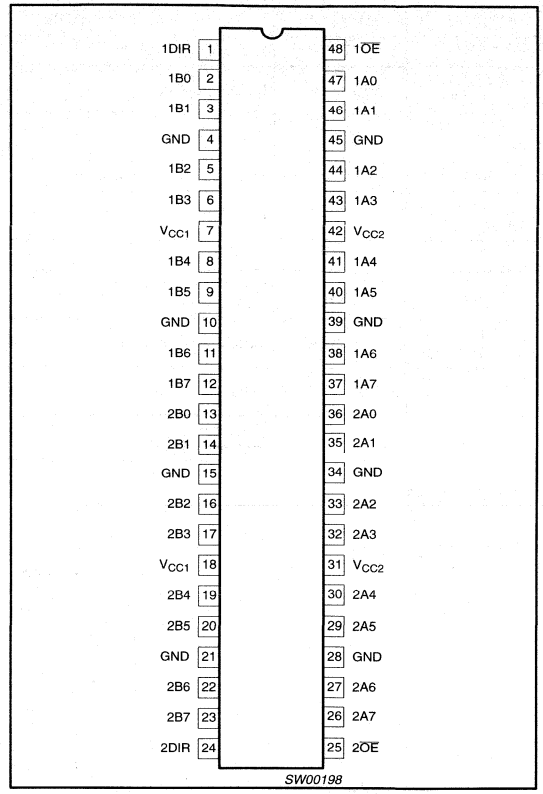
The 74ALVCH162245 is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

The 74ALVCH162245 features two output enable ($n\overline{OE}$) inputs for easy cascading and two send/receive (nDIR) inputs for direction control. $n\overline{OE}$ controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74ALVCH162245 is designed with 30Ω series resistors in both HIGH and LOW output states.

The 74ALVCH162245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.4	ns
C_I	Input capacitance			4.0	pF
$C_{I/O}$	Input/output capacitance			8.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	Outputs enabled	27	pF
			Outputs disabled	4	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVCH162245 DL	ACH162245 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH162245 DGG	ACH162245 DGG	SOT362-1

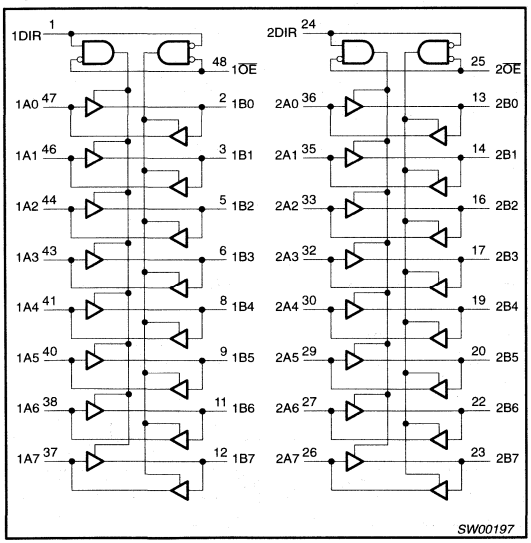
16-bit bus transceiver with direction pin and 30Ω termination resistor (3-State)

74ALVCH162245

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	Direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	Data inputs/outputs
24	2DIR	Direction control
25	$2\overline{OE}$	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	Data inputs/outputs
48	$1\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL

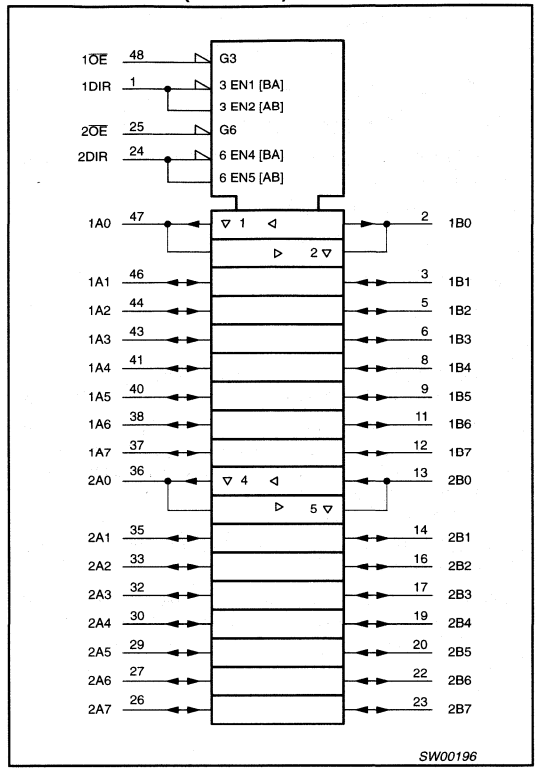


FUNCTION TABLE

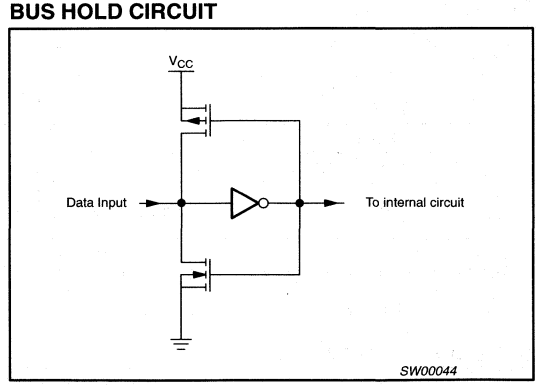
INPUTS		INPUTS/OUTPUT	
nOE	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF–state

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For data inputs with bus hold[1]	–0.5 to V_{CC} +0.5	V
		For control pins[1]	–0.5 to +4.6	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –4mA	V_{CC} – 0.4	V_{CC} – 0.11		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.6	V_{CC} – 0.17		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –4mA	V_{CC} – 0.5	V_{CC} – 0.09		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –8mA	V_{CC} – 0.7	V_{CC} – 0.19		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.6	V_{CC} – 0.13		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 1.0	V_{CC} – 0.27		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 4mA		0.07	0.40	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.11	0.55	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 4mA		0.06	0.40	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA		0.13	0.60	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.09	0.55	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.19	0.80	
I_I	Input leakage current per data pin with bus hold	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current given per data I/O pin with bus hold	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 3.6V	500			µA
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 3.6V	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7V			
			MIN	TYP[1, 2]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nBn; nBn to nAn	1, 3	1.0	2.5	4.9	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn	2, 3	1.0	2.9	6.8	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn	2, 3	1.0	3.0	6.3	ns

NOTES:
1. All typical values are measured T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 2.5V

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3 \pm 0.3V$			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nBn; nBn to nAn	1, 3	1.0	2.4	4.2	1.0	2.7	4.7	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn	2, 3	1.0	3.0	5.6	1.0	3.9	6.7	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn	2, 3	1.0	2.6	5.5	1.0	2.9	5.7	ns

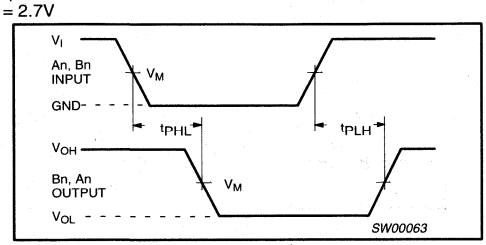
NOTES:
1. All typical values are measured T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

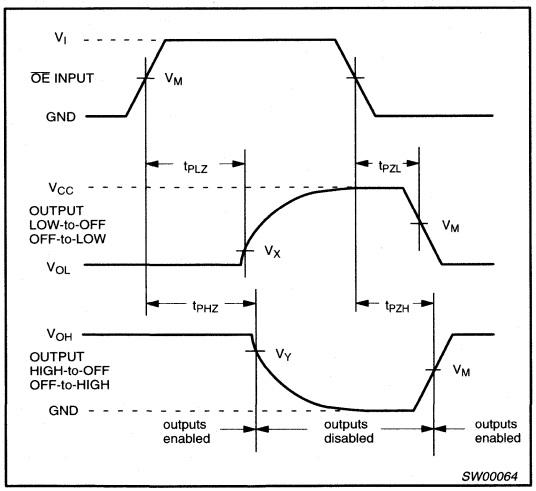
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$

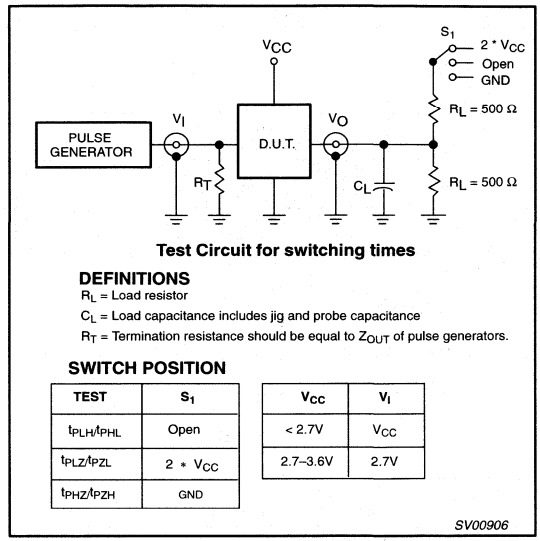


Waveform 1. Input (nAn, nBn) to output (nBn, nAn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

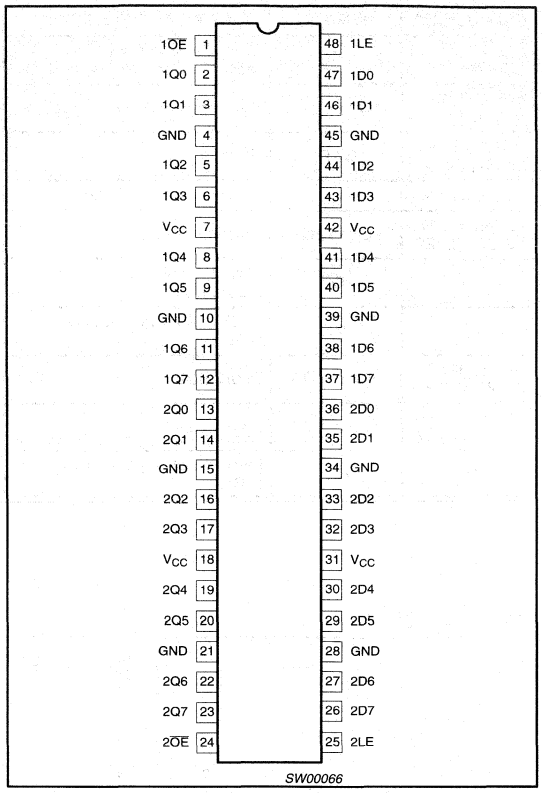
Waveform 3. Load circuitry for switching times

16-bit D-type transparent latch (3-State) 74ALVCH16373

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C
- Current drive ±24 mA at 3.0 V

PIN CONFIGURATION



DESCRIPTION

The 74ALVCH16373 is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. Incorporates bus hold data inputs which eliminate the need for external pull-up or pull-down resistors to hold unused inputs. One latch enable (LE) input and one output enable ($\overline{OE}$) are provided per 8-bit section.

The 74ALVCH16373 consists of 2 sections of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay Dn to Qn	V_{CC} = 2.5V, C_L = 30pF		2.1	ns
		V_{CC} = 3.3V, C_L = 50pF		2.1	
	Propagation delay LE to Qn	V_{CC} = 2.5V, C_L = 30pF		2.2	
		V_{CC} = 3.3V, C_L = 50pF		2.2	
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Outputs enabled	16	pF
			Outputs disabled	10	

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

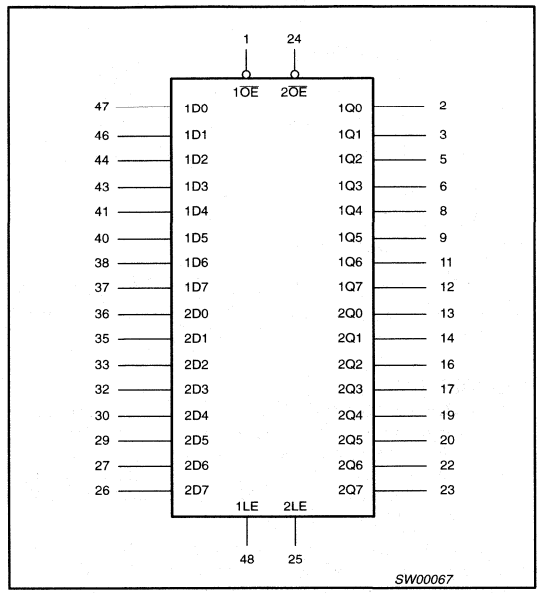
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVCH16373 DL	ACH16373 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16373 DGG	ACH16373 DGG	SOT362-1

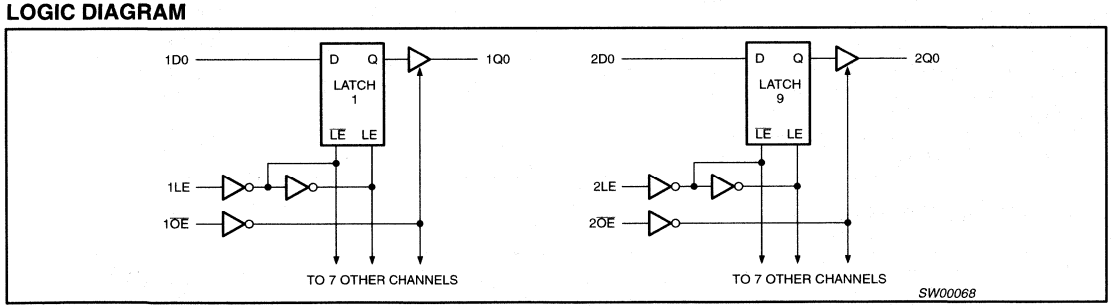
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	Data inputs/outputs
24	$2\overline{OE}$	Output enable input (active LOW)
25	2LE	Latch enable input (active HIGH)
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data inputs
48	1LE	Latch enable input (active HIGH)

LOGIC SYMBOL



LOGIC DIAGRAM

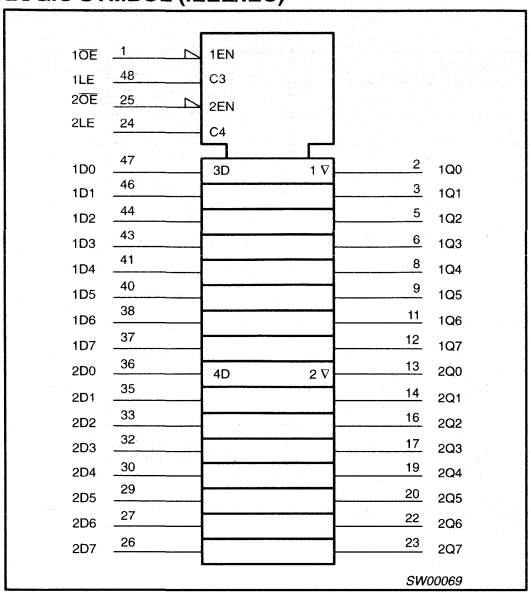


FUNCTION TABLE (per section of eight bits)

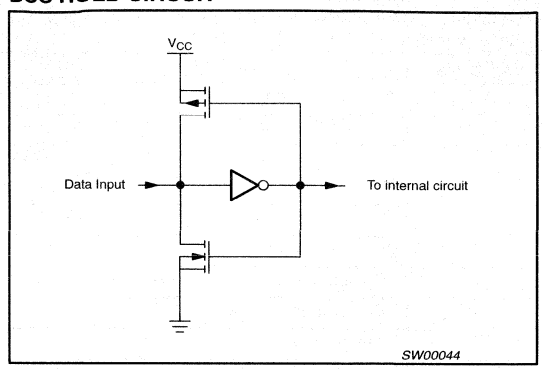
OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$n\overline{OE}$	nLE	nDn		nQn
Enable and read register (transparent mode)	L L	H H	L H	L H	L H
Latch and read register (hold mode)	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range	For data input pins	0	V_{CC}	V
		For control pins	0	5.5	
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[2]	–0.5 to +4.6	V
		For data inputs[2]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 1.8V	0.7*V_{CC}	0.9		
		V_{CC} = 2.3 to 2.7V	1.7	1.2		
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 1.8V		0.9	0.2*V_{CC}	
		V_{CC} = 2.3 to 2.7V		1.2	0.7	
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 1.8 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 1.8V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.4	V_{CC} – 0.10		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.17		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –18mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

V_{OL}	LOW level output voltage	V_{CC} = 1.8 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100μA		GND	0.20	V
		V_{CC} = 1.8V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.09	0.30	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.20	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.40	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.23	0.60	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current per control pin	V_{CC} = 1.8 to 3.6V; V_I = 5.5V or GND		0.1	5	μA
	Input leakage current per data pin	V_{CC} = 1.8 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 1.8 to 2.7V; $V_I = V_{CC}$ or GND		0.1	10	μA
		V_{CC} = 3.6V; $V_I = V_{CC}$ or GND		0.1	15	
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	μA
I_{CC}	Quiescent supply current	V_{CC} = 1.8 to 2.7V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	μA
		V_{CC} = 2.7 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	
ΔI_{CC}	Additional quiescent supply current given per control pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	μA
	Additional quiescent supply current given per data I/O pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		μA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			μA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 2.7V	300			μA
		V_{CC} = 3.6V	450			
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 2.7V	–300			μA
		V_{CC} = 3.6V	–450			

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE AND V_{CC} < 2.3V

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 2.3 to 2.7V			V_{CC} = 1.8V			V_{CC} = 1.2V	
			MIN	TYP[1, 2]	MAX	MIN	TYP1	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay nDn to nYn	1, 5	1.0	2.1	3.9	1.5	3.2	5.7	8.8	ns
t_{PHL}/t_{PLH}	Propagation delay nLE to nYn	2, 5	1.0	2.2	3.9	1.5	3.4	5.9	7.4	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nYn	4, 5	1.0	2.6	5.2	1.5	4.0	7.3	8.9	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nYn	4, 5	1.0	2.2	4.1	1.5	3.2	5.6	8.9	ns
t_W	nLE pulse width HIGH	2	3.0	1.0	–	3.5	1.0	–	–	ns
t_{SU}	Set-up time nDn to nLE	3	1.0	–0.1	–	1.0	–0.1	–	–	ns
t_h	Hold time nDn to nLE	3	1.5	0.2	–	1.2	0.1	–	–	ns

NOTES:

1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 2.5V.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nDn to nYn	1, 5	1.0	2.1	3.3	1.0	2.3	3.7	ns
t_{PHL}/t_{PLH}	Propagation delay nLE to nYn	2, 5	1.0	2.2	3.2	1.0	2.2	3.5	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nYn	4, 5	1.0	2.3	4.2	1.0	2.9	4.9	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nYn	4, 5	1.0	2.8	4.1	1.0	3.1	4.7	ns
t_W	nLE pulse width HIGH	2	2.5	1.0	–	3.0	1.0	–	ns
t_{SU}	Set-up time nDn to nLE	3	1.0	0.0	–	1.0	–0.1	–	ns
t_h	Hold time nDn to nLE	3	1.2	0.2	–	1.5	0.4	–	ns

NOTES:

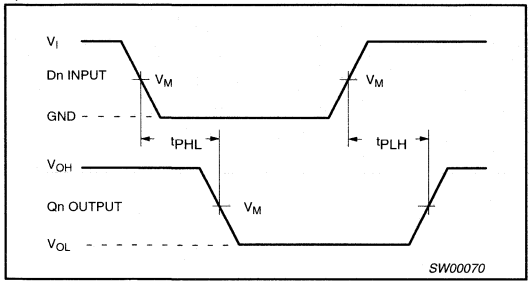
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V.

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

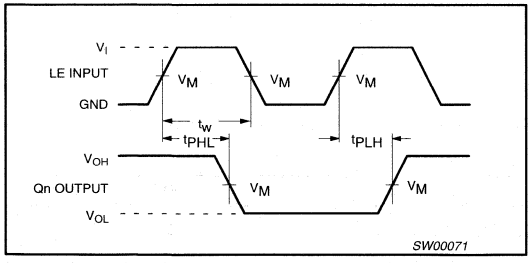
V_M = 0.5 V_{CC}
V_X = V_{OL} + 0.15V
V_Y = V_{OH} –0.15V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = V_{CC}

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

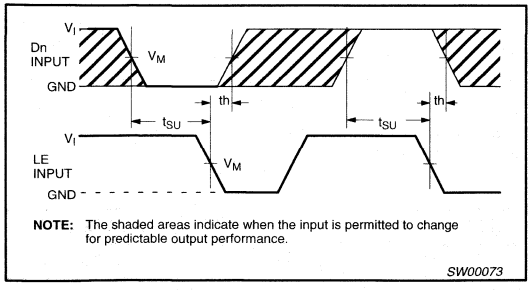
V_M = 1.5 V
V_X = V_{OL} + 0.3V
V_Y = V_{OH} –0.3V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = 2.7V



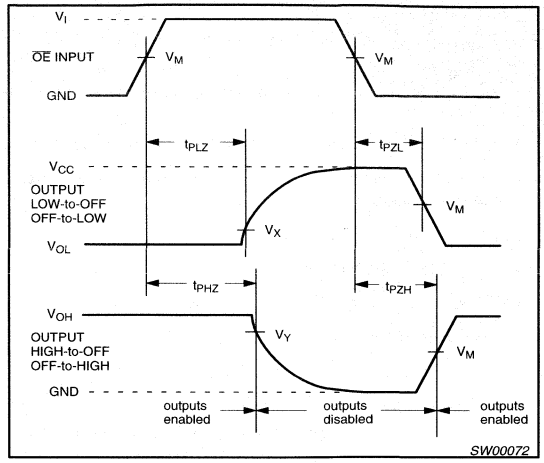
Waveform 1. Input (Dn) to output (Qn) propagation delays



Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays

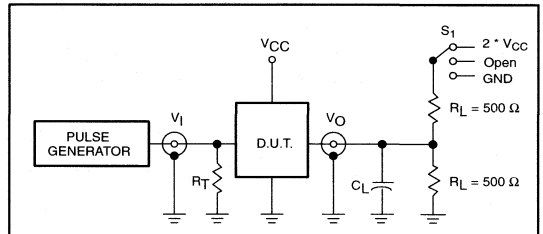


Waveform 3. Data set-up and hold times for the Dn input to the LE input



Waveform 4. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

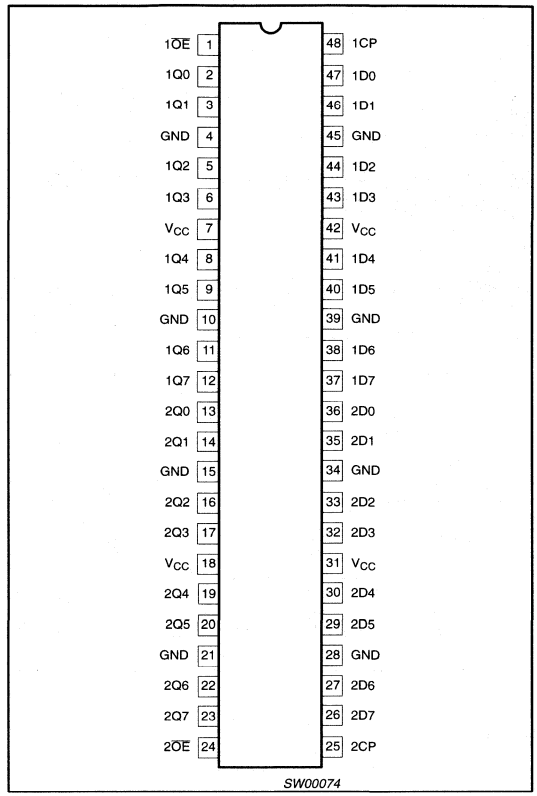
Waveform 5. Load circuitry for switching times

16-bit edge-triggered D-type flip-flop (3-State) 74ALVCH16374

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Output drive capability 50Ω transmission lines @ 85°C
- Current drive ±24 mA at 3.0 V

PIN CONFIGURATION



DESCRIPTION

The 74ALVCH16374 is a 16-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus oriented applications. Incorporates bus hold data inputs which eliminate the need for external pull-up or pull-down resistors to hold unused inputs. The 74ALVCH16374 consists of 2 sections of eight edge-triggered flip-flops. A clock (CP) input and an output enable ($\overline{OE}$) are provided per 8-bit section.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	V_{CC} = 2.5V, C_L = 30pF		2.3	ns
		V_{CC} = 3.3V, C_L = 50pF		2.4	
f_{MAX}	Maximum clock frequency	V_{CC} = 2.5V		300	MHz
		V_{CC} = 3.3V		350	MHz
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per flip-flop	V_I = GND to V_{CC}[1]	Outputs enabled	16	pF
			Outputs disabled	10	

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

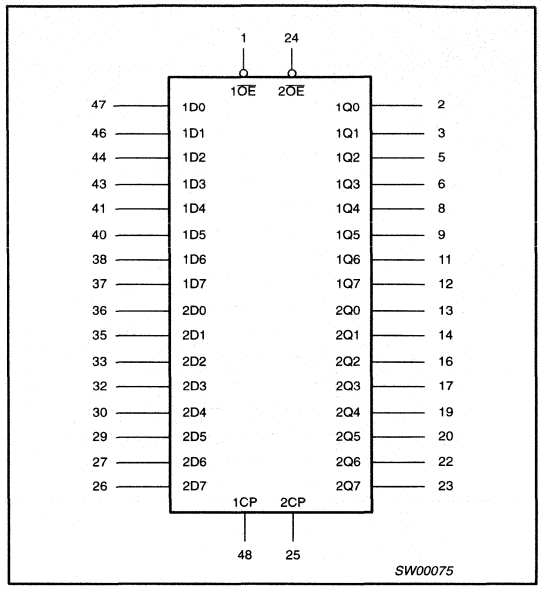
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVCH16374 DL	ACH16374 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16374 DGG	ACH16374 DGG	SOT362-1

16-bit edge-triggered D-type flip-flop (3-State) 74ALVCH16374

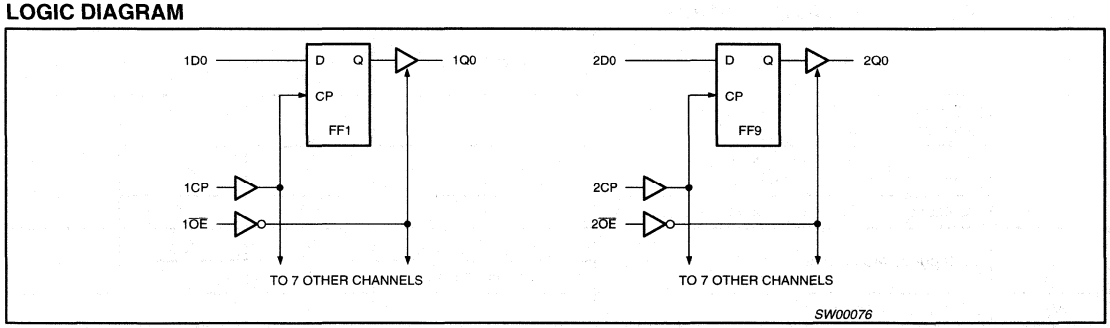
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State flip-flop outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State flip-flop outputs
24	$2\overline{OE}$	Output enable input (active LOW)
25	2CP	Clock input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data inputs
48	1CP	Clock input

LOGIC SYMBOL



LOGIC DIAGRAM

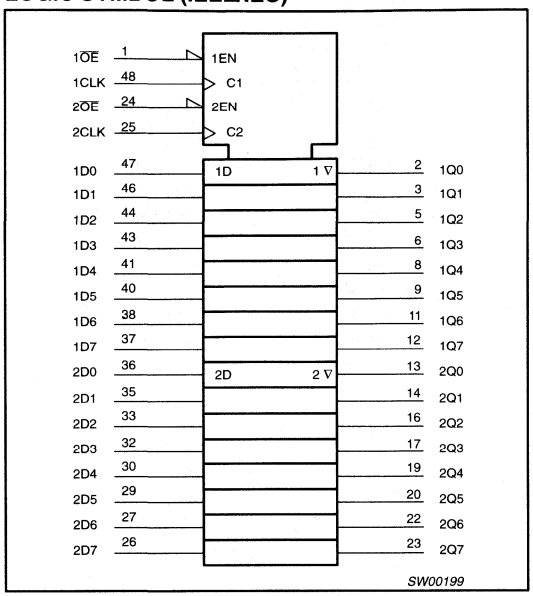


FUNCTION TABLE

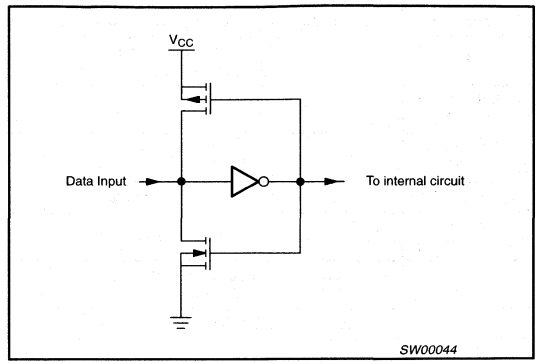
OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	Dn		Q0 to Q7
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range	For data input pins	0	V_{CC}	V
		For control pins	0	5.5	
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	−50	mA
V_I	DC input voltage	For control pins[1]	−0.5 to +4.6	V
		For data inputs[1]	−0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	−0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package −plastic medium-shrink (SSOP) −plastic thin-medium-shrink (TSSOP)	For temperature range: −40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 1.8V	0.7*V_{CC}	0.9		
		V_{CC} = 2.3 to 2.7V	1.7	1.2		
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 1.8V		0.9	0.2*V_{CC}	
		V_{CC} = 2.3 to 2.7V		1.2	0.7	
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 1.8 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = −100µA	V_{CC} − 0.2	V_{CC}		V
		V_{CC} = 1.8V; V_I = V_{IH} or V_{IL}; I_O = −6mA	V_{CC} − 0.4	V_{CC} − 0.10		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = −6mA	V_{CC} − 0.3	V_{CC} − 0.08		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC} − 0.5	V_{CC} − 0.17		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = −18mA	V_{CC} − 0.6	V_{CC} − 0.26		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = −12mA	V_{CC} − 0.5	V_{CC} − 0.14		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = −24mA	V_{CC} − 1.0	V_{CC} − 0.28		

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{OL}	LOW level output voltage	V_{CC} = 1.8 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 1.8V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.09	0.30	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.20	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.40	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.23	0.60	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current per control pin	V_{CC} = 1.8 to 3.6V; V_I = 5.5V or GND		0.1	5	µA
	Input leakage current per data pin	V_{CC} = 1.8 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 1.8 to 2.7V; $V_I = V_{CC}$ or GND		0.1	10	µA
		V_{CC} = 3.6V; $V_I = V_{CC}$ or GND		0.1	15	
I_{OZ}	3-State output OFF-state current	V_{CC} = 1.8 to 2.7V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	5	µA
		V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 1.8 to 2.7V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	20	µA
		V_{CC} = 2.7 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	
ΔI_{CC}	Additional quiescent supply current given per control pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		5	500	µA
	Additional quiescent supply current given per data I/O pin			150	750	
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 2.7V	300			µA
		V_{CC} = 3.6V	450			
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 2.7V	–300			µA
		V_{CC} = 3.6V	–450			

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE AND V_{CC} < 2.3V

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 2.3 to 2.7V			V_{CC} = 1.8V			V_{CC} = 1.2V	
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	TYP1	
t_{PHL}/t_{PLH}	Propagation delay nCP to nQn	1, 4	1.0	2.3	4.3	1.5	3.6	6.5	7.7	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nQn	2, 4	1.0	2.6	4.8	1.5	4.0	7.2	8.7	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nQn	2, 4	1.0	2.1	4.0	1.5	3.1	5.4	6.2	ns
t_W	nCP pulse width HIGH or LOW	1	3.0	1.6	–	4.0	2.0	–	–	ns
t_{su}	Set-up time Dn to nCP	3	1.2	0.2	–	1.5	0.2	–	–	ns
t_h	Hold time Dn to nCP	3	0.8	–0.1	–	0.6	–0.2	–	–	ns
f_{max}	Maximum clock pulse frequency	1	150	300	–	125	250	–	–	MHz

NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 2.5V.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 2.3 to 2.7V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nCP to nQn	1, 4	1.0	2.4	3.4	1.0	2.3	3.8	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nQn	2, 4	1.0	2.3	4.0	1.0	2.9	4.8	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nQn	2, 4	1.0	2.6	4.1	1.0	2.9	4.5	ns
t_W	nCP pulse width HIGH or LOW	1	2.5	1.4	–	3.0	1.6	–	ns
t_{su}	Set-up time Dn to nCP	3	1.2	0.2	–	1.5	0.4	–	ns
t_h	Hold time Dn to nCP	3	0.8	0.0	–	0.6	–0.2	–	ns
f_{max}	Maximum clock pulse frequency	1	200	350	–	150	300	–	MHz

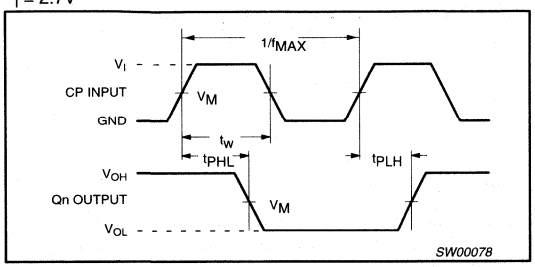
NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V.

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

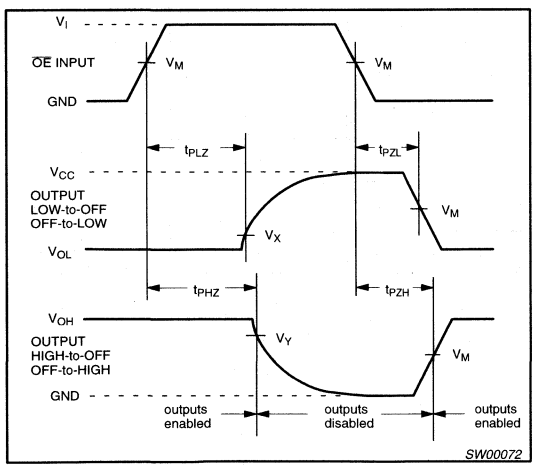
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

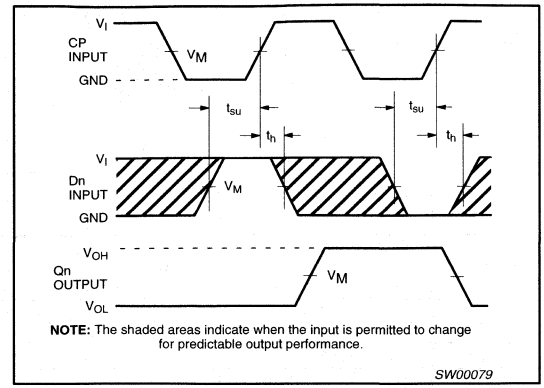
$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$



Waveform 1. Clock (CP) to output (Qn) propagation delays, the clock pulse width and the maximum clock pulse frequency

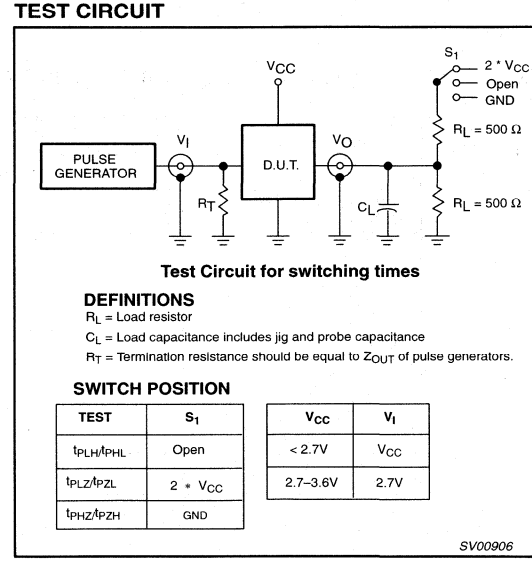


Waveform 2. 3-State enable and disable times



Waveform 3. Data set-up and hold times for the Dn input to the CP input

TEST CIRCUIT



Waveform 4. Load circuitry for switching times

18-bit universal bus transceiver (3-State) 74ALVCH16500

FEATURES

- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- All inputs have bushold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce

DESCRIPTION

The 74ALVCH16500 is a high-performance CMOS product..
This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OE_{AB} and $\overline{OE}_{BA}$), latch enable (LE_{AB} and LE_{BA}), and clock ($\overline{CP}_{AB}$ and $\overline{CP}_{BA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LE_{AB} is High. When LE_{AB} is Low, the A data is latched if $\overline{CP}_{AB}$ is held at a High or Low logic level. If LE_{AB} is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of $\overline{CP}_{AB}$. When OE_{AB} is High, the outputs are active. When OE_{AB} is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OE}_{BA}$, LE_{BA} and $\overline{CP}_{BA}$. The output enables are complimentary (OE_{AB} is active High, and $\overline{OE}_{BA}$ is active Low).

To ensure the high impedance state during power up or power down, $\overline{OE}_{BA}$ should be tied to V_{CC} through a pullup resistor and OE_{AB} should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An LE_{AB} to Bn; LE_{BA} to An CP_{AB} to Bn; CP_{BA} to An	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		3.0 3.2	ns
C_I	Input capacitance			5.0	pF
$C_{I/O}$	Input/output capacitance			10	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Outputs enabled	22	pF
			Outputs disabled	22	

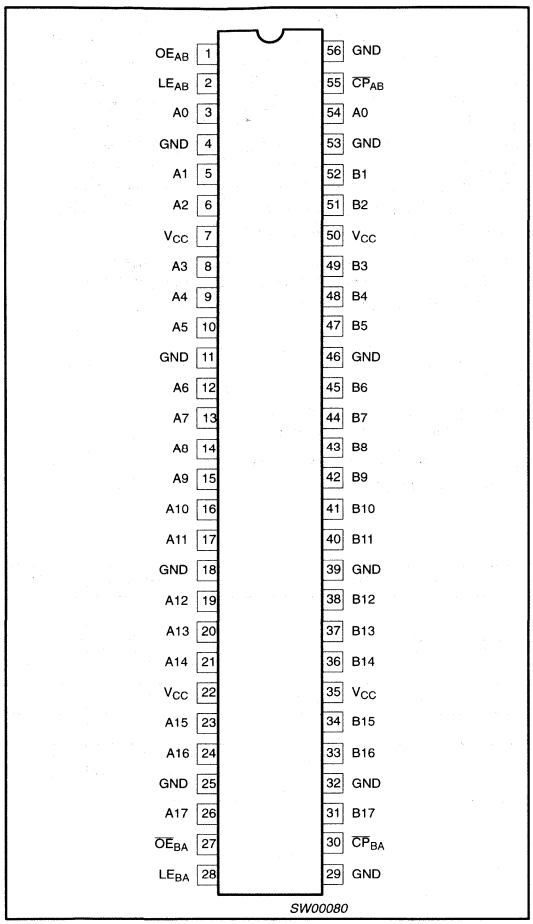
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16500 DGG	ACH16500 DGG	SOT364-1

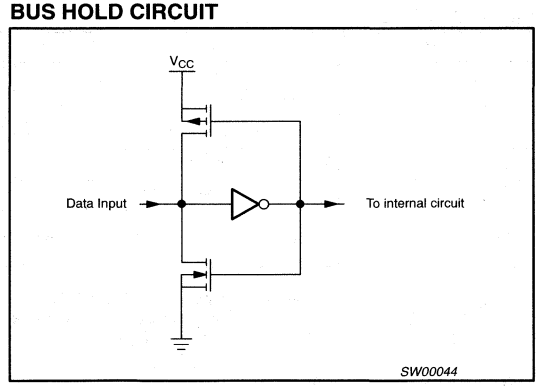
PIN CONFIGURATION



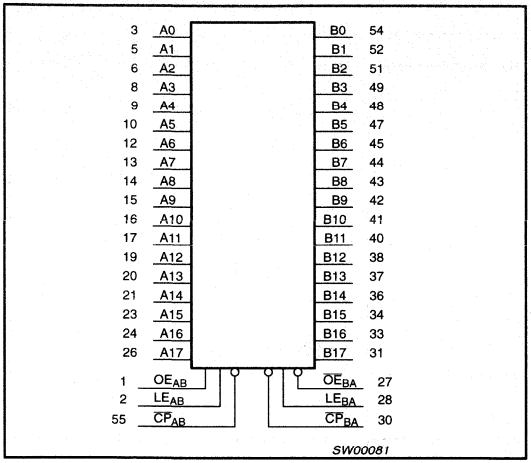
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0 to A17	Data inputs/outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
30	$\overline{CP}_{BA}$	Clock input B-to-A
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0 to B17	Data inputs/outputs
55	$\overline{CP}_{AB}$	Clock input A-to-B

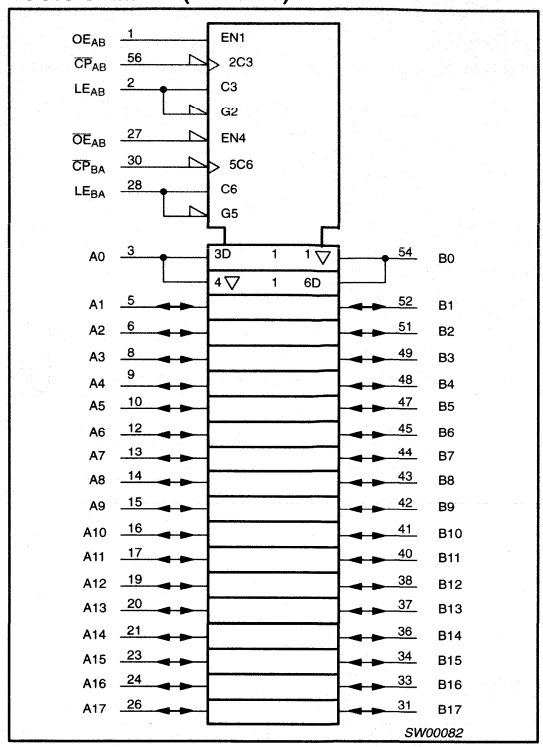
BUS HOLD CIRCUIT



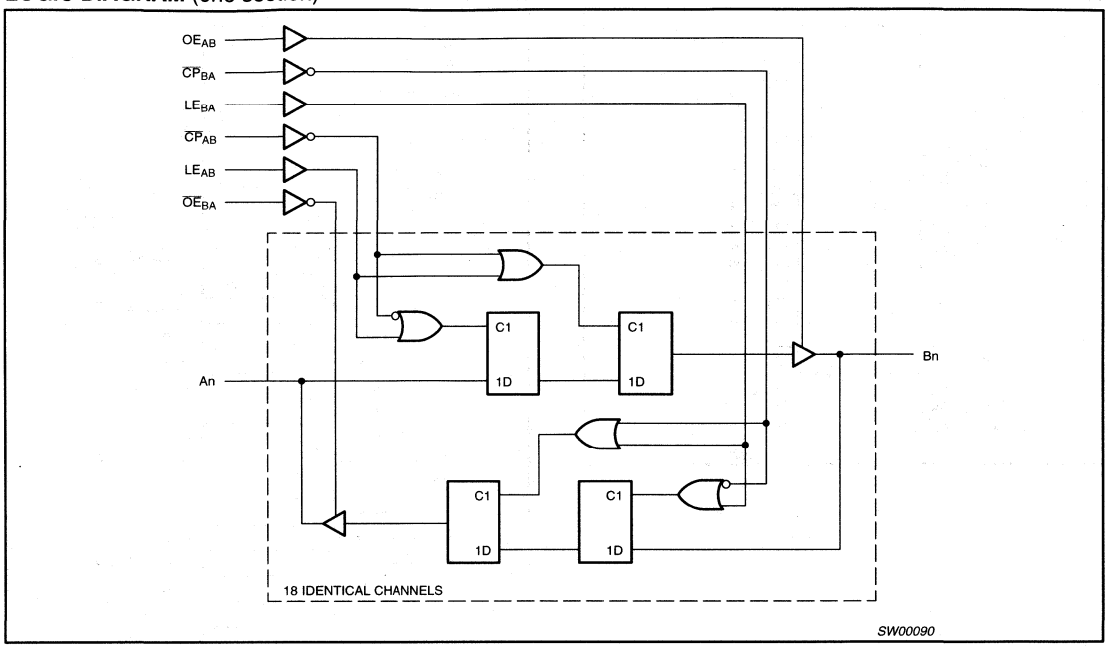
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	$\overline{CPAB}$	An		Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↓	h	H	Z	Disabled, Clock data
L	L	↓	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↓	h	H	H	Clock data & display
H	L	↓	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CPBA}$.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = High-to-Low Enable or Clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER		WAVEFORM	LIMITS			UNIT
				V_{CC} = 2.5V ± 0.2V			
				MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay An to Bn, Bn to An		1	1		5.1	ns
t_{PHL} t_{PLH}	Propagation delay LE_{BA} to An, LE_{AB} to Bn		2	1		5.9	ns
	Propagation delay CP_{BA} to An, CP_{AB} to Bn			1		6.6	
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An, OE_{AB} to Bn		3	1		5.7	ns
t_{PHZ} t_{PLZ}	3-State output disable time OE_{BA} to An, OE_{AB} to Bn		3	1		6.1	ns
t_W	LE pulse width LE_{AB} or LE_{BA} HIGH		2	3.3			ns
	LE pulse width CP_{AB} or CP_{BA} HIGH or LOW			3.3			
t_{SU}	Set-up time An before CP_{AB} ↑ or Bn before $\overline{CP}_{AB}$ ↑		4	1.7			ns
	Set-up time An before LE_{AB} ↓ or Bn before LE_{AB} ↓	CP HIGH		1.1			
		CP LOW		1.9			
t_h	Hold time An after CP_{AB} ↑ or Bn before $\overline{CP}_{AB}$ ↑		4	1.7			ns
	Hold time An before LE_{AB} ↓ or Bn before LE_{AB} ↓	CP HIGH	4	2.0			ns
		CP LOW		1.6			
f_{MAX}	Maximum clock frequency			150			

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER		WAVEFORM	LIMITS						UNIT
				V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay An to Bn, Bn to An		1	1.0		5.1	1.0		4.7	ns
t_{PHL} t_{PLH}	Propagation delay LE_{BA} to An, LE_{AB} to Bn		2	1.0		5.9	1.0		5.5	ns
	Propagation delay CP_{BA} to An, CP_{AB} to Bn			1.0		6.6	1.0		6.6	
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An, OE_{AB} to Bn		3	1.0		5.7	1.0		5.4	ns
t_{PHZ} t_{PLZ}	3-State output disable time OE_{BA} to An, OE_{AB} to Bn		3	1.0		6.1	1.0		5.7	ns
t_W	LE pulse width LE_{AB} or LE_{BA} HIGH		2	3.3			3.3			ns
	LE pulse width CP_{AB} or CP_{BA} HIGH or LOW		2	3.3			3.3			
t_{SU}	Set-up time An before $CP_{AB}\uparrow$ or Bn before $CP_{AB}\uparrow$		4	1.3			1.4			ns
	Set-up time An before $LE_{AB}\downarrow$ or Bn before $LE_{AB}\downarrow$	CP HIGH		1			1			
		CP LOW		1.4			1.6			
t_h	Hold time An after $CP_{AB}\uparrow$ or Bn before $\overline{CP}_{AB}\uparrow$		4	1.7			1.6			ns
	Hold time An before $LE_{AB}\downarrow$ or Bn before $LE_{AB}\downarrow$	CP HIGH	4	1.2			1.8			ns
		CP LOW		1.6			1.5			
f_{MAX}	Maximum clock frequency			150			150			

NOTES:

1. All typical values are at T_{amb} = 25°C.

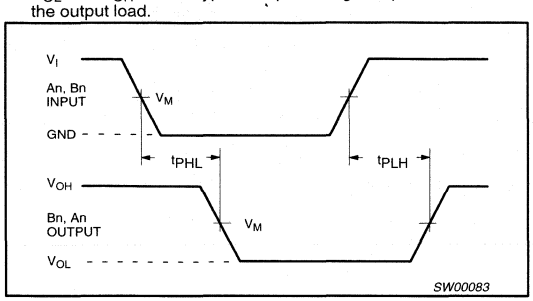
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

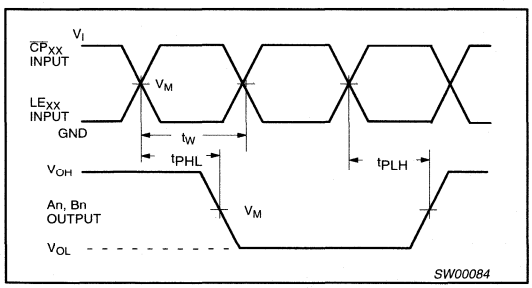
1. V_M = 0.5 V
2. $V_X = V_{OL}$ + 0.15V
3. $V_Y = V_{OH}$ – 0.15V
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

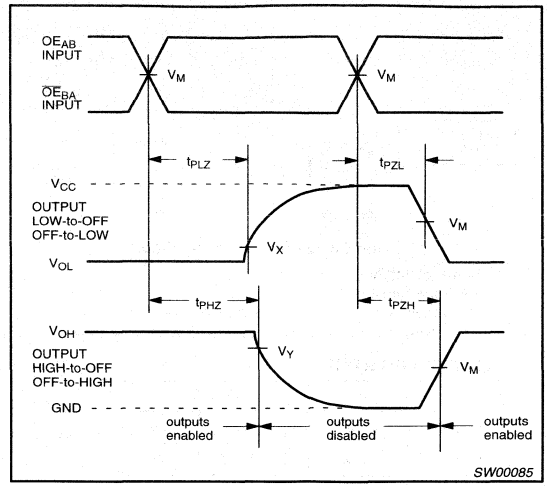
1. V_M = 1.5 V
2. $V_X = V_{OL}$ + 0.3V
3. $V_Y = V_{OH}$ – 0.3V
4. V_I = 2.7 V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



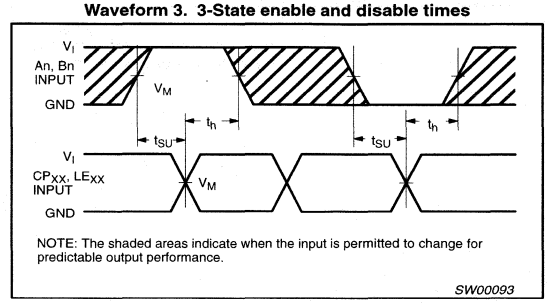
Waveform 1. Input (An, Bn) to output (Bn, An) propagation times



Waveform 2. Latch enable input (LE_{AB}, LE_{BA}) and clock pulse input ($\overline{CP}_{AB}$, $\overline{CP}_{BA}$) to output (An, Bn) propagation delays and latch enable pulse width

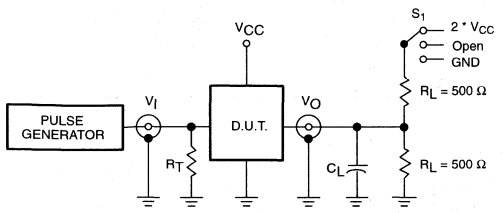


Waveform 3. 3-State enable and disable times



Waveform 4. Data set-up and hold times for the An and Bn inputs to the LE_{AB}, LE_{BA}, $\overline{CP}_{AB}$ and $\overline{CP}_{BA}$ inputs

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 5. Load circuitry for switching times

18-bit universal bus transceiver (3-State) 74ALVCH16501

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- Universal bus transceiver with D-type latches and D-type flip-flops capable of operating in transparent, latched or clocked mode.
- All inputs have bushold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- 3-State non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVCH16501 is a high-performance CMOS product designed for V_{CC} operation at 2.5V and 3.3V with I/O compatibility up to 5V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OE_{AB} and $\overline{OE}_{BA}$), latch enable (LE_{AB} and LE_{BA}), and clock (CP_{AB} and CP_{BA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LE_{AB} is High. When LE_{AB} is Low, the A data is latched if CP_{AB} is held at a High or Low logic level. If LE_{AB} is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CP_{AB}. When OE_{AB} is High, the outputs are active. When OE_{AB} is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OE}_{BA}$, LE_{BA} and CP_{BA}. The output enables are complimentary (OE_{AB} is active High, and $\overline{OE}_{BA}$ is active Low).

To ensure the high impedance state during power up or power down, $\overline{OE}_{BA}$ should be tied to V_{CC} through a pullup resistor and OE_{AB} should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An LE_{AB} to Bn; LE_{BA} to An CP_{AB} to Bn; CP_{BA} to An	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.4 2.9	ns
C_I	Input capacitance			5.0	pF
$C_{I/O}$	Input/output capacitance			10	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Outputs enabled	22	pF
			Outputs disabled	6	

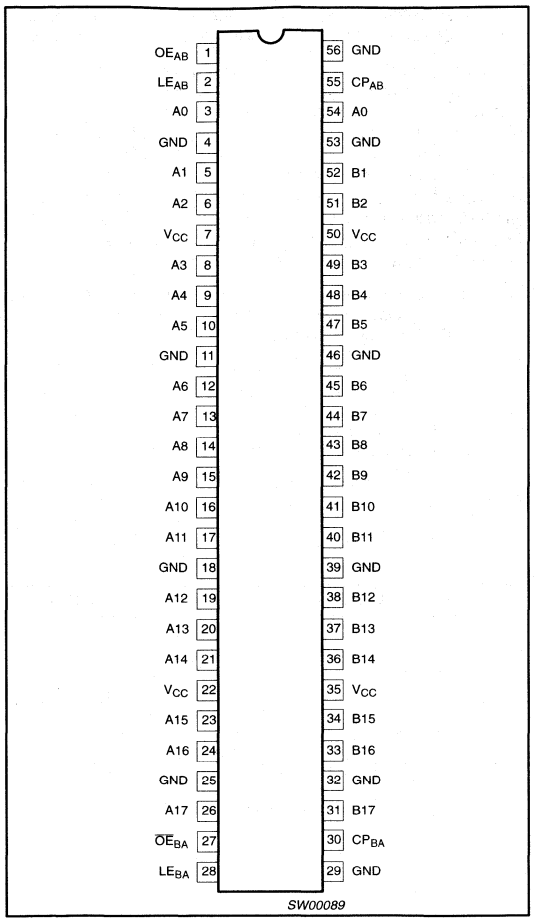
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16501 DGG	ACH16501 DGG	SOT364-1

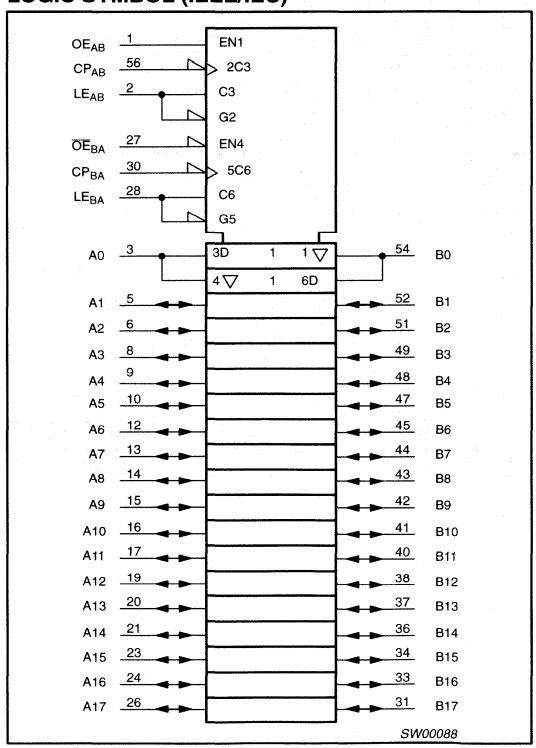
PIN CONFIGURATION



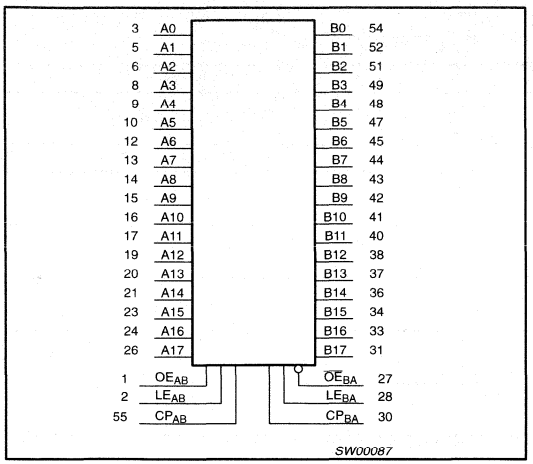
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0 to A17	Data inputs/outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
30	CP_{BA}	Clock input B-to-A
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0 to B17	Data inputs/outputs
55	CP_{AB}	Clock input A-to-B

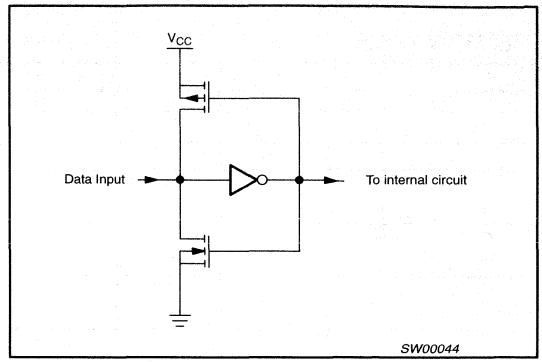
LOGIC SYMBOL (IEEE/IEC)



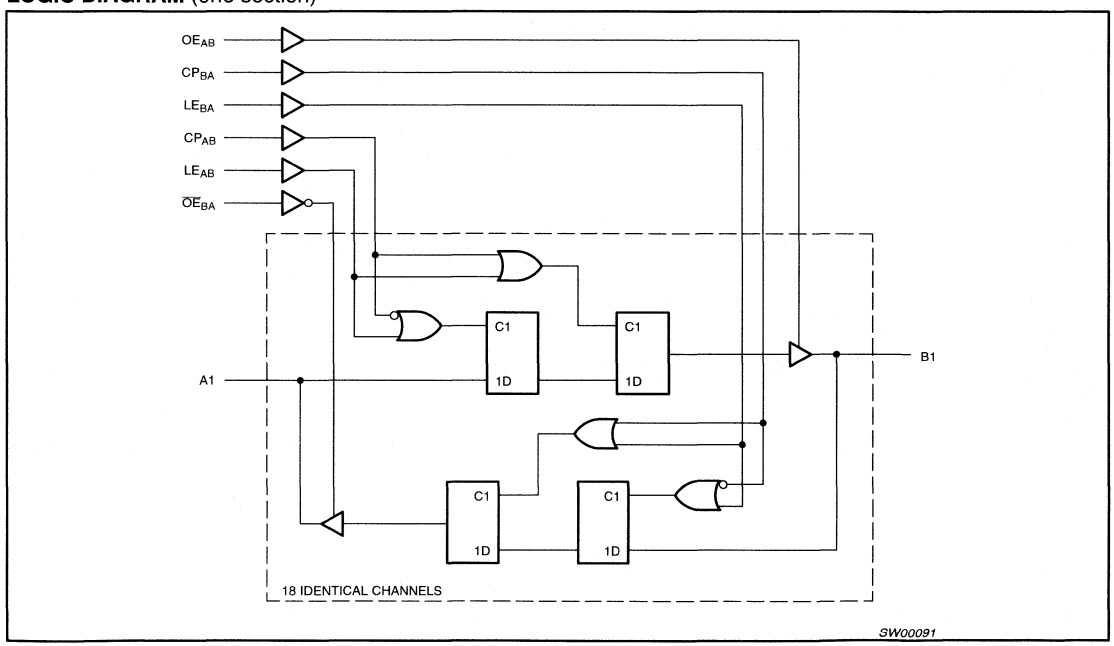
LOGIC SYMBOL



BUS HOLD CIRCUIT



LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS				Internal	OUTPUTS	OPERATING MODE
OEAB	LEAB	CPAB	An	Registers	Bn	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↑	h	H	Z	Disabled, Clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↑	h	H	H	Clock data & display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

NOTE: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CPBA.

H = High voltage level
h = High voltage level one set-up time prior to the Enable or Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Enable or Clock transition
NC= No Change
X = Don't care
Z = High Impedance "off" state
↓ = High-to-Low Enable or Clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	V_I < 0	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	V_O > V_{CC} or V_O < 0	± 50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER		WAVEFORM	LIMITS			UNIT
				V_{CC} = 2.5V ± 0.2V			
				MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay An to Bn, Bn to An		1	1		4.8	ns
t_{PHL} t_{PLH}	Propagation delay LE_{BA} to An, LE_{AB} to Bn		2	1.1		5.7	ns
	Propagation delay CP_{BA} to An, CP_{AB} to Bn			1.2		6.1	
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An, OE_{AB} to Bn		3	1.1		5.8	ns
t_{PHZ} t_{PLZ}	3-State output disable time OE_{BA} to An, OE_{AB} to Bn		3	1.5		6.2	ns
t_W	LE pulse width LE_{AB} or LE_{BA} HIGH		2	3.3			ns
	LE pulse width CP_{AB} or CP_{BA} HIGH or LOW			3.3			
t_{SU}	Set-up time An before CP_{AB} ↑ or Bn before $\overline{CP}_{AB}$ ↑		4	2.2			ns
	Set-up time An before LE_{AB} ↓ or Bn before LE_{AB} ↓	CP HIGH		1.9			
		CP LOW		1.3			
t_h	Hold time An after CP_{AB} ↑ or Bn before $\overline{CP}_{AB}$ ↑		4	0.6			ns
	Hold time An before LE_{AB} ↓ or Bn before LE_{AB} ↓	CP HIGH	4	1.4			ns
		CP LOW		1.4			
f_{MAX}	Maximum clock frequency			150			

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER		WAVEFORM	LIMITS						UNIT
				V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay An to Bn, Bn to An		1	1.0		3.9			4.5	ns
t_{PHL} t_{PLH}	Propagation delay LE_{BA} to An, LE_{AB} to Bn		2	1.0		4.6			5.3	ns
	Propagation delay CP_{BA} to An, CP_{AB} to Bn			1.0		4.9			5.6	
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An, OE_{AB} to Bn		3	1.0		4.6			6.3	ns
t_{PHZ} t_{PLZ}	3-State output disable time OE_{BA} to An, OE_{AB} to Bn		3	1.0		5			5.7	ns
t_W	LE pulse width LE_{AB} or LE_{BA} HIGH		2	3.3			3.3			ns
	LE pulse width CP_{AB} or CP_{BA} HIGH or LOW			3.3			3.3			
t_{SU}	Set-up time An before $CP_{AB}\uparrow$ or Bn before $CP_{AB}\uparrow$		4	1.7			2.1			ns
	Set-up time An before $LE_{AB}\downarrow$ or Bn before $LE_{AB}\downarrow$	CP HIGH		1.5			1.6			
		CP LOW		1			1.1			
t_h	Hold time An after $CP_{AB}\uparrow$ or Bn before $\overline{CP}_{AB}\uparrow$		4	0.7			0.6			ns
	Hold time An before $LE_{AB}\downarrow$ or Bn before $LE_{AB}\downarrow$	CP HIGH	4	1.4			1.7			ns
		CP LOW		1.4			1.7			
f_{MAX}	Maximum clock frequency			150			150			

NOTES:

1. All typical values are at T_{amb} = 25°C.

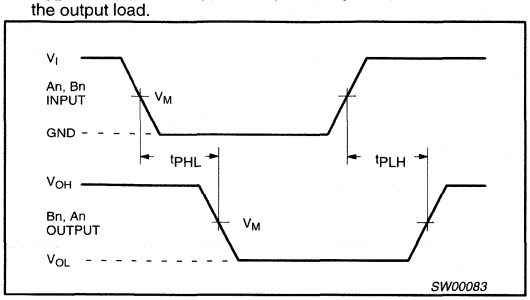
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

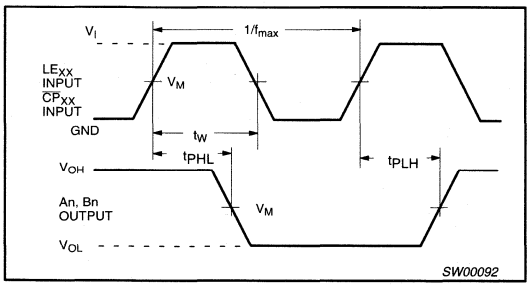
1. V_M = 0.5 V
2. $V_X = V_{OL}$ + 0.15V
3. $V_Y = V_{OH}$ − 0.15V
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

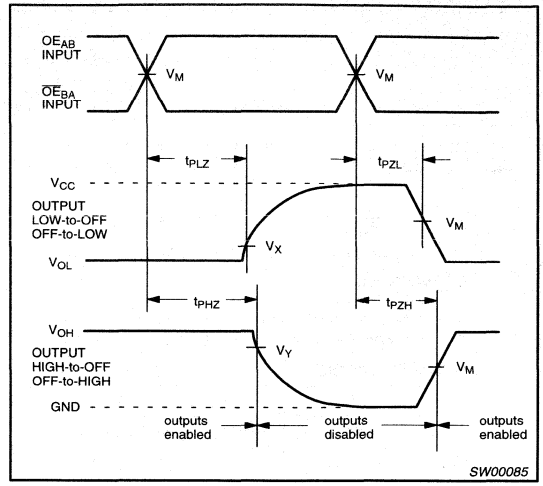
1. V_M = 1.5 V
2. $V_X = V_{OL}$ + 0.3V
3. $V_Y = V_{OH}$ − 0.3V
4. V_I = 2.7 V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



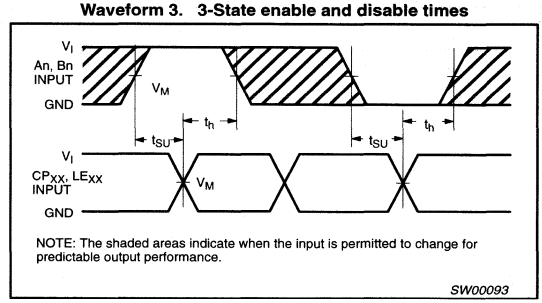
Waveform 1. Input (An, Bn) to output (Bn, An) propagation delays



Waveform 2. Latch enable input (E_{AB}, LE_{BA}) and clock pulse input (CP_{AB}, CP_{BA}) to output propagation delays and their pulse width

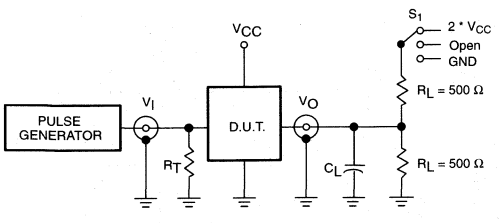


Waveform 3. 3-State enable and disable times



Waveform 4. Data set-up and hold times for the An and Bn inputs to the LE_{AB}, LE_{BA}, CP_{AB} and CP_{BA} inputs

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Figure 5. Load circuitry for switching times

16-bit buffer/line driver, inverting, 5V input tolerant (3-State)

74ALVCH16540

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on all data inputs eliminates the need for external pull-up resistors to hold unused inputs
- Output drive capability 50Ω transmission lines @ 85°C

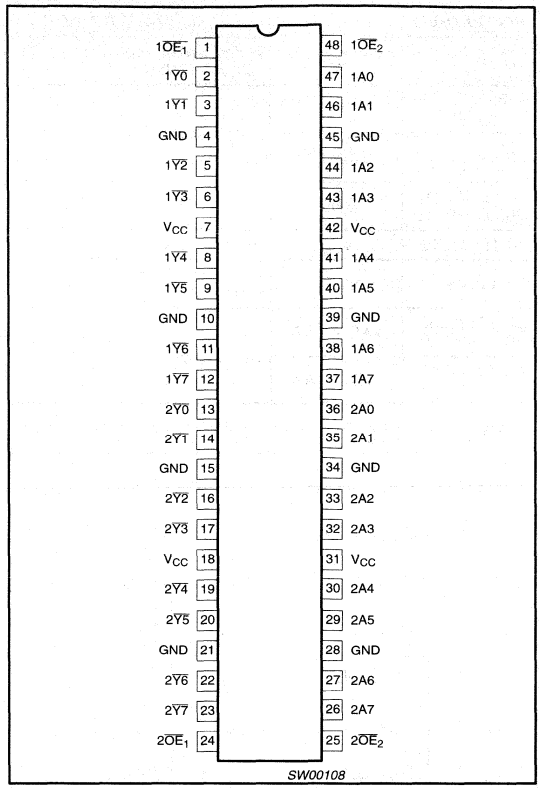
DESCRIPTION

The 74ALVCH16540 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVCH16540 is a 16-bit inverting buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}_n$ and $2\overline{OE}_n$. A HIGH on $n\overline{OE}_n$ causes the outputs to assume a high impedance OFF-state.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	C_L = 50pF; V_{CC} = 3.3V		1.8	ns
		C_L = 30pF; V_{CC} = 2.5V		1.8	ns
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	Outputs enabled	26	pF
			Outputs disabled	5	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVCH16540 DL	ACH16540 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16540 DGG	ACH16540 DGG	SOT362-1

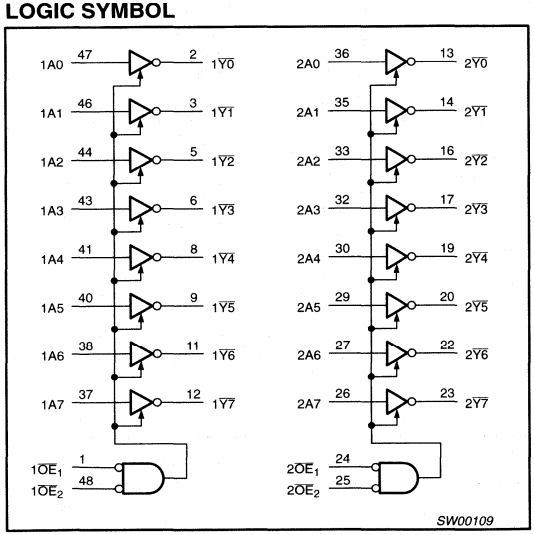
16-bit buffer/line driver, inverting, 5V input tolerant (3-State)

74ALVCH16540

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	$n\overline{OE}_1$	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Y0 to 1Y7	Data outputs
13, 14, 16, 17, 19, 20, 22, 23	2Y0 to 2Y7	
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
25, 48	$n\overline{OE}_2$	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	

LOGIC SYMBOL

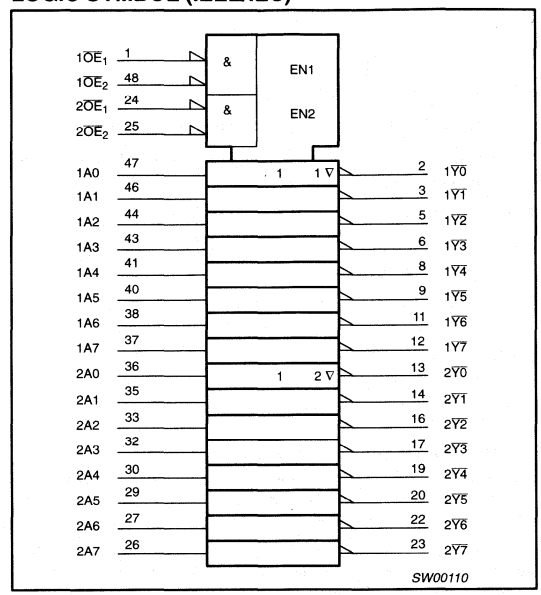


FUNCTION TABLE

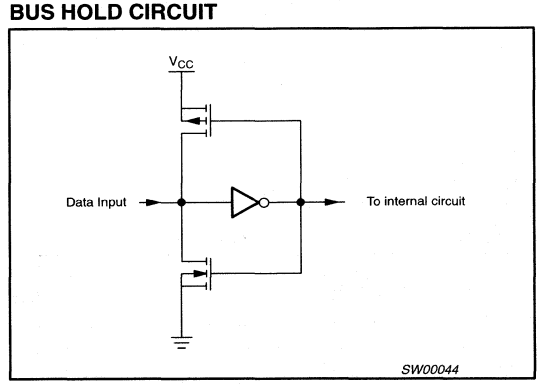
INPUTS			OUTPUT
$n\overline{OE}_1$	$n\overline{OE}_2$	nAn	nYn
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance)		3.0	3.6	
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range	For data input pins	0	V_{CC}	V
	DC Input voltage range	For control pins	0	5.5	
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	V_I < 0	–50	mA
V_I	DC input voltage	For control pins and data inputs of ALVC parts[2]	–0.5 to +5.5	V
		For data inputs of ALVCH parts[2]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	V_O > V_{CC} or V_O < 0	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink SO (SSOP) –plastic mini-pack (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V		V_{CC}			V
		V_{CC} = 2.3 to 2.7V		1.7			
		V_{CC} = 2.7 to 3.6V		2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V				GND	V
		V_{CC} = 2.3 to 2.7V				0.7	
		V_{CC} = 2.7 to 3.6V				0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –1mA		V_{CC} – 0.3			V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –8mA		V_{CC} – 0.5			
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA		V_{CC} – 0.5			
		V_{CC} = 2.3/3.0V; V_I = V_{IH} or V_{IL}; I_O = –100µA		V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA		V_{CC} – 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 1mA				0.40	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 8mA				0.60	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA				0.40	
		V_{CC} = 2.3/3.0V; V_I = V_{IH} or V_{IL}; I_O = 100µA				0.20	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA				0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND	Control pins		±0.1	±5	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Data input pins		±0.1	±5	
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; V_I = V_{CC} or GND			±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			0.1	±10	µA
	3-State output OFF-state current	V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND			0.1	±5	
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; V_I = V_{CC} or GND; I_O = 0			0.2	40	µA
	Quiescent supply current	V_{CC} = 2.7V; V_I = V_{CC} or GND; I_O = 0			0.2	20	
ΔI_{CC}	Additional quiescent supply current per control pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0			5	500	µA
	Additional quiescent supply current per data I/O pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} –0.6V; I_O = 0			150	750	
IBHL	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V		45			µA
		V_{CC} = 3.0V; V_I = 0.8V		75			
IBHH	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V		–45			µA
		V_{CC} = 3.0V; V_I = 2.0V		–75			
IBHLO	Bus hold LOW overdrive current	V_{CC} = 2.7V		300			µA
		V_{CC} = 3.6V		450			
IBHHO	Bus hold HIGH overdrive current	V_{CC} = 2.7V		–300			µA
		V_{CC} = 3.6V		–450			

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.0 ± 0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	TYP	MAX	
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	4		1.8	3.0	2.1	3.6	ns
t_{PZH}/t_{PZL}	3-State output enable time 1$\overline{OE}$n to 1Yn; 2$\overline{OE}$n to 2Yn	5, 6		2.1	3.8	2.9	4.7	ns
t_{PHZ}/t_{PLZ}	3-State output disable time 1$\overline{OE}$n to 1Yn; 2$\overline{OE}$n to 2Yn	5, 6		2.7	4.1	3.2	4.5	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE AND V_{CC} < 2.3V

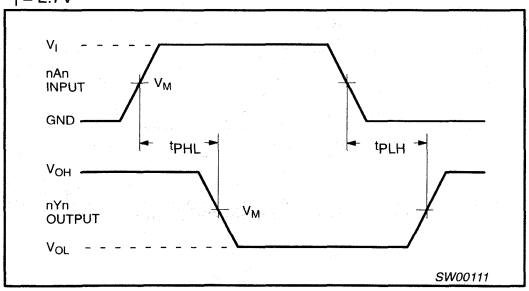
GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 2.3 to 2.7V			V_{CC} = 1.8V	V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	TYP	MAX	
t_{PHL}/t_{PLH}	Propagation delay 1An to 1Yn; 2An to 2Yn	4		1.8	3.2	3.1	6.0	ns
t_{PZH}/t_{PZL}	3-State output enable time 1$\overline{OE}$n to 1Yn; 2$\overline{OE}$n to 2Yn	5, 6		2.5	4.4	4.3	8.9	ns
t_{PHZ}/t_{PLZ}	3-State output disable time 1$\overline{OE}$n to 1Yn; 2$\overline{OE}$n to 2Yn	5, 6		2.2	3.8	3.6	6.4	ns

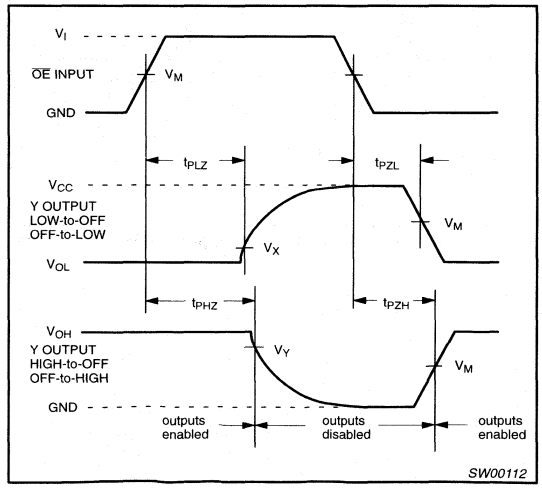
NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

V_M = 1.5 V
$V_X = V_{OL}$ + 0.3V
$V_Y = V_{OH}$ −0.3V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = 2.7V

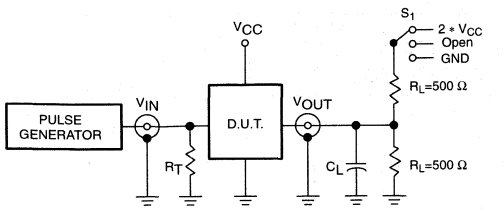


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

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Waveform 3. Load circuitry for switching times

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

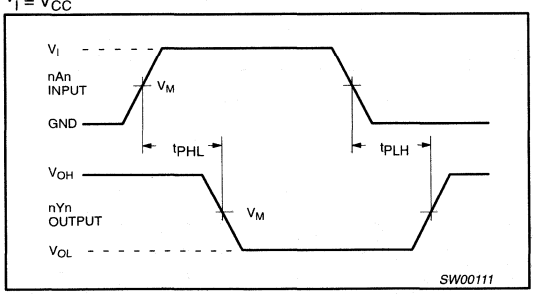
$V_M = 0.5 * V_{CC}$

$V_X = V_{OL} + 0.15V$

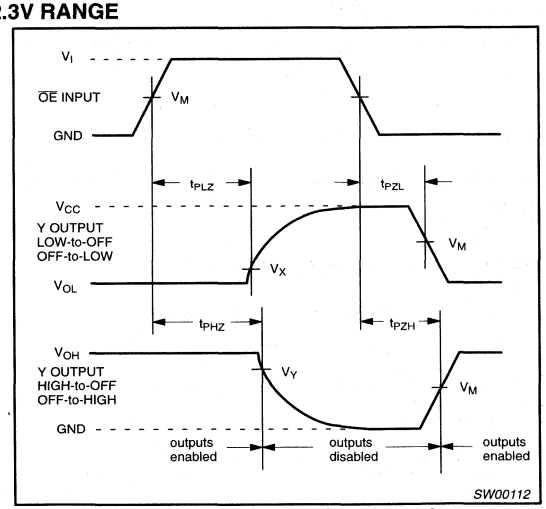
$V_Y = V_{OH} – 0.15V$

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_I = V_{CC}$

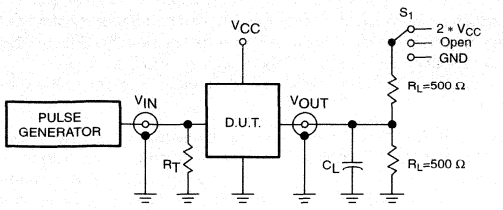


Waveform 4. Input (An) to output (Yn) propagation delay times



Waveform 5. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 6. Load circuitry for switching times

16-bit D-type registered transceiver (3-State) 74ALVCH16543

FEATURES

- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- 16-bit transceiver with D-type latch
- Combines 74ALVCH16245 and 74ALVCH16373 type functions in one chip
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Current drive ± 24 mA at 3.0 V
- All inputs have bushold circuitry

DESCRIPTION

The 74ALVCH16543 is a dual octal registered transceiver. Each section contains two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and output enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control in either direction of the data flow.

The 74ALVCH16543 contains two sections each consisting of two sets of eight D-type latches with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable ($n\overline{E}_{AB}$, where n equals 1 or 2) input must be LOW in order to enter data from nA0-nA7 or take data from nB0-nB7, as indicated in the function table. With $n\overline{E}_{AB}$ LOW, a LOW signal on the A-to-B latch enable ($n\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $n\overline{LE}_{AB}$ signal stores the A data into the latches. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both LOW, the 3-State B output buffers are active and display the data present at the output of the A latches. Similarly, the $\overline{E}_{BA}$, $\overline{LE}_{BA}$ and $\overline{OE}_{BA}$ signals control the data flow from B-to-A.

To ensure the high impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nAx to nBx, nBx to nAx	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		3.0 3.2	ns
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Outputs enabled	22	pF
			Outputs disabled	6	

NOTES:

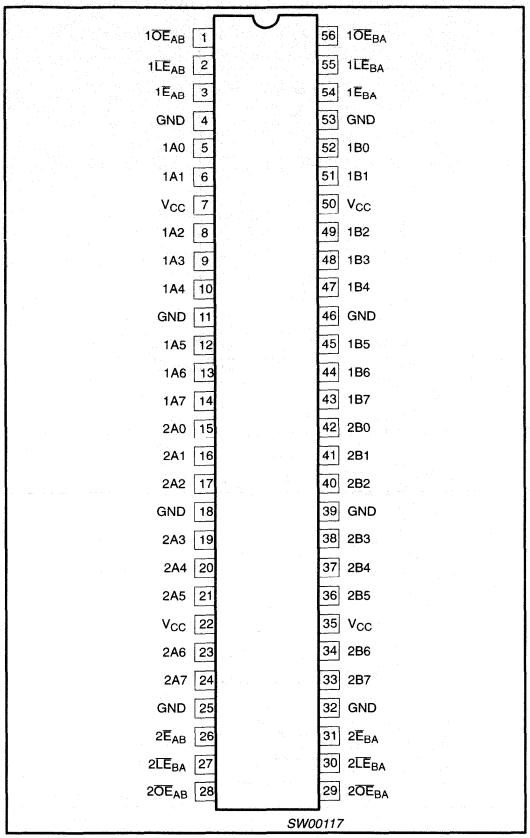
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74ALVCH16543 DGG	ACH16543 DGG	SOT364-1

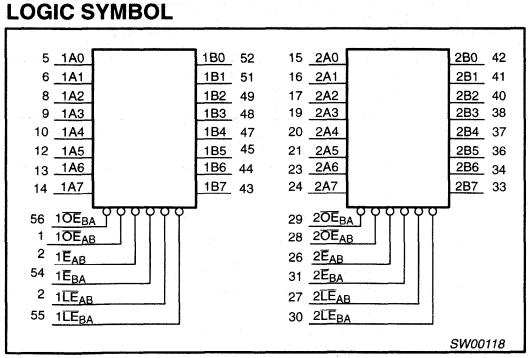
16-bit D-type registered transceiver (3-State) 74ALVCH16543

PIN CONFIGURATION



SW00117

LOGIC SYMBOL

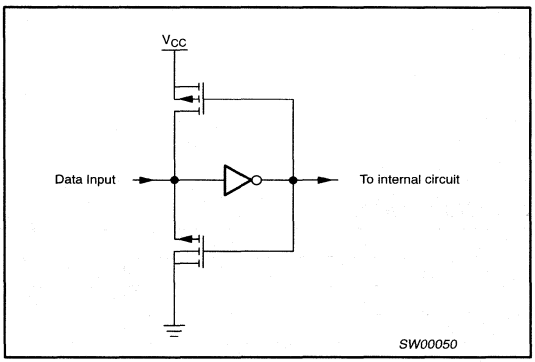


SW00118

PIN DESCRIPTION

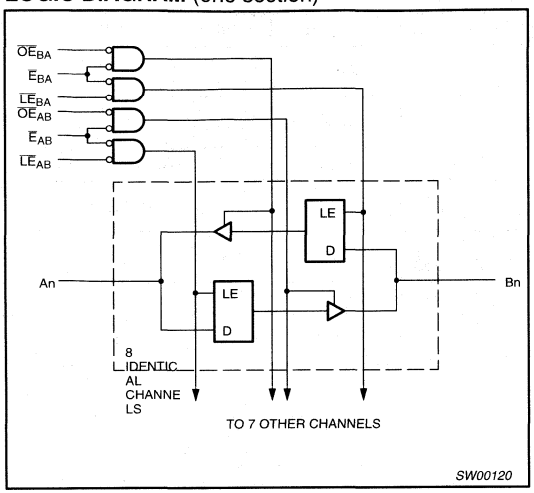
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	n$\overline{OE}_{AB}$	Output enable A-to-B for register 1 or 2
2, 27	n$\overline{LE}_{AB}$	Latch enable A-to-B for register 1 or 2
3, 26	n$\overline{E}_{AB}$	A-to-B enable for register 1 or 2
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	1A data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2B0 to 2B7	2B data inputs/outputs
29, 56	n$\overline{OE}_{BA}$	Output enable B-to-A for register 1 or 2
30, 55	n$\overline{LE}_{BA}$	Latch enable B-to-A for register 1 or 2
31, 54	n$\overline{E}_{BA}$	B-to-A enable for register 1 or 2
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	2B data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	1B data inputs/outputs

BUS HOLD CIRCUIT

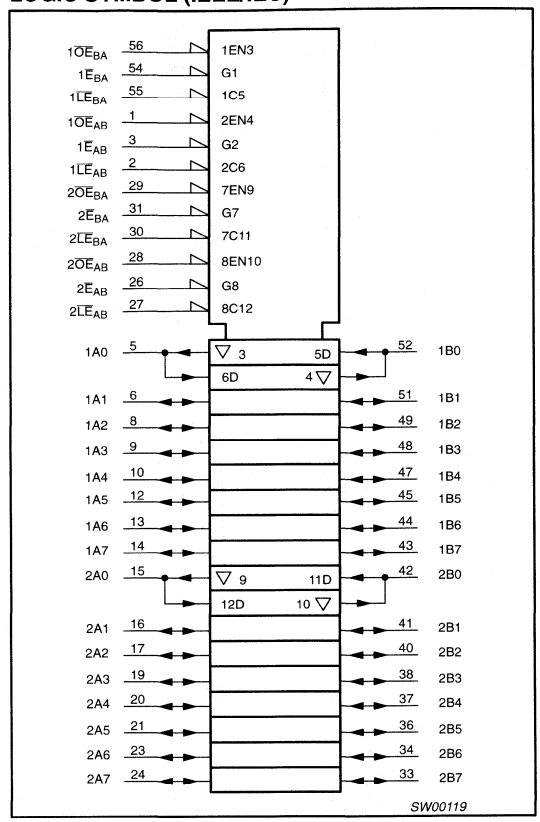


SW00050

LOGIC DIAGRAM (one section)



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS nBx, nAx	STATUS
$n\overline{OE}_{XX}$	$n\overline{E}_{XX}$	$n\overline{LE}_{XX}$	nBx, nAx		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$ or $\overline{E}_{BA}$
l = LOW state must be present one setup time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$ or $\overline{E}_{BA}$
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
Z = High impedance "off" state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ± 0.2V			
			MIN	TYP	MAX	
t_{PLH}/t_{PHL}	Propagation delay nAx to nBx, nBx to nAx	1, 4	1.0	2.2	5.1	ns
t_{PLH}/t_{PHL}	Propagation delay $n\overline{LE}_{BA}$ to nAx, $n\overline{LE}_{AB}$ to nBx	1, 4	1.0	2.6	6.5	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{E}_{BA}$ to nAx, $n\overline{E}_{AB}$ to nBx	2, 4	1.0	2.5	7.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{E}_{BA}$ to nAx, $n\overline{E}_{AB}$ to nBx	2, 4	1.3	2.3	6.1	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_{BA}$ to nAx, $n\overline{OE}_{AB}$ to nBx	1, 4	1.0	2.5	6.8	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_{BA}$ to nAx, $n\overline{OE}_{AB}$ to nBx	1, 4	1.0	2.2	5.7	ns
t_W	Pulse width $\overline{LE}$, $\overline{E}$ LOW	3, 4	3.3	1.5		ns
t_{SU}	Set up time data before $\overline{LE}\uparrow$, $\overline{E}\uparrow$	3, 4	1.2	0.7		ns
t_h	Hold time data before $\overline{LE}\uparrow$, $\overline{E}\uparrow$	3, 4	1.2	0.0		ns

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAx to nBx, nBx to nAx	1, 4	1.0	2.1	4.3		2.5	4.8	ns
t_{PHL}/t_{PLH}	Propagation delay $n\overline{LE}_{BA}$ to nAx, $n\overline{LE}_{AB}$ to nBx	1, 4	1.1	2.2	5		3.1	6.2	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{E}_{BA}$ to nAx, $n\overline{E}_{AB}$ to nBx	2, 4	1.0	2.1	5.6		3.0	6.9	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{E}_{BA}$ to nAx, $n\overline{E}_{AB}$ to nBx	2, 4	1.5	2.9	5.1		3.1	6.2	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_{BA}$ to nAx, $n\overline{OE}_{AB}$ to nBx	2, 4	1.0	2.1	5.3		2.9	6.3	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_{BA}$ to nAx, $n\overline{OE}_{AB}$ to nBx	2, 4	1.1	2.9	4.6		3.1	4.8	ns
t_W	Pulse width $\overline{LE}$, $\overline{E}$ LOW	3, 4	3.3	1.5		3.3	1.5		ns
t_{SU}	Set up time data before $\overline{LE}\uparrow$, $\overline{E}\uparrow$	3, 4	1.2	0.8		1.5	0.9		ns
t_h	Hold time data before $\overline{LE}\uparrow$, $\overline{E}\uparrow$	3, 4	1.3	0.0		0.8	0.0		ns

NOTES:

1. All typical values are at T_{amb} = 25°C.

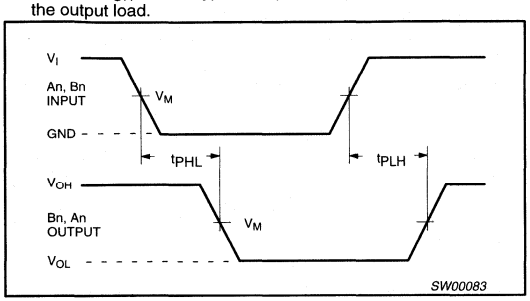
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

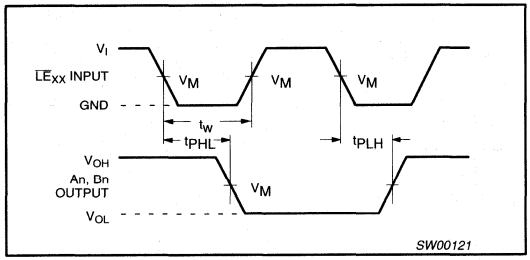
1. V_M = 0.5 V
2. $V_X = V_{OL}$ + 0.15V
3. $V_Y = V_{OH}$ – 0.15V
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

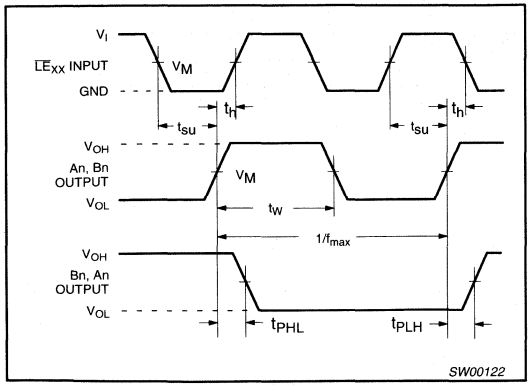
1. V_M = 1.5 V
2. $V_X = V_{OL}$ + 0.3V
3. $V_Y = V_{OH}$ – 0.3V
4. V_I = 2.7 V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



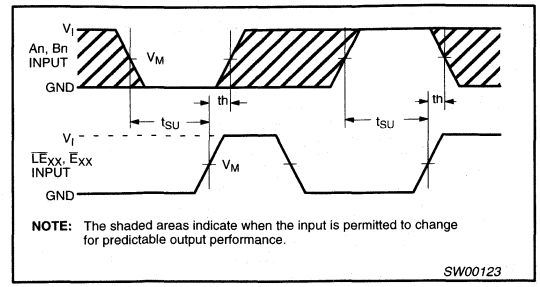
Waveform 1. Input (Dn) to output (Qn) propagation times



Waveform 2. Latch enable input ($\overline{LE}_{XX}$) pulse width, the latch enable input to output (Qn) propagation delay times

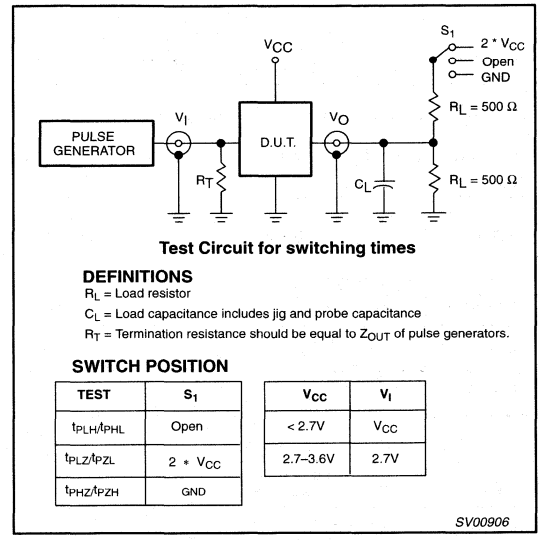


Waveform 3. 3-State enable and disable times



Waveform 4. Data set-up and hold times for the Dn input to the LE input

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Load circuitry for switching times

18-bit universal bus transceiver (3-State) 74ALVCH16600

FEATURES

- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- All inputs have bus hold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce

DESCRIPTION

The 74ALVCH16600 is a high-performance CMOS product designed for V_{CC} operation at 2.5V and 3.3V with I/O compatibility up to 5V. This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($\overline{OE}_{AB}$ and $\overline{OE}_{BA}$), latch enable (LE_{AB} and LE_{BA}), and clock ($\overline{CP}_{AB}$ and $\overline{CP}_{BA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LE_{AB} is High. When LE_{AB} is Low, the A data is latched if $\overline{CP}_{AB}$ is held at a High or Low logic level. If LE_{AB} is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of $\overline{CP}_{AB}$. When $\overline{OE}_{AB}$ is Low, the outputs are active. When $\overline{OE}_{AB}$ is High, the outputs are in the high-impedance state. The High clock can be controlled with the clock-enable inputs ($\overline{CE}_{BA}/\overline{CE}_{AB}$).

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OE}_{BA}$, LE_{BA} and $\overline{CP}_{BA}$.

To ensure the high impedance state during power up or power down, $\overline{OE}_{BA}$ should be tied to V_{CC} through a pullup resistor and OE_{AB} should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An LE_{AB} to Bn; LE_{BA} to An CP_{AB} to Bn; CP_{BA} to An	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		3.0 3.2	ns
C_I	Input capacitance			5.0	pF
$C_{I/O}$	Input/Output capacitance			10	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Outputs enabled	22	pF
			Outputs disabled		

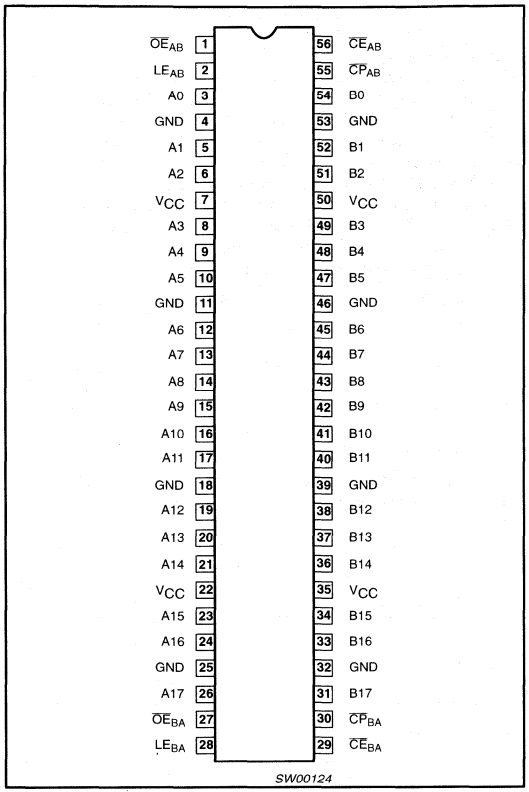
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16600 DGG	ACH16600 DGG	SOT364-1

PIN CONFIGURATION

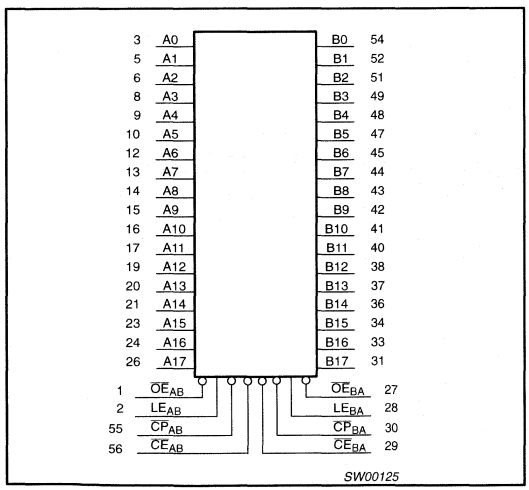


SW00124

PIN DESCRIPTION

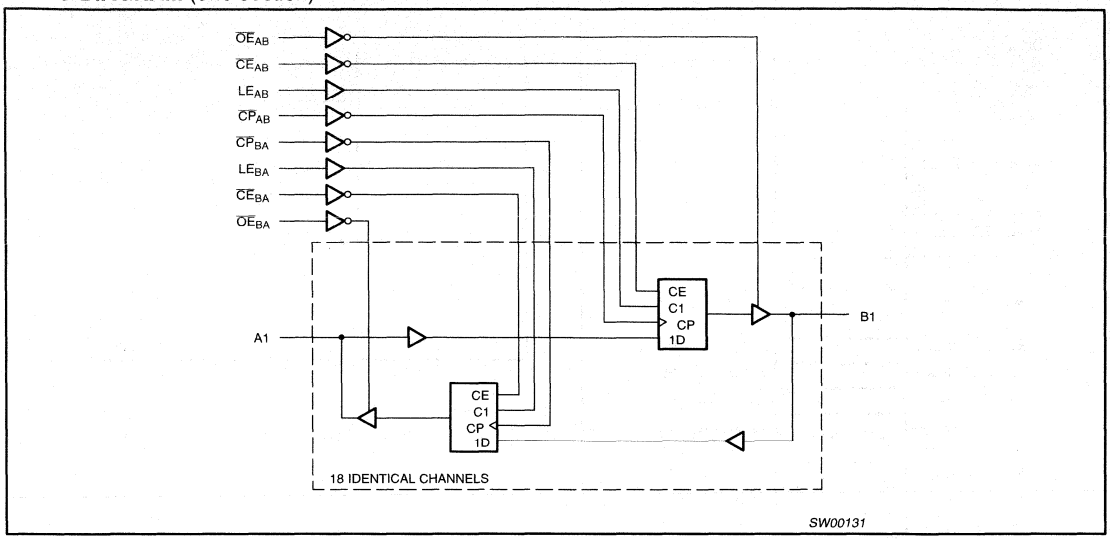
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0 to A17	Data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
29	$\overline{CE}_{BA}$	Clock enable B-to-A
30	$\overline{CP}_{BA}$	Clock input B-to-A
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0 to B17	Data inputs/outputs
55	$\overline{CP}_{AB}$	Clock input A-to-B
56	$\overline{CE}_{AB}$	Clock enable A-to-B

LOGIC SYMBOL



SW00125

LOGIC DIAGRAM (one section)

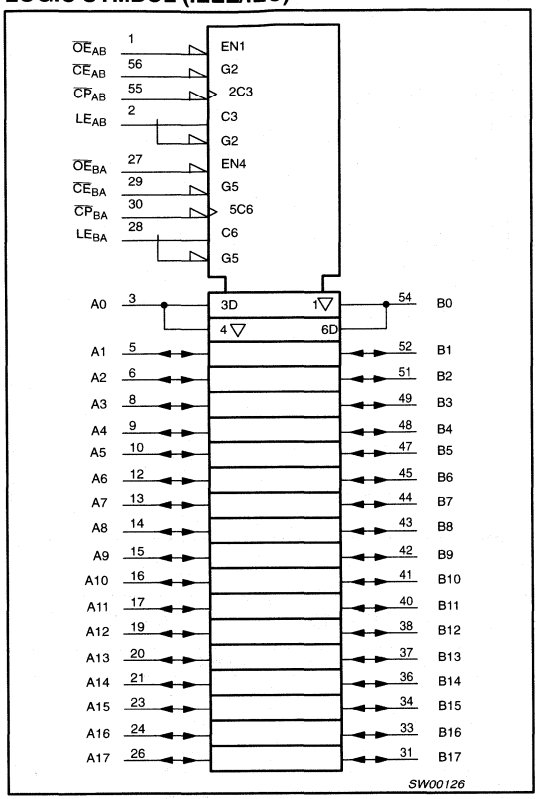


FUNCTION TABLE

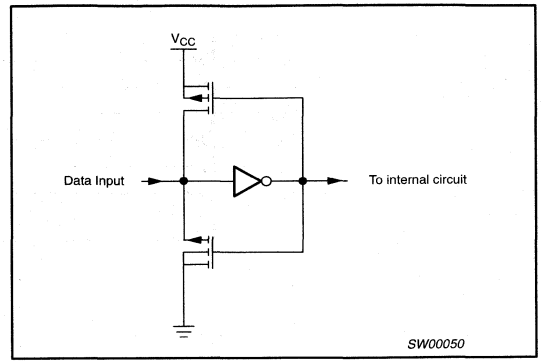
INPUTS					OUTPUTS	STATUS
$\overline{CE}_{XX}$	$\overline{OE}_{XX}$	LE_{XX}	$\overline{CP}_{XX}$	DATA		
X	H	X	X	X	Z	Disabled
X X	L L	H H	X X	H L	H L	Transparent
H H	L L	L L	X X	X X	NC NC1	Hold
L L	L L	L L	↓ ↓	h l	Z Z	Disabled + latch
L L	L L	L L	↓ ↓	h l	H L	Latch + display
L L	L L	L L	H L	X X	NC NC1	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of $\overline{CP}_{XX}$
l = LOW state must be present one setup time before the LOW-to-HIGH transition of $\overline{CP}_{XX}$
X = Don't care
↓ = HIGH-to-LOW level transition
NC = No change
NC1 = No change provided that $\overline{CP}_{XX}$ was LOW before LE_{XX} went LOW
Z = High impedance "off" state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER		WAVEFORM	LIMITS			UNIT
				V_{CC} = 2.5V ± 0.2V			
				MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay An to Bn, Bn to An		1	1		5.1	ns
t_{PHL} t_{PLH}	Propagation delay LE_{BA} to An, LE_{AB} to Bn		2	1		5.9	ns
	Propagation delay CP_{BA} to An, CP_{AB} to Bn			1		7.3	
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An, OE_{AB} to Bn		3	1		6.5	ns
t_{PHZ} t_{PLZ}	3-State output disable time OE_{BA} to An, OE_{AB} to Bn		3	1		5.1	ns
t_W	LE pulse width LE_{AB} or LE_{BA} HIGH		2	3.3			ns
	LE pulse width CP_{AB} or CP_{BA} HIGH or LOW			3.3			
t_{SU}	Set-up time An before CP_{AB} ↑ or Bn before $\overline{CP}_{AB}$ ↑		4	1.3			ns
	Set-up time An before LE_{AB} ↓ or Bn before LE_{AB} ↓	CP HIGH		1.2			
		CP LOW		1.8			
	Set-up time CE_{AB} before CP_{AB} ↑ or CE_{BA} before CP_{AB}↑		4	0.7			ns
t_h	Hold time An after CP_{AB} ↑ or Bn before $\overline{CP}_{AB}$ ↑		4	1.5			ns
	Hold time An before LE_{AB} ↓ or Bn before LE_{AB} ↓	CP HIGH	4	1.6			ns
		CP LOW		1.2			
	Hold time An after $\overline{CE}_{AB}$ ↑ or Bn before $\overline{CE}_{BA}$ ↑		4	1.4			ns
f_{MAX}	Maximum clock frequency			150			

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER		WAVEFORM	LIMITS						UNIT
				V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay An to Bn, Bn to An		1	1.0		4			4.7	ns
t_{PHL} t_{PLH}	Propagation delay LE_{BA} to An, LE_{AB} to Bn		2	1.0		4.8			5.5	ns
	Propagation delay CP_{BA} to An, CP_{AB} to Bn			1.3		5.7			6.8	
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An, OE_{AB} to Bn		3	1.1		5.2			6.3	ns
t_{PHZ} t_{PLZ}	3-State output disable time OE_{BA} to An, OE_{AB} to Bn		3	1.2		4.4			4.7	ns
t_W	LE pulse width LE_{AB} or LE_{BA} HIGH		4	3.3			3.3			ns
	LE pulse width CP_{AB} or CP_{BA} HIGH or LOW			3.3			3.3			
t_{SU}	Set-up time An before $CP_{AB}\uparrow$ or Bn before $CP_{AB}\uparrow$		4	1.2			1.3			ns
	Set-up time An before $LE_{AB}\downarrow$ or Bn before $LE_{AB}\downarrow$	CP HIGH		1.1			1.1			
		CP LOW		1.5			1.5			
	Set-up time CE_{AB} before $CP_{AB}\uparrow$ or CE_{BA} before $CP_{AB}\uparrow$		4	0.8			0.7			ns
t_h	Hold time An after $CP_{AB}\uparrow$ or Bn before $\overline{CP}_{AB}\uparrow$		4	1.5			1.8			ns
	Hold time An before $LE_{AB}\downarrow$ or Bn before $LE_{AB}\downarrow$	CP HIGH	4	1.6			1.9			ns
		CP LOW		1.3			1.6			
	Hold time An after $\overline{CE}_{AB}\uparrow$ or Bn before $\overline{CE}_{BA}\uparrow$		4	1.4			1.7			ns
f_{MAX}	Maximum clock frequency			150			150			

NOTES:

1. All typical values are at T_{amb} = 25°C.

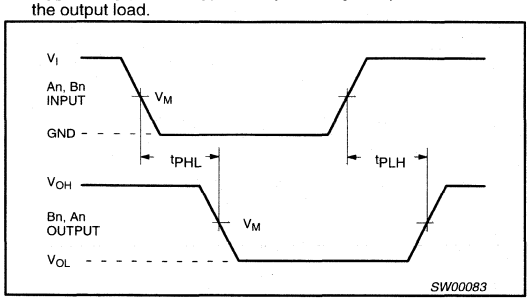
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

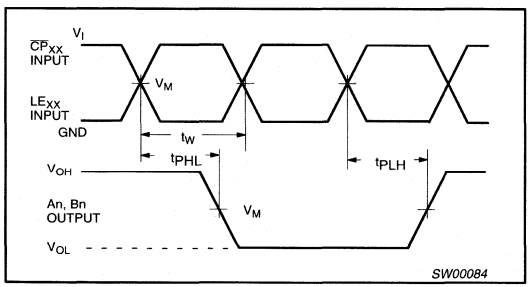
1. V_M = 0.5 V
2. $V_X = V_{OL}$ + 0.15V
3. $V_Y = V_{OH}$ − 0.15V
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

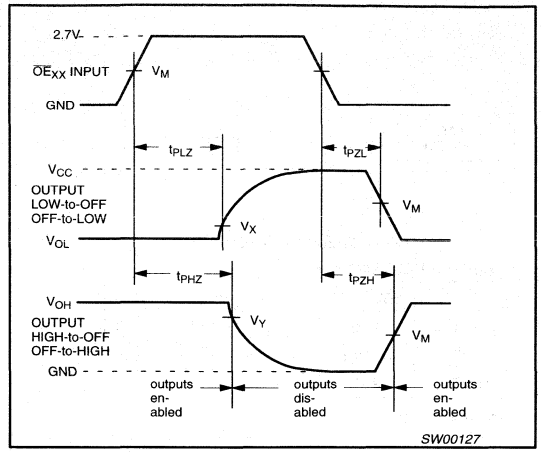
1. V_M = 1.5 V
2. $V_X = V_{OL}$ + 0.3V
3. $V_Y = V_{OH}$ − 0.3V
4. V_I = 2.7 V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



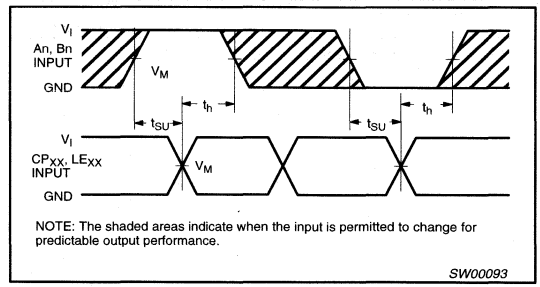
Waveform 1. Input (An, Bn) to output (Bn, An) propagation delay times



Waveform 2. Latch enable input (LE_{AB}, LE_{BA}) and clock pulse input ($\overline{CP}_{AB}$, $\overline{CP}_{BA}$) to output (An, Bn) propagation delays and latch enable pulse width

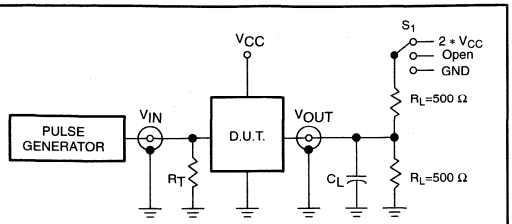


Waveform 3. 3-State enable and disable times



Waveform 4. Data set-up and hold times for the An and Bn inputs to the LE_{AB}, LE_{BA}, $\overline{CP}_{AB}$ and $\overline{CP}_{BA}$ inputs

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Load circuitry for switching times

18-bit universal bus transceiver (3-State) 74ALVCH16601

FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- Current drive ± 24 mA at 3.0 V
- All inputs have bus hold circuitry
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16601 is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($\overline{OE}_{AB}$ and $\overline{OE}_{BA}$), latch enable (LE_{AB} and LE_{BA}), and clock (CP_{AB} and CP_{BA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LE_{AB} is High. When LE_{AB} is Low, the A data is latched if CP_{AB} is held at a High or Low logic level. If LE_{AB} is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CP_{AB}. When $\overline{OE}_{AB}$ is Low, the outputs are active. When $\overline{OE}_{AB}$ is High, the outputs are in the high-impedance state. The clocks can be controlled with the clock-enable inputs ($\overline{CE}_{BA}$/$\overline{CE}_{AB}$).

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OE}_{BA}$, LE_{BA} and CP_{BA}.

To ensure the high impedance state during power up or power down, $\overline{OE}_{BA}$ should be tied to V_{CC} through a pullup resistor and OE_{AB} should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Bn; Bn to An LE_{AB} to Bn; LE_{BA} to An CP_{AB} to Bn; CP_{BA} to An	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		3.0 3.4	ns
C_I	Input capacitance			5.0	pF
$C_{I/O}$	Input/Output capacitance			10	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Outputs enabled	22	pF
			Outputs disabled		

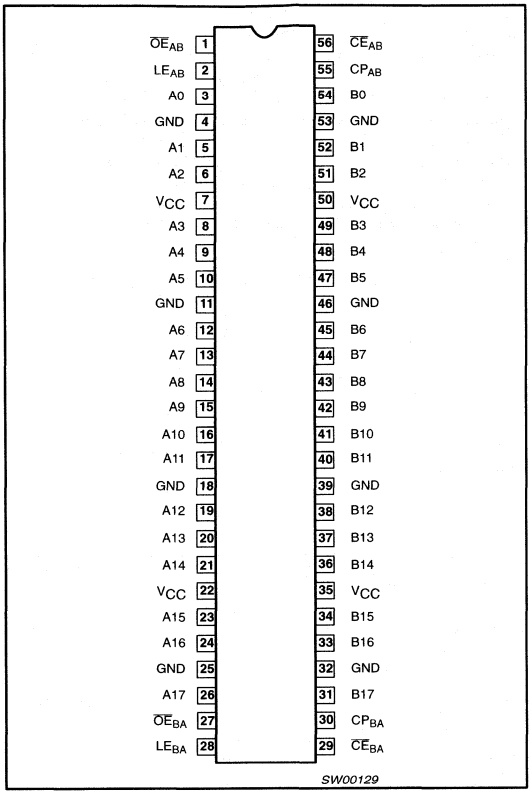
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16601 DGG	ACH16601 DGG	SOT364-1

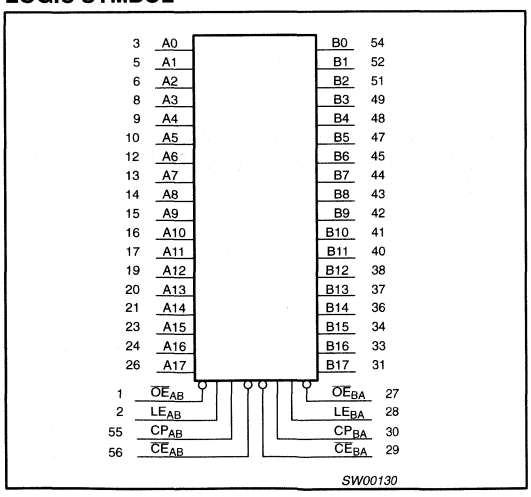
PIN CONFIGURATION



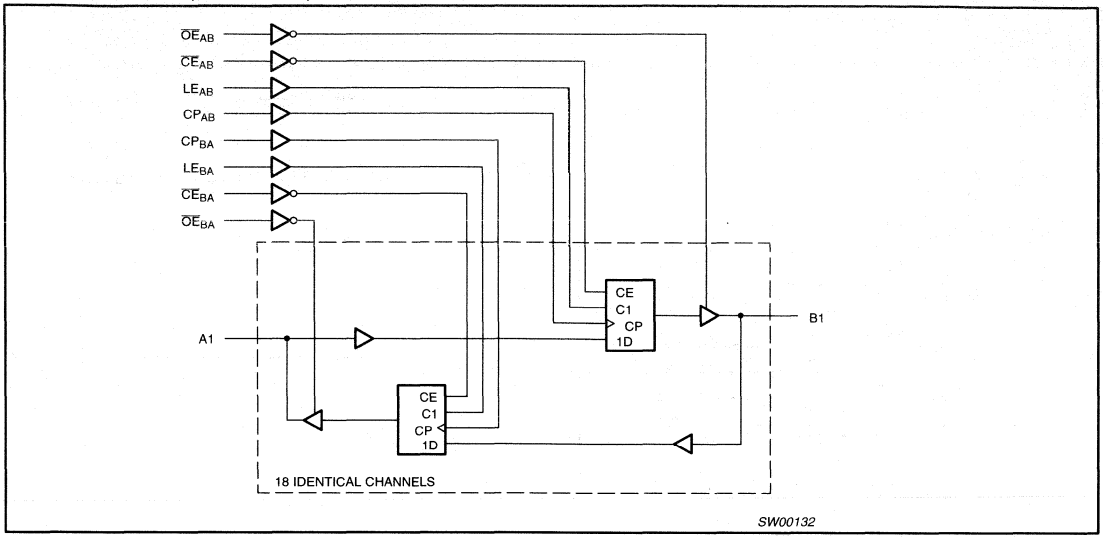
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_{AB}$	Output enable A-to-B
2	LE_{AB}	Latch enable A-to-B
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0 to A17	Data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}_{BA}$	Output enable B-to-A
28	LE_{BA}	Latch enable B-to-A
29	$\overline{CE}_{BA}$	Clock enable B-to-A
30	CP_{BA}	Clock input B-to-A
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0 to B17	Data inputs/outputs
55	CP_{AB}	Clock input A-to-B
56	$\overline{CE}_{AB}$	Clock enable A-to-B

LOGIC SYMBOL



LOGIC DIAGRAM (one section)

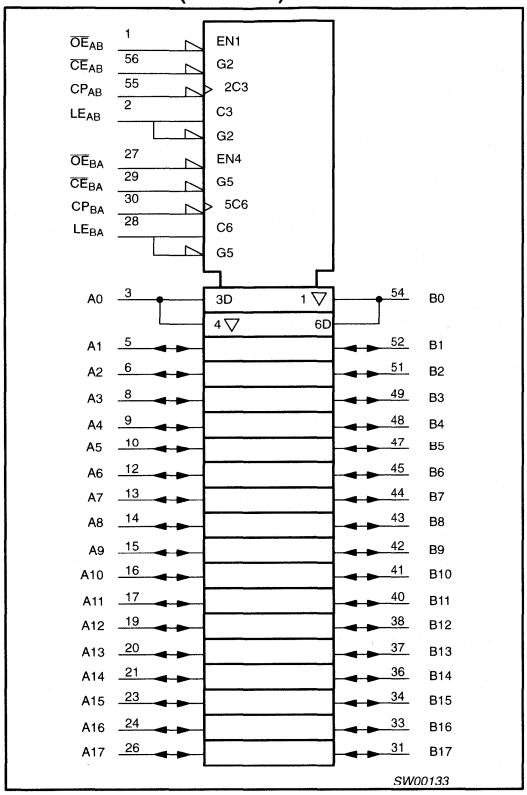


FUNCTION TABLE

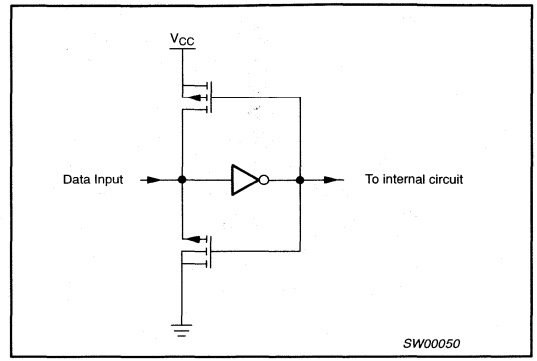
INPUTS					OUTPUTS	STATUS
$\overline{CE}_{XX}$	$\overline{OE}_{XX}$	LE_{XX}	CP_{XX}	DATA		
X	H	X	X	X	Z	Disabled
X X	L L	H H	X X	H L	H L	Transparent
H H	L L	L L	X X	X X	NC NC1	Hold
L L	L L	L L	↑ ↑	h l	Z Z	Disabled + latch
L L	L L	L L	↑ ↑	h l	H L	Latch + display
L L	L L	L L	L H	X X	NC NC1	Hold

XX = AB for A-to-B direction, BA for B-to-A direction
H = HIGH voltage level
L = LOW voltage level
h = HIGH state must be present one setup time before the LOW-to-HIGH transition of CP_{XX}
l = LOW state must be present one setup time before the LOW-to-HIGH transition of CP_{XX}
X = Don't care
↑ = LOW-to-HIGH level transition
NC = No change
NC1 = No change provided that CP_{XX} was LOW before LE_{XX} went LOW
Z = High impedance "off" state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	V_I < 0	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	V_O > V_{CC} or V_O < 0	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER		WAVEFORM	LIMITS			UNIT
				V_{CC} = 2.5V ± 0.2V			
				MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay An to Bn, Bn to An		1	1	2.7	4	ns
t_{PHL} t_{PLH}	Propagation delay LE_{BA} to An, LE_{AB} to Bn		2	1	2.7	4.6	ns
	Propagation delay CP_{BA} to An, CP_{AB} to Bn			1.2	2.7	5.2	
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An, OE_{AB} to Bn		3	1.1	2.8	5.3	ns
t_{PHZ} t_{PLZ}	3-State output disable time OE_{BA} to An, OE_{AB} to Bn		3	1.4	2.3	4.9	ns
t_W	LE pulse width LE_{AB} or LE_{BA} HIGH		2	3.3	1.0		ns
	LE pulse width CP_{AB} or CP_{BA} HIGH or LOW			3.3	0.7		
t_{SU}	Set-up time An before CP_{AB} ↑ or Bn before $\overline{CP}_{AB}$ ↑		4	0.7	0.2		ns
	Set-up time An before LE_{AB} ↓ or Bn before LE_{AB} ↓	CP HIGH		2.0	0.1		
		CP LOW		1.3	0.1		
	Set-up time CE_{AB} before CP_{AB} ↑ or CE_{BA} before CP_{AB}↑		4	2.0	0.2		ns
t_h	Hold time An after CP_{AB} ↑ or Bn before $\overline{CP}_{AB}$ ↑		4	0.7	0.0		ns
	Hold time An before LE_{AB} ↓ or Bn before LE_{AB} ↓	CP HIGH	4	1.3	0.1		ns
		CP LOW		1.7	0.4		
	Hold time An after $\overline{CE}_{AB}$ ↑ or Bn before $\overline{CE}_{BA}$ ↑		4	0.3	0.1		ns
f_{MAX}	Maximum clock frequency			150	340		

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER		WAVEFORM	LIMITS						UNIT
				V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL} t_{PLH}	Propagation delay An to Bn, Bn to An		1	1.0	3.0	4.1	1.0	3.3	4.6	ns
t_{PHL} t_{PLH}	Propagation delay LE_{BA} to An, LE_{AB} to Bn		2	1.0	3.2	4.7	1.0	3.5	5.3	ns
	Propagation delay CP_{BA} to An, CP_{AB} to Bn			1.0	3.4	5.0	1.0	3.7	5.8	
t_{PZH} t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An, OE_{AB} to Bn		3	1.0	3.5	5.2	1.0	4.5	6.1	ns
t_{PHZ} t_{PLZ}	3-State output disable time OE_{BA} to An, OE_{AB} to Bn		3	1.0	3.1	4.4	1.0	3.2	4.8	ns
t_W	LE pulse width LE_{AB} or LE_{BA} HIGH		2	3.3	0.6		3.3	0.6		ns
	LE pulse width CP_{AB} or CP_{BA} HIGH or LOW			3.3	0.7		3.3	1.2		
t_{SU}	Set-up time An before $CP_{AB}\uparrow$ or Bn before $CP_{AB}\uparrow$		4	2.1	0.1		2.4	0.2		ns
	Set-up time An before $LE_{AB}\downarrow$ or Bn before $LE_{AB}\downarrow$	CP HIGH		1.6	0.0		1.6	0.0		
		CP LOW		1.1	0.0		1.2	0.0		
	Set-up time CE_{AB} before $CP_{AB}\uparrow$ or CE_{BA} before $CP_{AB}\uparrow$		4	1.7	0.2		2.0	0.2		ns
t_h	Hold time An after $CP_{AB}\uparrow$ or Bn before $\overline{CP}_{AB}\uparrow$		4	0.8	0.1		0.7	0.1		ns
	Hold time An before $LE_{AB}\downarrow$ or Bn before $LE_{AB}\downarrow$	CP HIGH	4	1.4	0.4		1.6	0.6		ns
		CP LOW		1.7	0.4		0.2	0.6		
	Hold time An after $\overline{CE}_{AB}\uparrow$ or Bn before $\overline{CE}_{BA}\uparrow$		4	0.6	0.2		0.5	0.2		ns
f_{MAX}	Maximum clock frequency			150	370		150	330		

NOTES:

1. All typical values are at T_{amb} = 25°C.

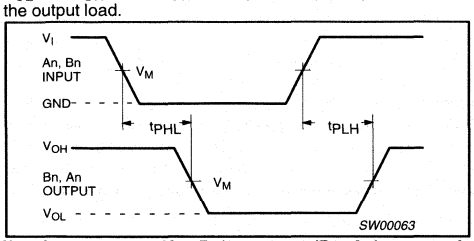
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

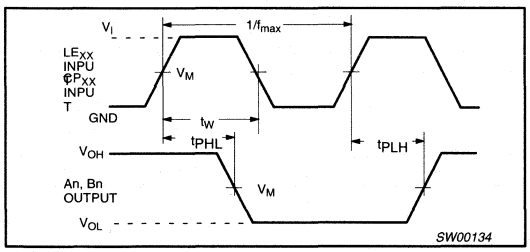
1. $V_M = 0.5$ V
2. $V_X = V_{OL} + 0.15$V
3. $V_Y = V_{OH} - 0.15$V
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

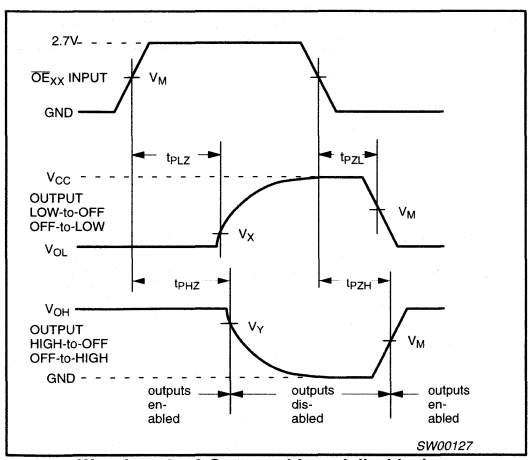
1. $V_M = 1.5$ V
2. $V_X = V_{OL} + 0.3$V
3. $V_Y = V_{OH} - 0.3$V
4. $V_I = 2.7$ V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



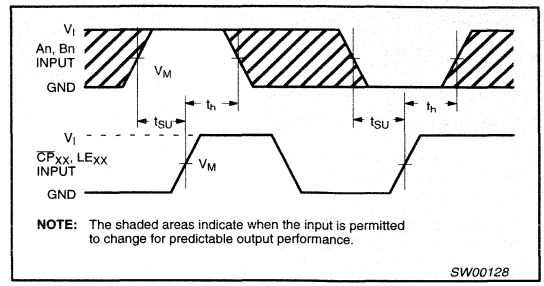
Waveform 1. Input (An, Bn) to output (Bn, An) propagation delays



Waveform 2. Latch enable input (E_{AB}, LE_{BA}) and clock pulse input (CP_{AB}, CP_{BA}) to output propagation delays and their pulse width

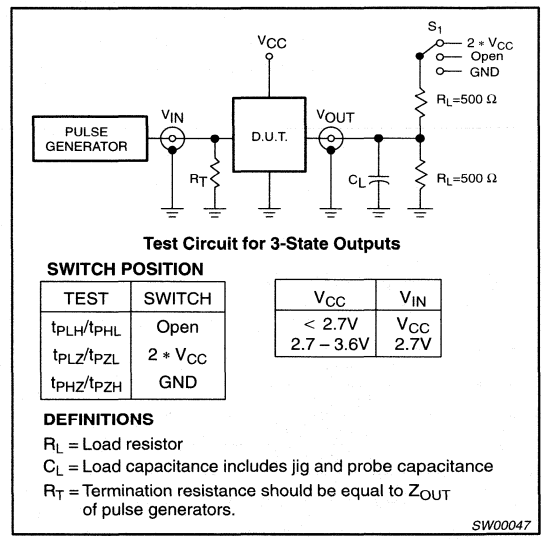


Waveform 3. 3-State enable and disable times



Waveform 4. Data set-up and hold times for the An and Bn inputs to the LE_{AB}, LE_{BA}, CP_{AB} and CP_{BA} inputs

TEST CIRCUIT



Load circuitry for switching times

16-bit transceiver with dual enable (3-State) 74ALVCH16623

FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ pin-out architecture
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16623 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVCH16623 is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

This 16-bit bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (nOE_{AB}, $n\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of nOE_{AB} and $n\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when all control inputs are enabled and all other data sources to the four sets of the bus lines are at high impedance OFF-state, all sets of bus lines will remain at their last states. The 8-bit codes appearing on the two double sets of buses will be complementary. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

To ensure the high impedance state during power up or power down, $\overline{OE}_{BA}$ should be tied to V_{CC} through a pullup resistor and OE_{AB} should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nAx to nBx; nBx to nAx	V_{CC} = 2.5V, CL = 30pF V_{CC} = 3.3V, CL = 50pF		2 1.9	ns
C_I	Input capacitance			3.0	pF
$C_{I/O}$	Input/output capacitance			10.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	Outputs enabled	35	pF
			Outputs disabled	5	

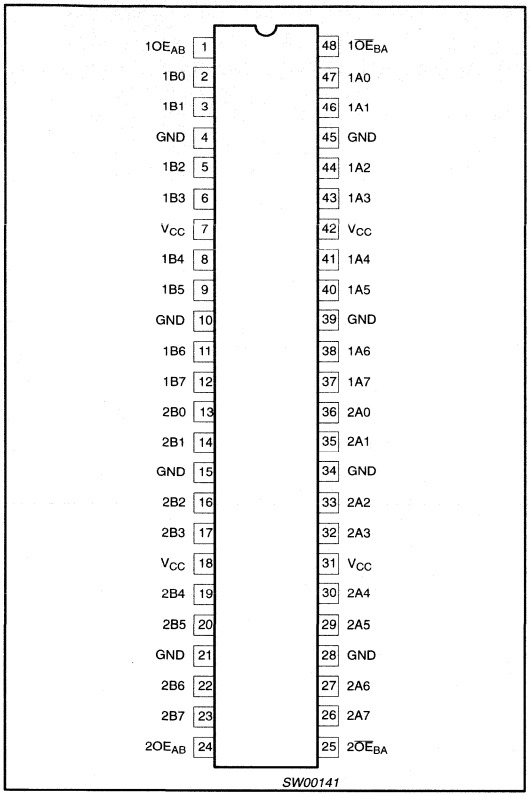
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

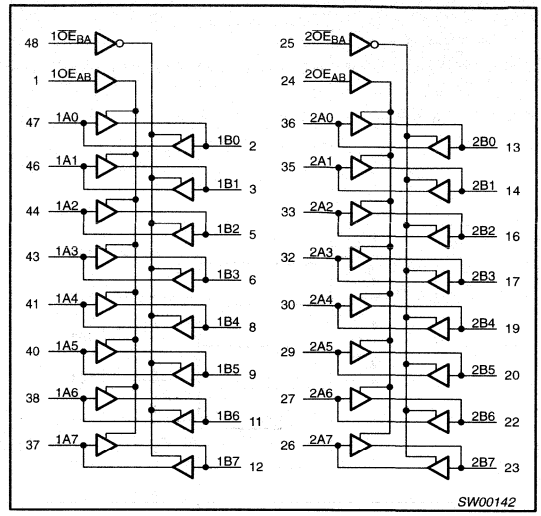
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16623 DGG	ACH16623 DGG	SOT362-1

PIN CONFIGURATION



LOGIC SYMBOL



FUNCTION TABLE

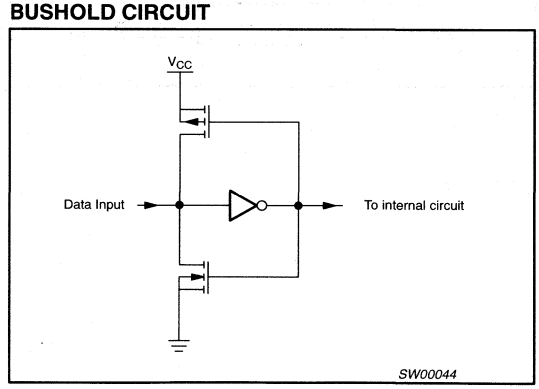
INPUTS		INPUTS/OUTPUTS	
nOEAB	**nOEBA**	**nAx**	**nBn**
L	L	A = B	inputs
H	H	inputs	B = A
L	H	Z	Z
H	L	A = B	B = A

H = HIGH voltage level
L = LOW voltage level
Z = high impedance "OFF"-state

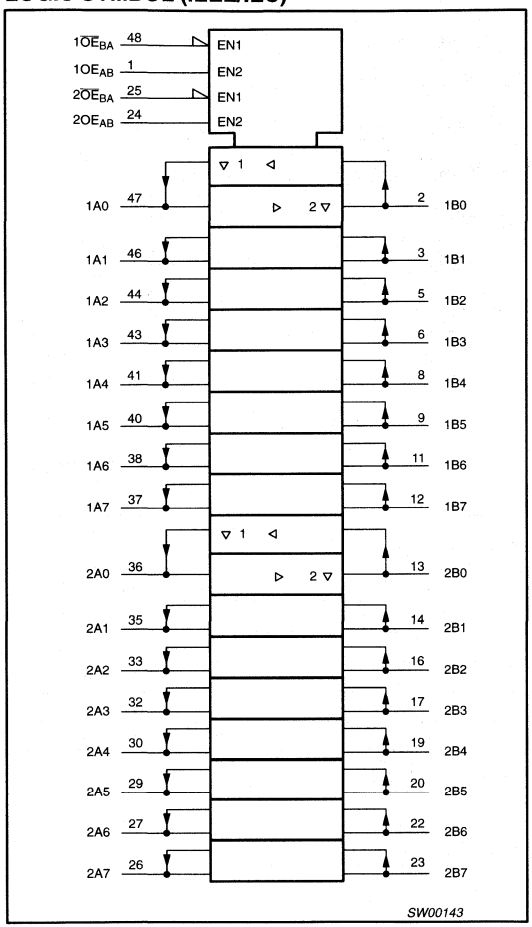
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1OE_{AB}$	Output enable input (active HIGH)
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	Data inputs/outputs
24	$2OE_{AB}$	Output enable input (active HIGH)
25	$2\overline{OE}_{BA}$	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	Data inputs/outputs
48	$1\overline{OE}_{BA}$	Output enable input (active LOW)

BUSHOLD CIRCUIT



LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP[1]	MAX	
t_{PHL} t_{PLH}	Propagation delay nAx to nBn; nBn to nAx	1,4	1.0	2.0	4.0	ns
t_{PZH} t_{PZL}	3-State output enable time nOE_{AB} to nBn	2, 4	1.0	2.7	5.7	ns
t_{PHZ} t_{PLZ}	3-State output disable time nOE_{AB} to nBn	2, 4	1.0	2.2	5.2	ns
t_{PZH} t_{PZL}	3-State output enable time $n\overline{OE}_{BA}$ to nAx	2, 4	1.0	2.7	5.7	ns
t_{PHZ} t_{PLZ}	3-State output disable time $n\overline{OE}_{BA}$ to nAx	3, 4	1.0	2.2	5.2	ns
t_W	pulse width HIGH or LOW	3, 4				ns
T_{SU}	Set up time	3, 4				ns
t_h	Hold time	3, 4				ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL} t_{PLH}	Propagation delay nAx to nBn; nBn to nAx	1,4	1.0	1.9	3.3				ns
t_{PZH} t_{PZL}	3-State output enable time nOE_{AB} to nBn	2, 4	1.0	2.3	4.5				ns
t_{PHZ} t_{PLZ}	3-State output disable time nOE_{AB} to nBn	2, 4	1.0	2.8	4.3				ns
t_{PZH} t_{PZL}	3-State output enable time $n\overline{OE}_{BA}$ to nAx	2, 4	1.0	2.3	4.5				ns
t_{PHZ} t_{PLZ}	3-State output disable time $n\overline{OE}_{BA}$ to nAx	3, 4	1.0	2.8	4.3				ns
t_W	pulse width HIGH or LOW	3, 4							ns
T_{SU}	Set up time	3, 4							ns
t_h	Hold time	3, 4							ns

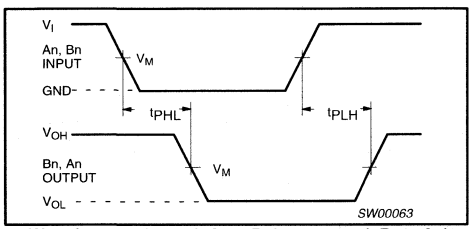
NOTES:
1. All typical values are at T_{amb} = 25°C.
2. All typical values are at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

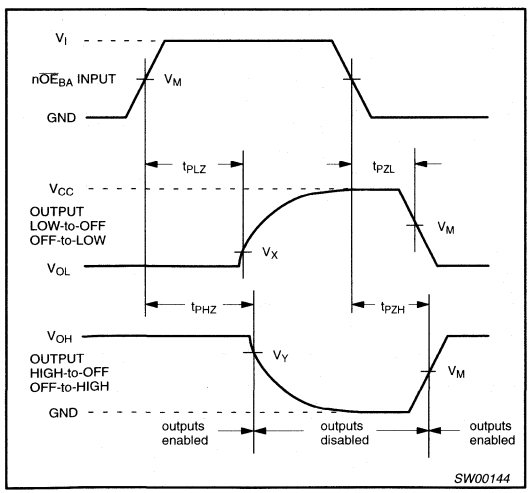
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

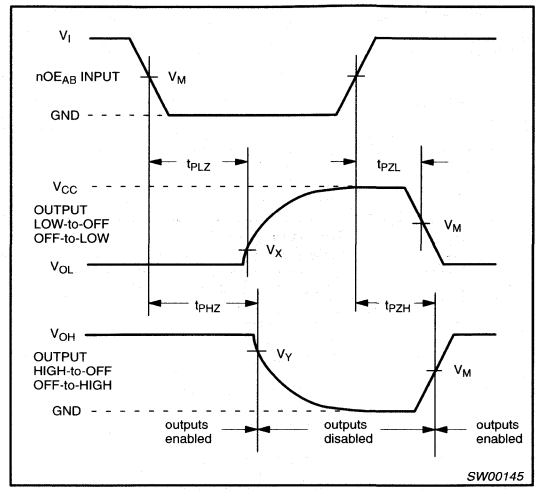
$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$



Waveform 1. Input (nAx, nBn) to output (nBn, nAx) propagation delay times

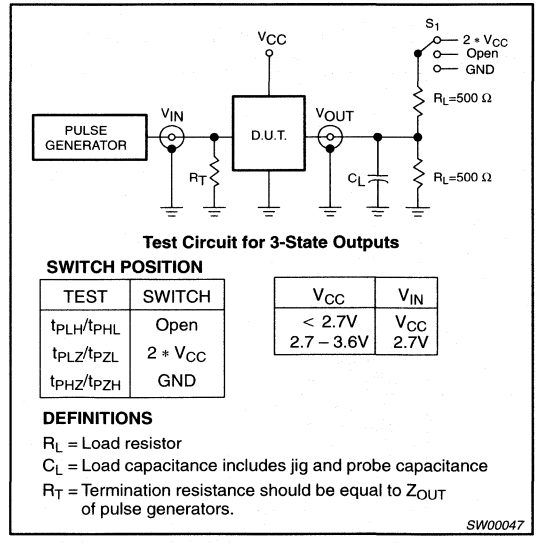


Waveform 2. 3-State enable and disable times for $n\overline{OE}_{BA}$ input



Waveform 3. 3-State enable and disable times for nOE_{AB} input

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Waveform 4. Load circuitry for switching times

16-bit bus transceiver/register (3-State) 74ALVCH16646

FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through pin-out architecture
- Low inductance, multiple V_{CC} and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- Output drive capability 50Ω transmission lines @ 85°C
- All inputs have bushold circuitry

DESCRIPTION

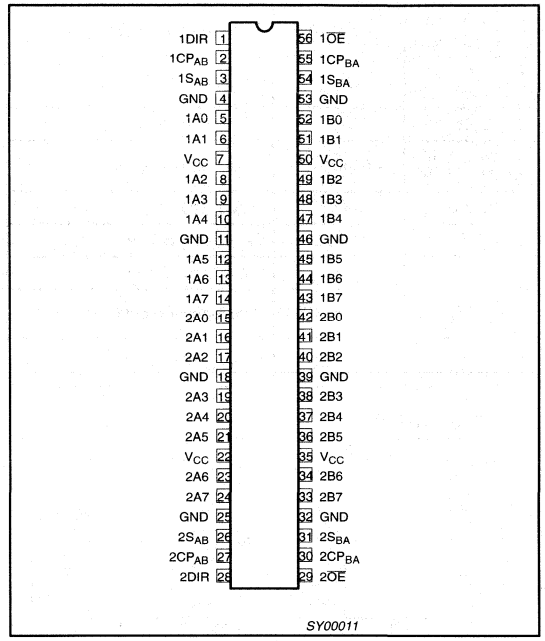
The 74ALVCH16646 consists of 16 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropriate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both. The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

To ensure the high impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nAx to nBx	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.6 2.7	ns
C_I	Input capacitance			3.0	pF
C_{PD}	Power dissipation capacitance per channel	V_I = GND to V_{CC}[1]	Outputs enabled	36	pF
			Outputs disabled	4	
F_{max}	Maximum clock frequency	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		300 320	MHz

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

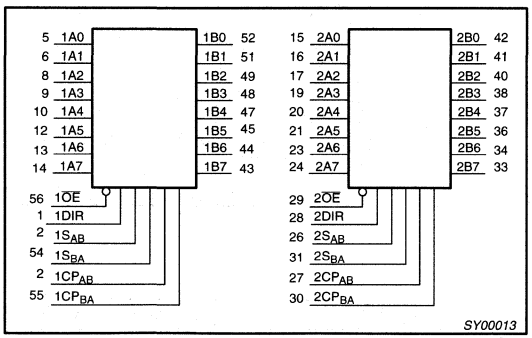
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16646 DGG	ACH16646 DGG	SOT364-1

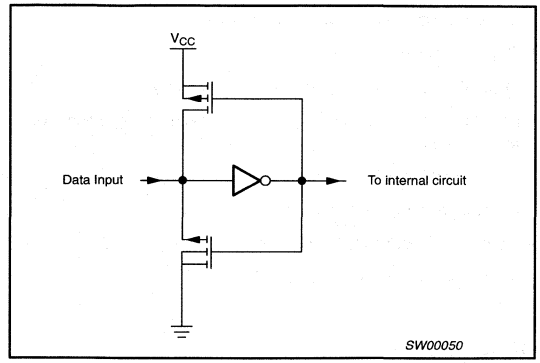
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	nDIR	Direction control input
2, 27	nCP_{AB}	Clock input A-to-B
3, 26	nS_{AB}	Select input A-to-B
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	Data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2A0 to 2A7	Data inputs/outputs
29, 56	$n\overline{OE}$	Output enable
30, 55	nCP_{BA}	Clock input B-to-A
31, 54	nS_{BA}	Select input B-to-A
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	Data inputs/outputs

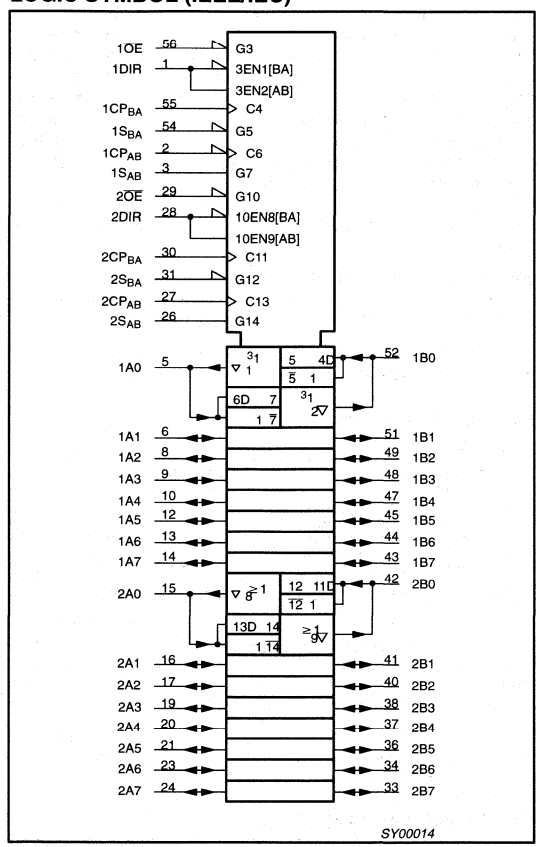
LOGIC SYMBOL



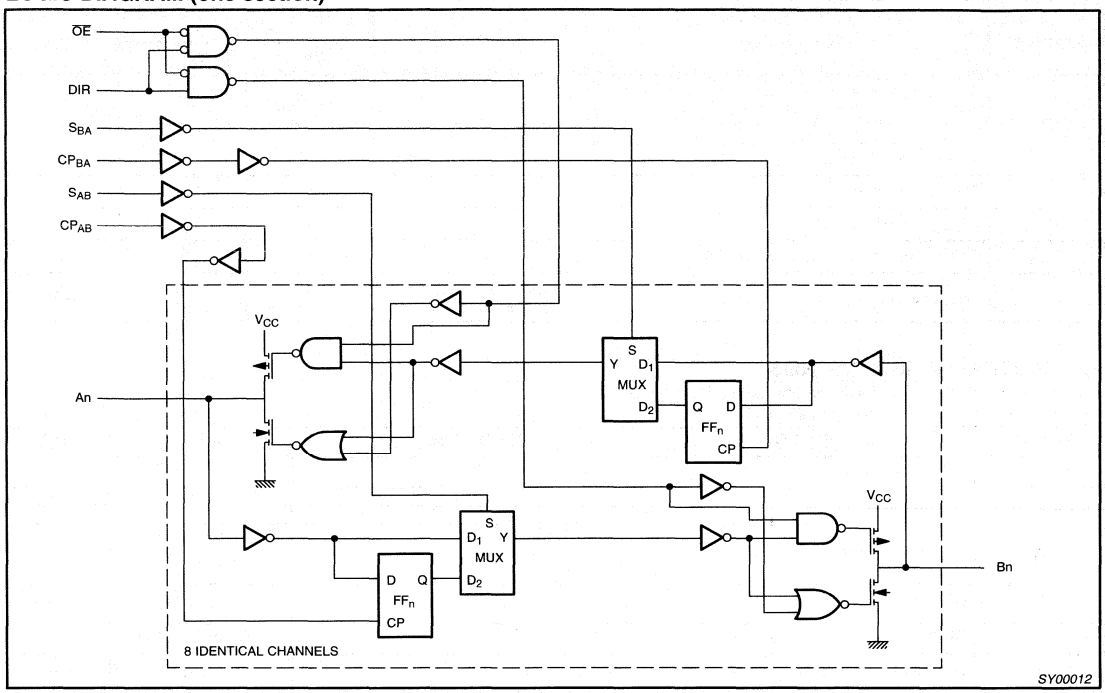
BUSHOLD CIRCUIT



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (one section)



FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$n\overline{OE}$	nDIR	nCP_{AB}	nCP_{BA}	nS_{AB}	nS_{BA}	nAx	nBx	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	store A, B unspecified* store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L X	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ± 0.2V			
			MIN	TYP	MAX	
t_{PLH}/t_{PHL}	Propagation delay nAx to nBx, nBx to nAx	1	1.0	2.7	4.8	ns
	Propagation delay nCP_{AB} to nBx, nCP_{BA} to nAx	3	1.0	3.4	5.6	
	Propagation delay nS_{AB} to nBx, nS_{BA} to nAx	2	1.0	3.4	6.8	
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nAx, nBx	4	1.0	3.3	6.5	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAx, nBx	4	1.6	2.8	5.7	ns
t_{PZH}/t_{PZL}	3-State output enable time nDIR to nAx, nBx	5	1.0	3.4	7.8	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nDIR to nAx, nBx	5	1.5	3.0	6.5	ns
t_W	Pulse width HIGH or LOW nCP_{AB}, nCP_{BA}	3	3.3	1.2		ns
t_{SU}	Set up time nAx to nCP_{AB}, nBx to nCP_{BA}	3	1.6	0.2		ns
t_h	Hold time nAx to nCP_{AB}, nBx to nCP_{BA}	3	0.6	0.1		ns
F_{max}	Maximum clock pulse frequency	3	150	300		MHz

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAx to nBx, nBx to nAx	1	1.0	2.6	3.9	1.0	2.8	4.5	ns
t_{PHL}/t_{PLH}	Propagation delay nCP_{AB} to nBx, nCP_{BA} to nAx	3	1.4	2.9	4.5	1.4	3.1	5.2	ns
t_{PHL}/t_{PLH}	Propagation delay nSAB to nBx, nSBA to nAx	2	1.3	3.1	5.3	1.3	3.5	6.4	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nAx, nBx	4	1.0	2.3	5.1	1.0	3.2	6.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAx, nBx	4	1.0	2.9	4.7	1.0	3.1	5.0	ns
t_{PZH}/t_{PZL}	3-State output enable time nDIR to nAx, nBx	5	1.4	3.0	5.1	1.4	3.4	6.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nDIR to nAx, nBx	5	1.4	2.5	5.3	1.4	3.3	6.0	ns
t_W	Pulse width HIGH or LOW nCP_{AB}, nCP_{BA}	3	3.3	0.7		3.3	1.0		ns
t_{SU}	Set up time nAx to nCP_{AB}, nBx to nCP_{BA}	3	1.4	0.3		1.7	0.2		ns
t_h	Hold time nAx to nCP_{AB}, nBx to nCP_{BA}	3	0.7	0.2		0.4	0.1		ns
F_{max}	Maximum clock pulse frequency	3	150	320		150	320		MHz

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. V_{CC} = 3.3V

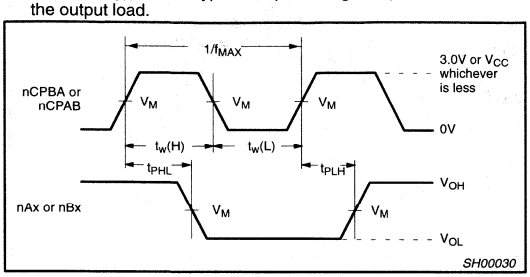
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

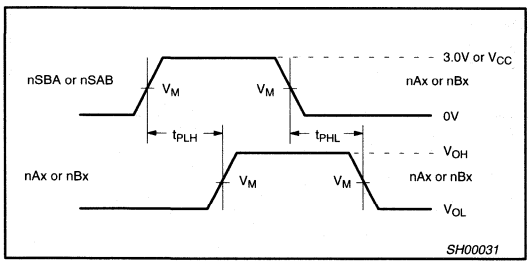
1. $V_M = 0.5$ V
2. $V_X = V_{OL} + 0.15$V
3. $V_Y = V_{OH} - 0.15$V
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

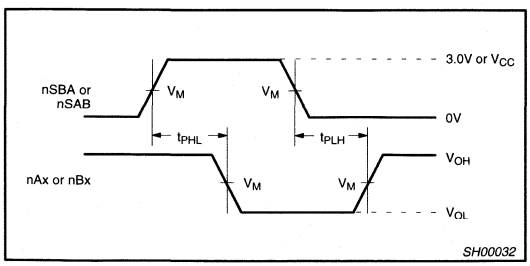
1. $V_M = 1.5$ V
2. $V_X = V_{OL} + 0.3$V
3. $V_Y = V_{OH} - 0.3$V
4. $V_I = 2.7$ V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



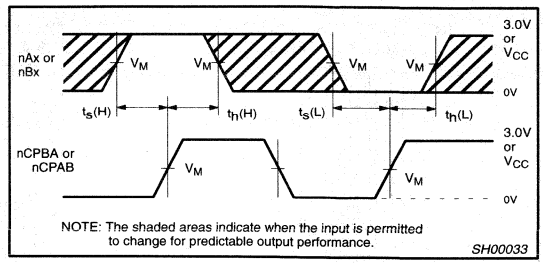
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



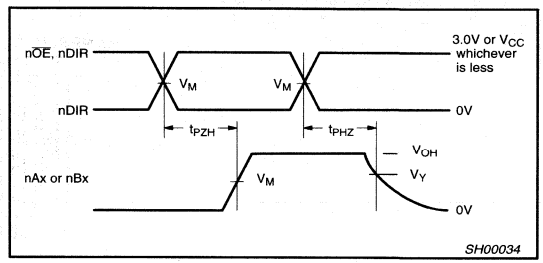
Waveform 2. Propagation Delay, nSAB to nBx or nSBA to nAx, nAx to nBx or nBx to nAx



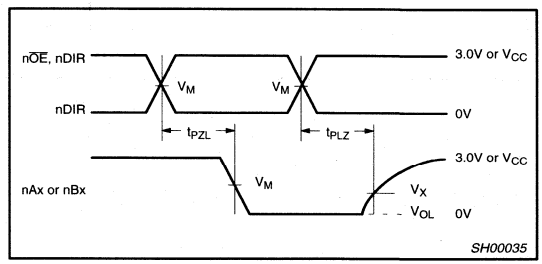
Waveform 3. Propagation Delay, nSBA to nAx or nSAB to nBx



Waveform 4. Data Setup and Hold Times

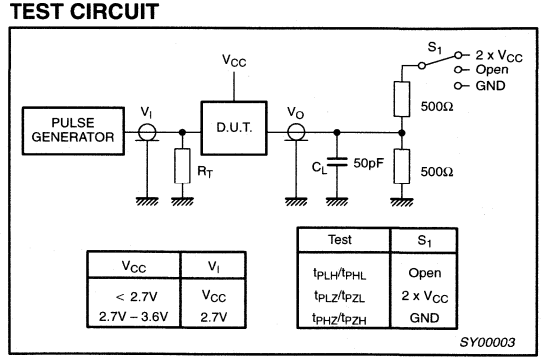


Waveform 5. 3–State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT



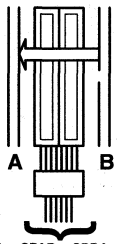
V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Load circuitry for switching times

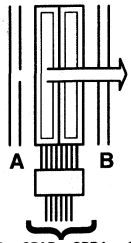
APPLICATION INFORMATION

REAL TIME BUS TRANSFER BUS B TO BUS A



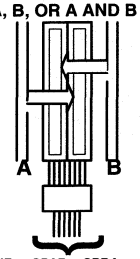
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



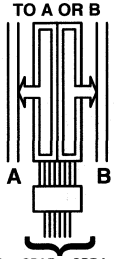
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	↑	X	X	X
L	L	X	↑	X	X
H	X	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

SH00028

16-bit transceiver/register with dual enable (3-State) 74ALVCH16652

FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through pin-out architecture
- Low inductance, multiple V_{CC} and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- Output drive capability 50Ω transmission lines @ 85°C
- All inputs have bushold circuitry

DESCRIPTION

The 74ALVCH16652 consists of 16 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the 'A' or 'B' or both buses, will be stored in the internal registers, at the appropriate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE inputs permit this operating mode. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from An to Bn is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from Bn to An possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input.

To ensure the high impedance state during power up or power down, $\overline{OE}_{BA}$ should be tied to V_{CC} through a pullup resistor and OE_{AB} should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ_n	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		3.2 3.2	ns
C_I	Input capacitance			3.0	pF
$C_{I/O}$	Input/Output capacitance				pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Outputs enabled	33	pF
			Outputs disabled	17	
F_{max}	Maximum clock frequency	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		250 350	MHz

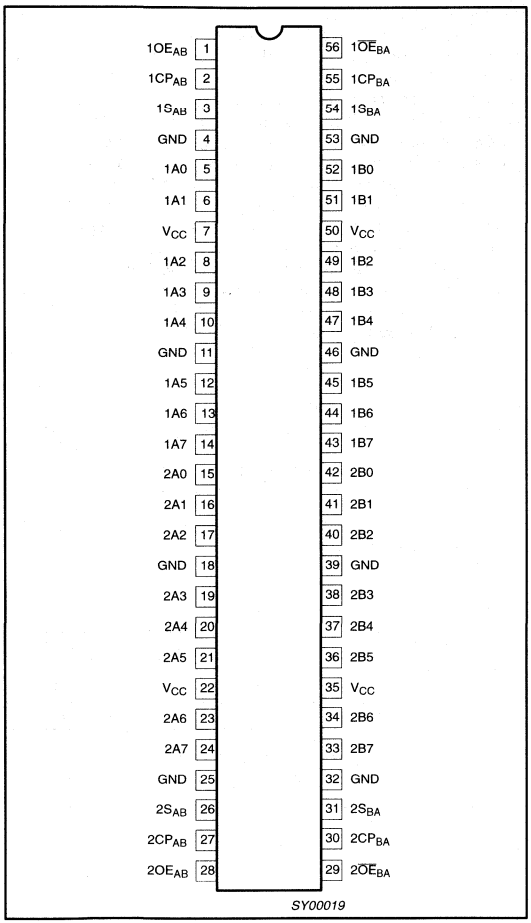
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16652 DGG	ACH16652 DGG	SOT364-1

PIN CONFIGURATION

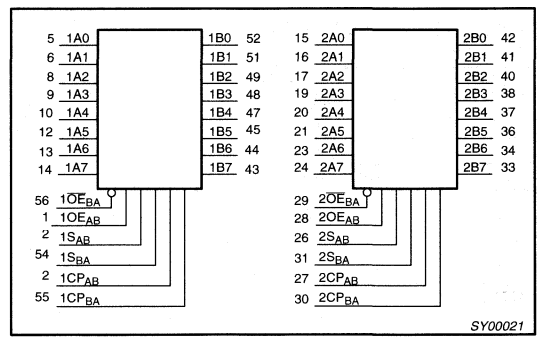


SY00019

PIN DESCRIPTION

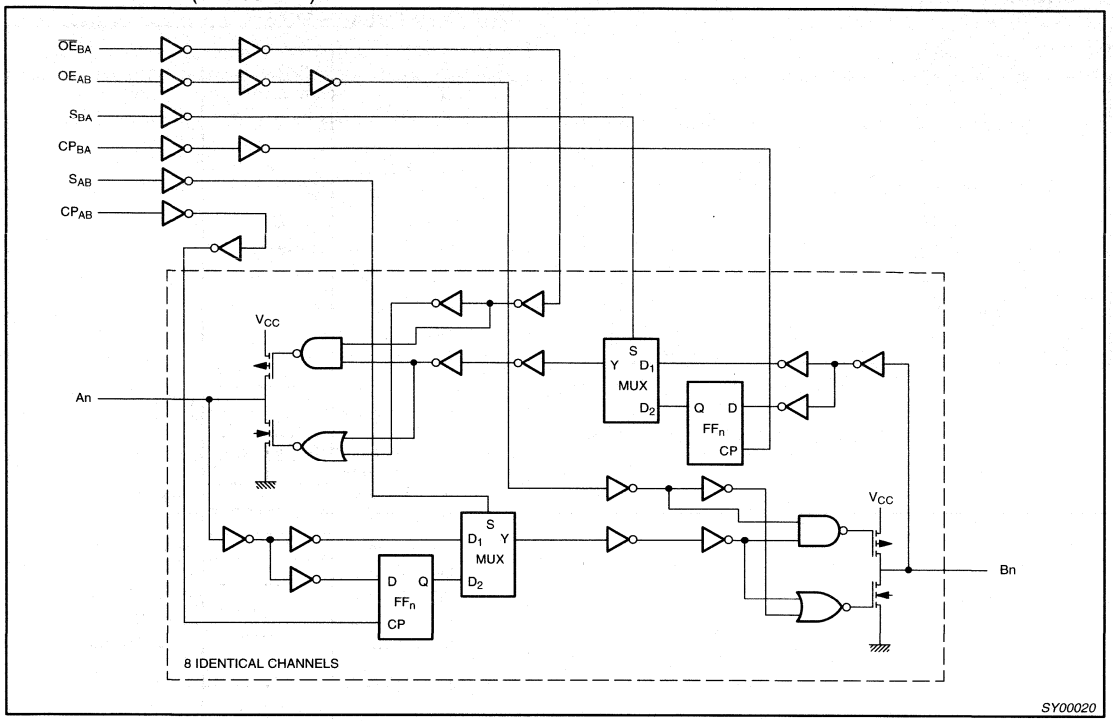
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	nOE$_{AB}$	Output enable A-to-B
2, 27	nCP$_{AB}$	Clock input A-to-B
3, 26	nS$_{AB}$	Select input A-to-B
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	Data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V$_{CC}$	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2B0 to 2B7	Data inputs/outputs
29, 56	n$\overline{OE}_{BA}$	Output enable B-to-A
30, 55	nCP$_{BA}$	Clock input B-to-A
31, 54	nS$_{BA}$	Select input B-to-A
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	Data inputs/outputs

LOGIC SYMBOL



SY00021

LOGIC DIAGRAM (one section)



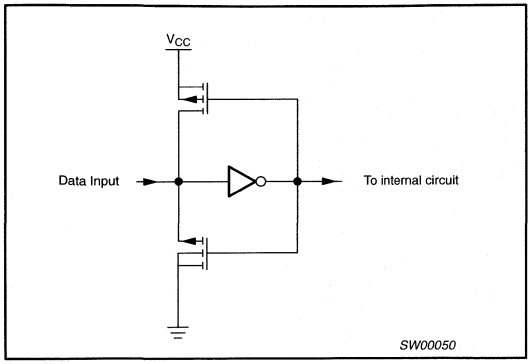
FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
nOEAB	$\overline{nOEBA}$	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un* output	store A, hold B store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un* output	input input	hold A, store B store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

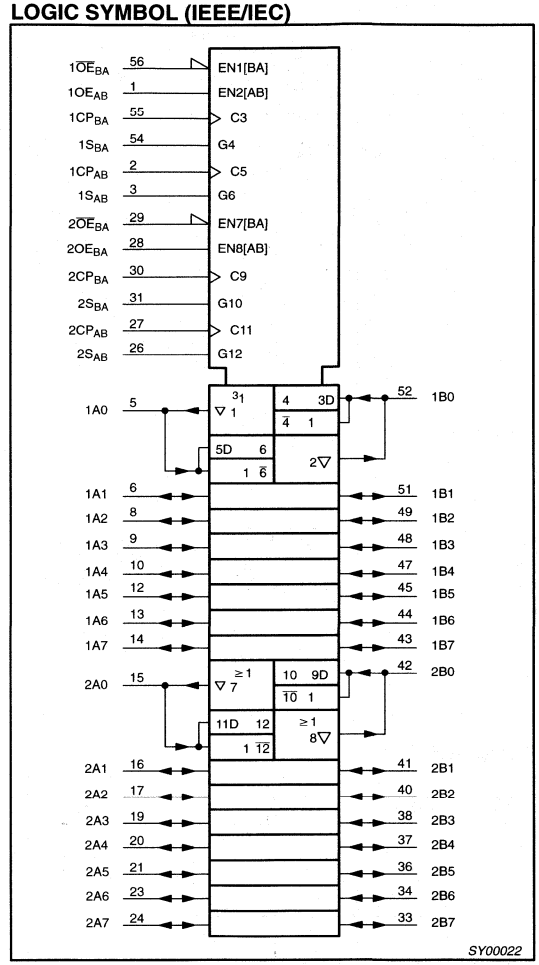
* The data output functions may be enabled or disabled by various signals at the OEAB and $\overline{OE}$BA inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

BUSHOLD CIRCUIT



LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	V_I < 0	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	V_O > V_{CC} or V_O < 0	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $I_O = -100\mu A$	$V_{CC}-0.2$	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = -6mA$	$V_{CC}-0.3$	$V_{CC}-0.08$		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = -12mA$	$V_{CC}-0.6$	$V_{CC}-0.26$		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $I_O = -12mA$	$V_{CC}-0.5$	$V_{CC}-0.14$		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $I_O = -12mA$	$V_{CC}-0.6$	$V_{CC}-0.09$		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $I_O = -24mA$	$V_{CC}-1.0$	$V_{CC}-0.28$		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = 6mA$		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = 12mA$		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $I_O = 12mA$		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $I_O = 24mA$		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; $I_O = 0$		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC} - 0.6V$; $I_O = 0$		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; $V_I = 0.7V$[2]	45	–		µA
		V_{CC} = 3.0V; $V_I = 0.8V$[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; $V_I = 1.7V$[2]	–45			µA
		V_{CC} = 3.0V; $V_I = 2.0V$[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	$V_{CC} = 3.6V$[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	$V_{CC} = 3.6V$[2]	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ±0.2V			
			MIN	TYP	MAX	
t_{PLH}/t_{PHL}	Propagation delay nAn to nBn, nBn to nAn	1, 5	1.0		4.8	ns
t_{PLH}/t_{PHL}	Propagation delay nCP_{AB} to nBn, nCP_{BA} to nAn	3, 5	1.0		5.6	ns
t_{PLH}/t_{PHL}	Propagation delay nS_{AB} to nBn, nS_{BA} to nAn	2, 5	1.0		6.8	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nAn, nBn	4, 5	1.0		6.5	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAn, nBn	4, 5	1.6		5.7	ns
t_{PZH}/t_{PZL}	3-State output enable time OEAB to nBn	3, 5	1.0		7.8	ns
t_{PHZ}/t_{PLZ}	3-State output disable time OEAB to nBn	3, 5	1.5		6.5	ns
t_W	Pulse width HIGH or LOW nCP_{AB}, nCP_{BA}	3, 5	3.3			ns
t_{SU}	Set up time nAn to nCP_{AB}, nBn to nCP_{BA}	3, 5	1.6			ns
t_h	Hold time nAn to nCP_{AB}, nBn to nCP_{BA}		0.6			ns
F_{max}	Maximum clock pulse frequency		150			MHz

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nBn, nBn to nAn	1, 5	1.0	3.9	3.9		4.5	4.5	ns
t_{PHL}/t_{PLH}	Propagation delay nCP_{AB} to nBn, nCP_{BA} to nAn	3, 5	1.0	4.5	4.5		5.2	5.2	ns
t_{PHL}/t_{PLH}	Propagation delay nS_{AB} to nBn, nS_{BA} to nAn	2, 5	1.0	5.3	5.3		6.4	6.4	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nAn, nBn	4, 5	1.0	5.1	5.1		6.2	6.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAn, nBn	4, 5	1.4	4.7	4.7		5	5	ns
t_{PZH}/t_{PZL}	3-State output enable time OE_{AB} to nBn	3, 5	1.0	5.1	5.1		6.2	6.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time OE_{AB} to nBn	3, 5	1.1	5.3	5.3		6.0	6.0	ns
t_W	Pulse width HIGH or LOW nCP_{AB}, nCP_{BA}	3, 5	3.3			3.3			ns
t_{SU}	Set up time nAn to nCP_{AB}, nBn to nCP_{BA}	3, 5	1.4			1.7			ns
t_h	Hold time nAn to nCP_{AB}, nBn to nCP_{BA}		0.7			0.4			ns
F_{max}	Maximum clock pulse frequency		150			150			MHz

NOTES:

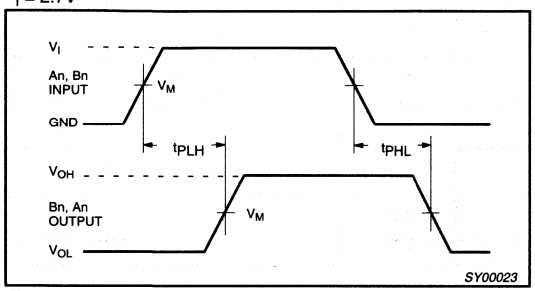
1. All typical values are at T_{amb} = 25°C.
2. Typical values are at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

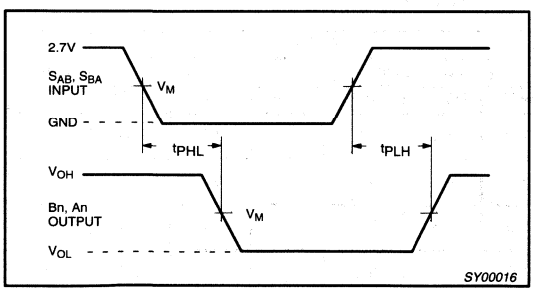
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

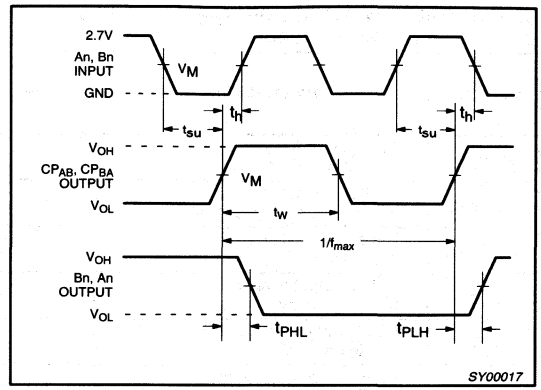
$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$



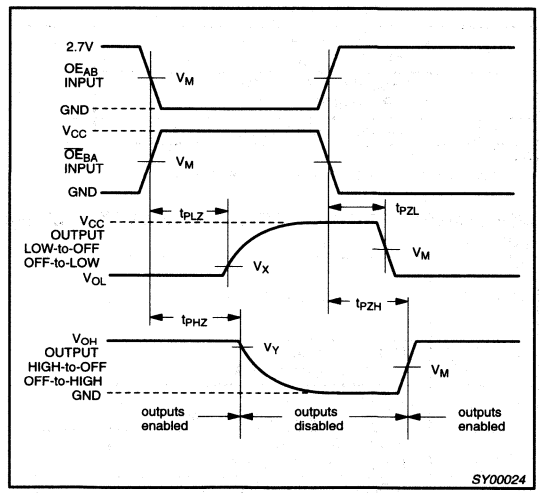
Waveform 1. Input An, Bn to output Bn, An propagation delay times



Waveform 2. Input S_{AB}, S_{BA} to output Bn, An propagation delay times

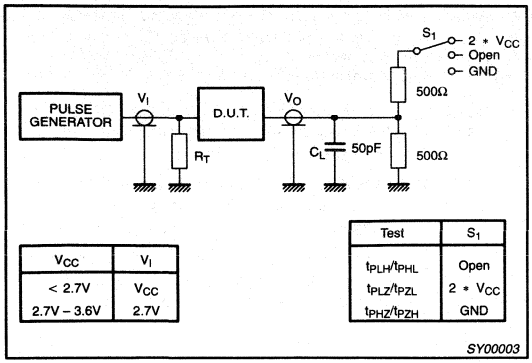


Waveform 3. An, Bn to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock frequency and the CP_{AB}, CP_{BA} to output Bn, An propagation delays



Waveform 4. OE inputs (OE_{AB}, OE_{BA}) to outputs An, Bn enable and disable times and the input rise and fall times

TEST CIRCUIT

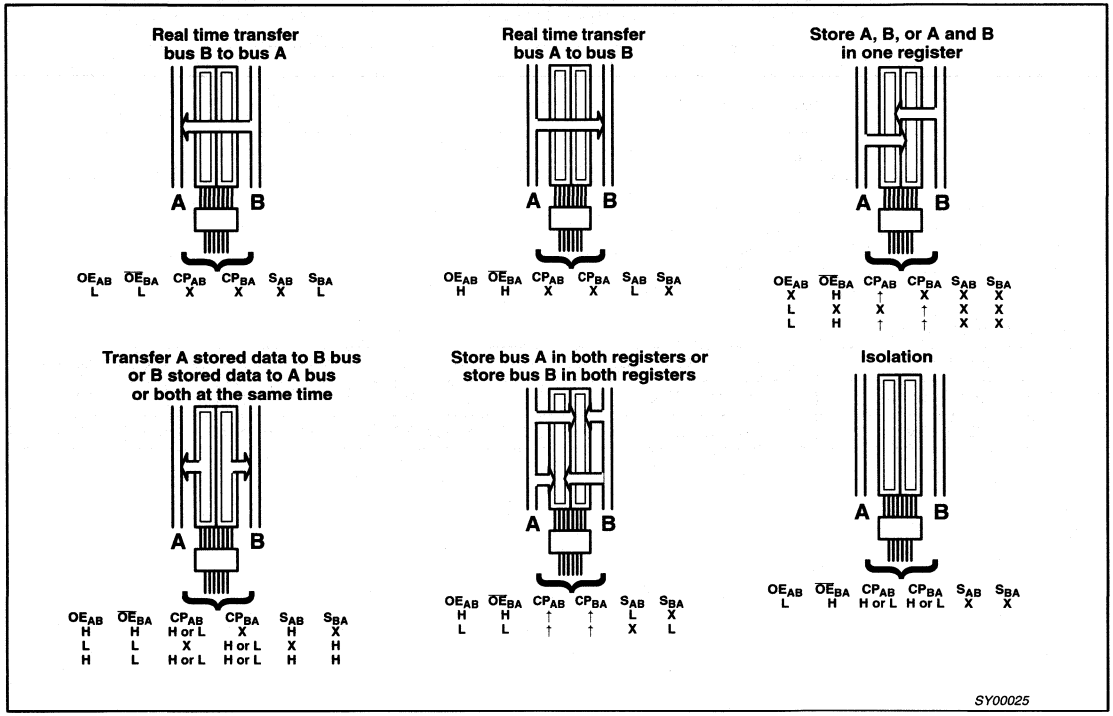


V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

Waveform 5. Load circuitry for switching times

APPLICATION INFORMATION



20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Current drive ± 24 mA at 3.0 V
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16821 has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable ($n\overline{OE}$) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

When $n\overline{OE}$ is LOW, the data in the register appears at the outputs. When $n\overline{OE}$ is HIGH, the outputs are in high impedance OFF state. Operation of the $n\overline{OE}$ input does not affect the state of the flip-flops.

The 74ALVCH16821 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ_n	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.6 2.5	ns
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	Outputs enabled	33	pF
			Outputs disabled	17	
F_{max}	Maximum clock frequency	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		250 350	MHz

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVCH16821 DL	ACH16821 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16821 DGG	ACH16821 DGG	SOT364-1

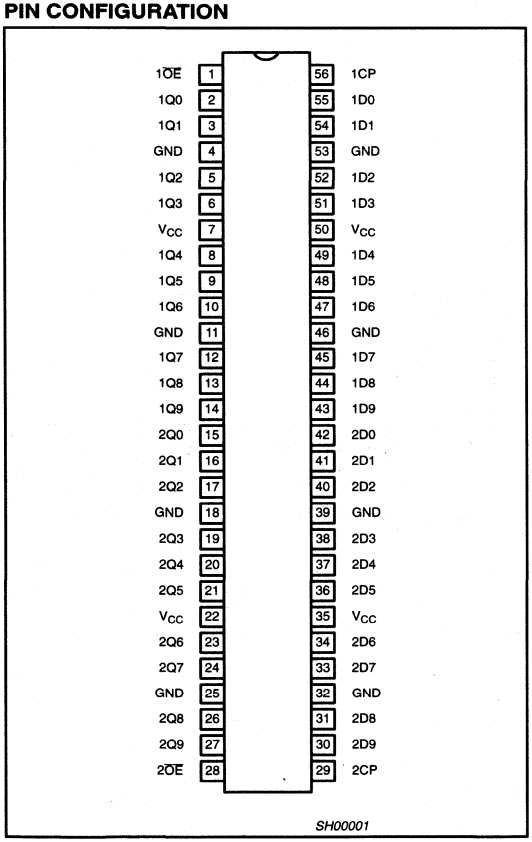
20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43	1D0 - 1D9	Data inputs
42, 41, 40, 38, 37, 36, 34, 33, 31, 30	2D0 - 2D9	
2, 3, 5, 6, 8, 9, 10, 12, 13, 14	1Q0 - 1Q9	Data outputs
15, 16, 17, 19, 20, 21, 23, 24, 26, 27	2Q0 - 2Q9	
1, 28	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION



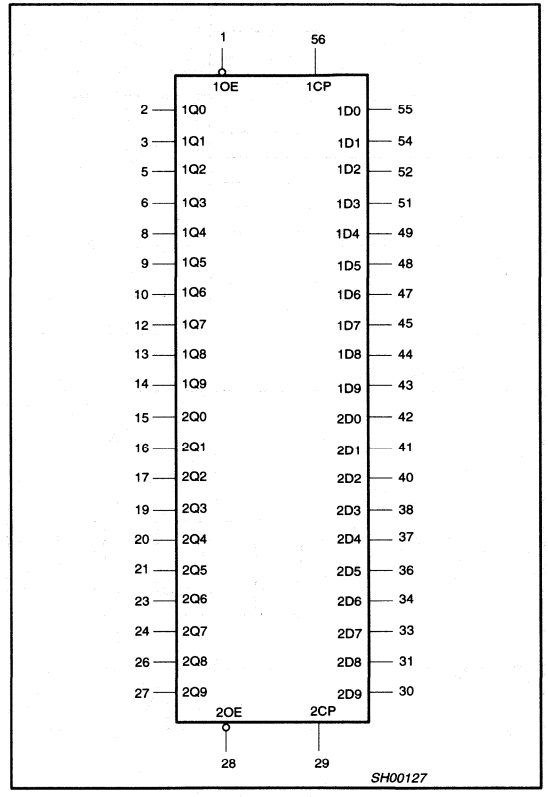
SH00001

FUNCTION TABLE

INPUTS			OUTPUT
$n\overline{OE}$	CP	Dx	Q
L	↑	L	L
L	↑	H	H
L	‡	X	Q0
H	X	X	Z

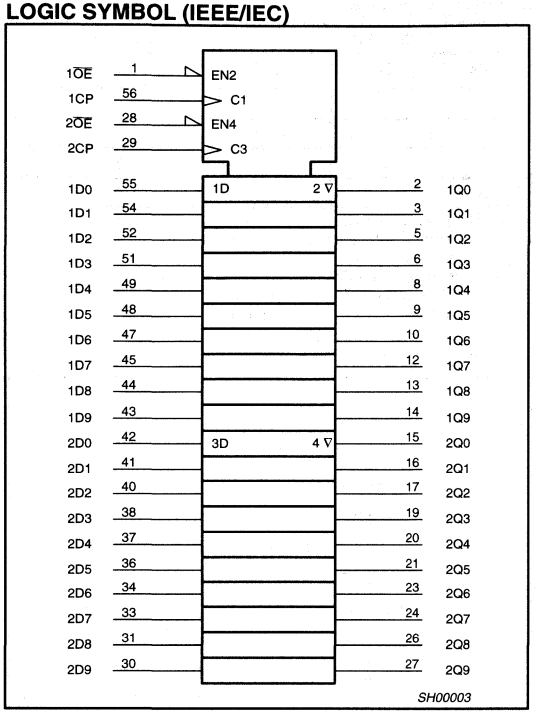
H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance OFF state
↑ = LOW to HIGH clock transition
‡ = Not a LOW-to-HIGH clock transition

LOGIC SYMBOL

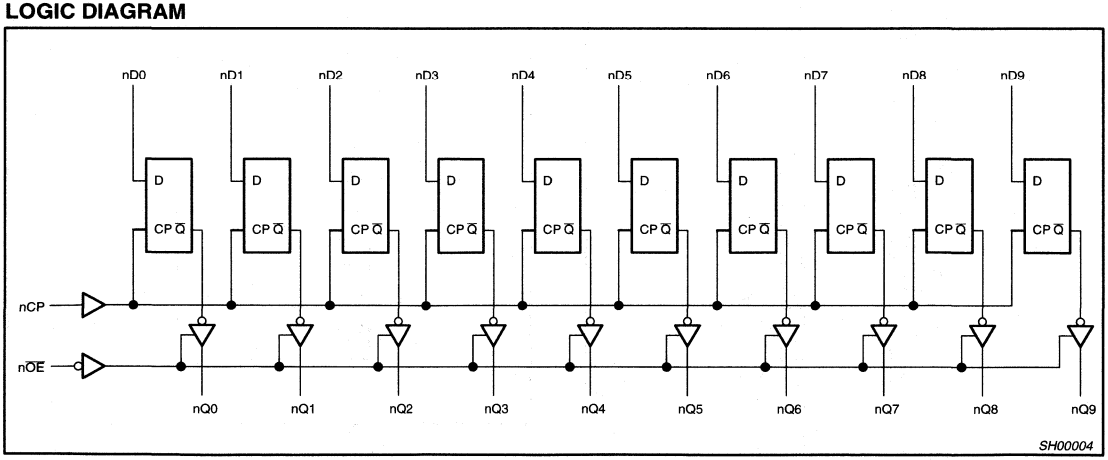


SH00127

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	V_I < 0	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	V_O > V_{CC} or V_O < 0	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $I_O = -100\mu A$	$V_{CC} - 0.2$	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = -6mA$	$V_{CC} - 0.3$	$V_{CC} - 0.08$		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = -12mA$	$V_{CC} - 0.6$	$V_{CC} - 0.26$		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $I_O = -12mA$	$V_{CC} - 0.5$	$V_{CC} - 0.14$		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $I_O = -12mA$	$V_{CC} - 0.6$	$V_{CC} - 0.09$		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $I_O = -24mA$	$V_{CC} - 1.0$	$V_{CC} - 0.28$		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = 6mA$		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = 12mA$		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $I_O = 12mA$		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $I_O = 24mA$		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; $I_O = 0$		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC} - 0.6V$; $I_O = 0$		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; $V_I = 0.7V$[2]	45	–		µA
		V_{CC} = 3.0V; $V_I = 0.8V$[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; $V_I = 1.7V$[2]	–45			µA
		V_{CC} = 3.0V; $V_I = 2.0V$[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ± 0.2V			
			MIN	TYP[1]	MAX	
t_{PLH}/t_{PHL}	Propagation delay nCP to nQ_n	1, 4	1.0	2.6	5.8	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nQ_n	2, 4	1.0	2.8	6.6	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nQ_n	2, 4	1.0	2.2	5.7	ns
t_W	nCP pulse width HIGH or LOW	3, 4	3.0	1.8		ns
t_{SU}	Set up time nD_n to nCP	3, 4	1.4	0.3		ns
t_h	Hold time nD_n to nCP	3, 4	0.4	0.0		ns
F_{max}	Maximum clock pulse frequency	1, 4	150	250		MHz

NOTE:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ_n	1, 4	1.0	2.5	4.5	1.0	2.8	5.3	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nQ_n	2, 4	1.0	2.3	5.1	1.0	3.2	6.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nQ_n	2, 4	1.0	2.8	4.6	1.0	3.1	5.0	ns
t_W	nCP pulse width HIGH or LOW	3, 4	3.3	0.2		3.3	1.7		ns
t_{SU}	Set up time nD_n to nCP	3, 4	1.0	0.2		1.2	0.3		ns
t_h	Hold time nD_n to nCP	3, 4	0.8	0.4		0.6	–0.3		ns
F_{max}	Maximum clock pulse frequency	1, 4	150	350		150	300		MHz

NOTES:

1. All typical values are at T_{amb} = 25°C.

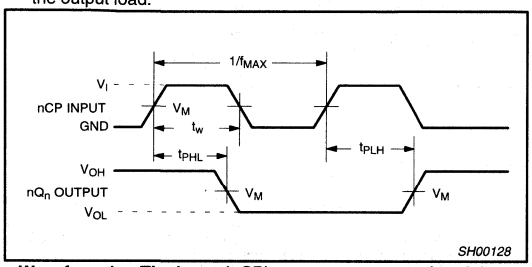
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

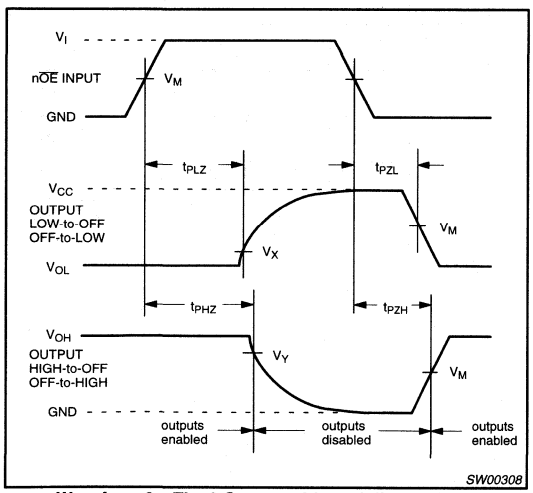
1. V_M = 0.5 V
2. $V_X = V_{OL} + 0.15V$
3. $V_Y = V_{OH} - 0.15V$
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

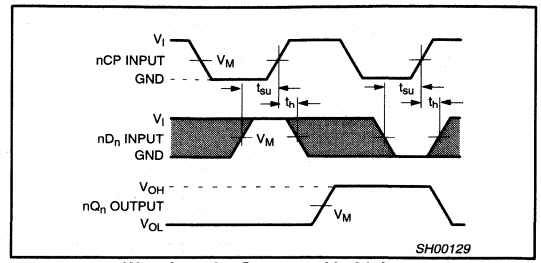
1. V_M = 1.5 V
2. $V_X = V_{OL} + 0.3V$
3. $V_Y = V_{OH} - 0.3V$
4. V_I = 2.7 V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. The input (nCP) to output propagation delays.

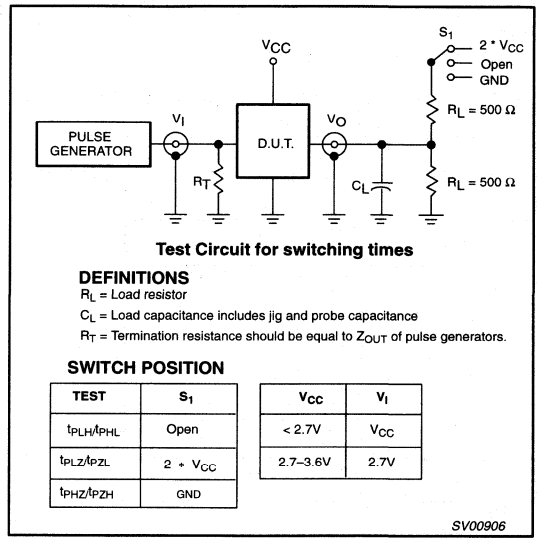


Waveform 2. The 3-State enable and disable times.



Waveform 3. Set up and hold times.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Waveform 4. Load circuitry for switching times

18-bit D-type flip-flop (3-State) 74ALVCH16823

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- Multibyte™flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins to minimize noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16823 is a 18-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. Incorporates bushold data inputs which eliminate the need for external pull-up resistors to hold unused inputs. The74ALVCH16823 consists of two sections of nine edge-triggered flip-flops. A clock (CP) input, an output-enable ($\overline{OE}$) input, a Master reset ($\overline{MR}$) input and a clock-enable($\overline{CE}$) input are provided for each total 9-bit section.

With the clock-enable ($\overline{CE}$) input LOW, the D-type flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition. Taking $\overline{CE}$ HIGH disables the clock buffer, thus latching the outputs. Taking the Master reset ($\overline{MR}$) input LOW causes all the Q outputs to go LOW independently of the clock.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of flip-flops.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	V_{CC} = 2.5V, CL = 30pF V_{CC} = 3.3V, CL = 50pF		2.1 2.1	ns
F_{max}	Maximum clock frequency	V_{CC} = 2.5V, CL = 30pF V_{CC} = 3.3V, CL = 50pF		300 350	MHz
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Outputs enabled	16	pF
			Outputs disabled	10	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

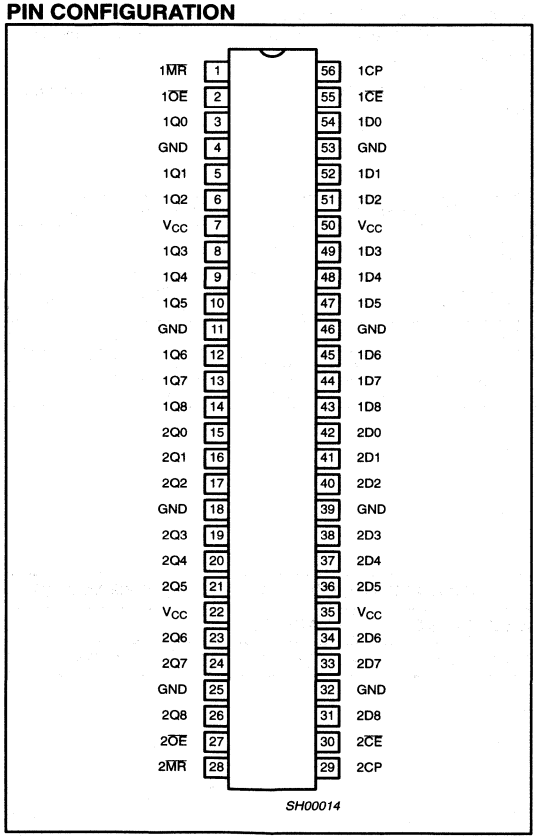
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type II	-40°C to +85°C	74ALVCH16823 DL	ACH16823 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVCH16823 DGG	ACH16823 DGG	SOT364-1

18-bit D-type flip-flop (3-State) 74ALVCH16823

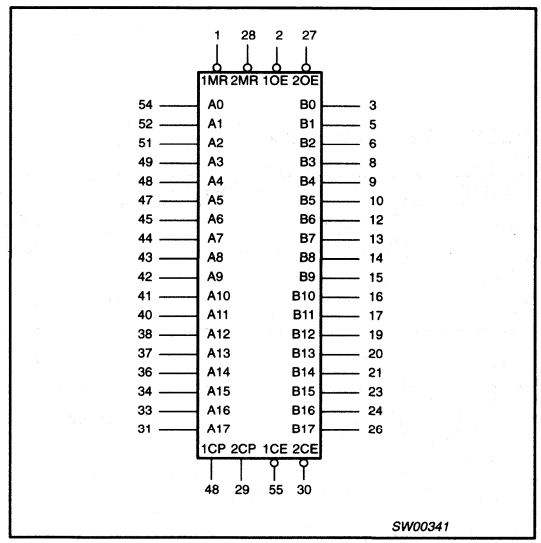
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 27	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active-Low)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	1D0-1D8 2D0-2D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	1Q0-1Q8 2Q0-2Q8	Data outputs
56, 29	1CP, 2CP	Clock pulse input (active rising edge)
55, 30	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active-Low)
1, 28	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION

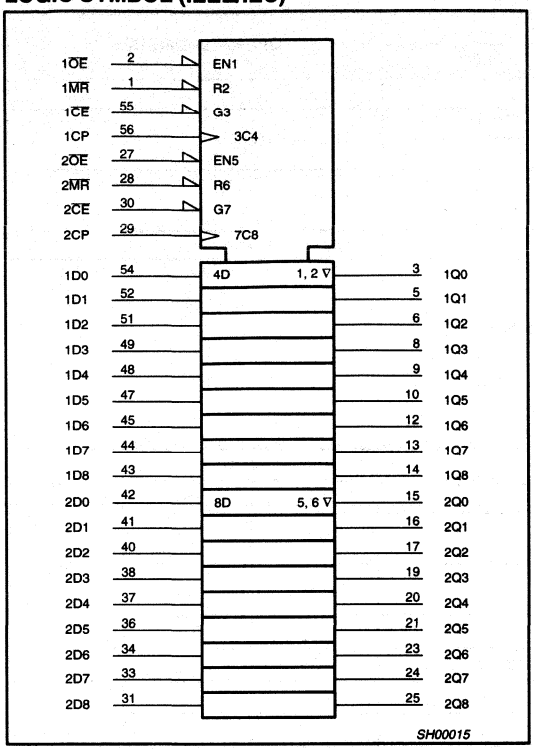


LOGIC SYMBOL

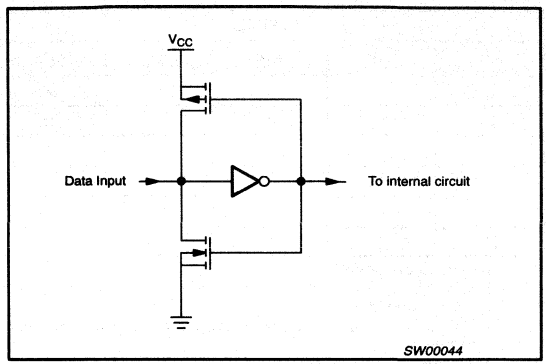


18-bit D-type flip-flop (3-State) 74ALVCH16823

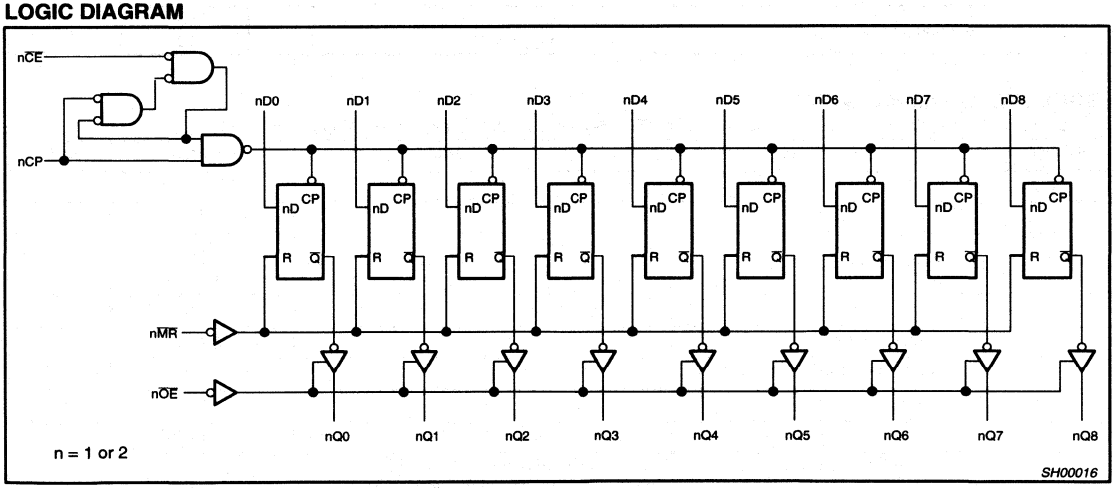
LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUT	OPERATING MODES
$n\overline{OE}$	$n\overline{MR}$	$n\overline{CE}$	nCP	nDx	nQx	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	L	L	X	Q_0	Hold
L	H	H	X	X	Q_0	
H	X	X	X	X	Z	Disable outputs

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the Low-to-High clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
Z = HIGH impedance "off" state
↑ = LOW to High clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range	for data input pins	0	V_{CC}	V
		for control pins	0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +5.5	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 1.8V	0.7*V_{CC}	0.9		
		V_{CC} = 2.3 to 2.7V	1.7	1.2		
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V		–	GND	V
		V_{CC} = 1.8V		0.9	0.2*V_{CC}	
		V_{CC} = 2.3 to 2.7V		1.2	0.7	
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 1.8 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}	–	V
		V_{CC} = 1.8V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC} – 0.4	V_{CC} – 0.10	–	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08	–	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.17	–	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6	V_{CC} – 0.26	–	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14	–	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28	–	
V_{OL}	LOW level output voltage	V_{CC} = 1.8 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 1.8V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.09	0.30	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.07	0.20	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.15	0.40	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 18mA		0.23	0.60	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current per control pin	V_{CC} = 1.8 to 3.6V; V_I = 5.5V or GND		0.1	5	µA
	Input leakage current per data pin	V_{CC} = 1.8 to 3.6V; V_I = V_{CC} or GND		0.1	5	
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 1.8 to 2.7V; V_I = V_{CC} or GND		0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND		0.1	15	
I_{OZ}	3-State output OFF-state current	V_{CC} = 1.8 to 2.7V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	5	µA
		V_{CC} = 2.7 to 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	10	
ΔI_{CC}	Additional quiescent supply current given per data I/O pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 2.7V[2]	300			µA
		V_{CC} = 3.6V[2]	450			
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 2.7V[2]	–300			µA
		V_{CC} = 3.6V[2]	–450			

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE AND V_{CC} < 2.3V

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 2.3 to 2.7V			V_{CC} = 1.8V			V_{CC} = 1.2V	
			MIN	TYP[1, 2]	MAX	MIN	TYP1	MAX	TYP[1]	
t_{PLH}/t_{PHL}	Propagation delay nCP to nQ_n	1, 5	1.0	2.8	4.9	1.5	4.5	7.5	10.6	ns
t_{PLH}/t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n	2, 5	1.0	2.9	5.0	1.5	4.6	7.4	9.9	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nQ_n	4, 5	1.0	2.8	5.3	1.5	4.4	7.7	10.4	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nQ_n	4, 5	1.0	2.2	4.1	1.5	3.3	5.5	6.7	ns
t_W	nCP pulse width	1, 5	3.0	1.6		4.0	2.0			ns
	$n\overline{MR}$ pulse width, LOW	3, 5	3.0	0.4		4.0	0.8			
t_{SU}	Set up time nD_n to nCP	3, 5	1.2	0.2		1.5	0.2			ns
	Set up time $n\overline{CE}$ to nCP		1.8	–0.2		2.0	–0.2			
t_h	Hold time nD_n to nCP	3, 5	0.8	–0.1		0.6	–0.2			ns
	Hold time $n\overline{CE}$ to nCP		0.3	0.2		0.3	0.2			
t_{rec}	Recovery time $n\overline{MR}$ to nCP	2, 5	1.0	0.3		0.8	0.2			ns
F_{max}	Maximum clock pulse frequency	1, 5	150	300		125	250			MHz

NOTE:
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 2.5V.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.0 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PLH}/t_{PHL}	Propagation delay nCP to nQ_n	1, 5	1.0	2.5	3.7	1.0	2.7	4.3	ns
t_{PLH}/t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n	2, 5	1.0	2.6	4.0	1.0	3.1	4.6	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nQ_n	4, 5	1.0	2.5	4.3	1.0	3.1	5.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nQ_n	4, 5	1.0	2.8	3.9	1.0	3.1	4.3	ns
t_W	nCP pulse width HIGH or LOW	1, 5	2.5	1.4		3.0	1.6		ns
	$n\overline{MR}$ pulse width HIGH or LOW	3, 5	2.5	0.3		3.0	0.6		
t_{SU}	Set up time nD_n to nCP	3, 5	1.2	0.2		1.5	0.4		ns
	Set up time $n\overline{CE}$ to nCP		1.5	–0.1		1.9	–0.1		
t_h	Hold time nD_n to nCP	3, 5	0.8	0.0		0.6	–0.2		ns
	Hold time $n\overline{CE}$ to nCP		0.5	0.1		0.4	0.1		
t_{rec}	Recovery time $n\overline{MR}$ to nCP	2, 5	1.0	0.2		0.8	0.1		ns
F_{max}	Maximum clock pulse frequency	1, 5	200	350		150	300		MHz

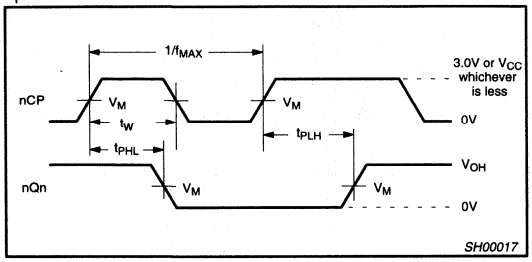
NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V.

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

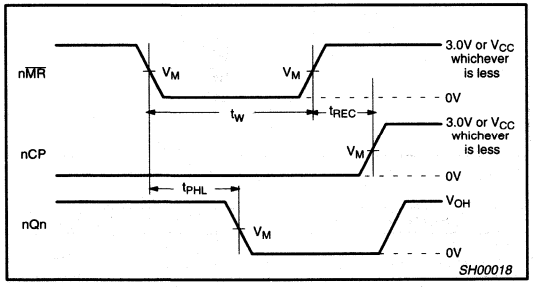
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

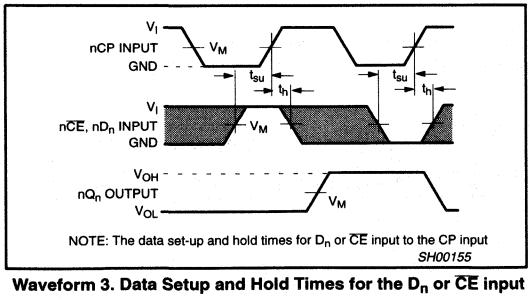
$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$



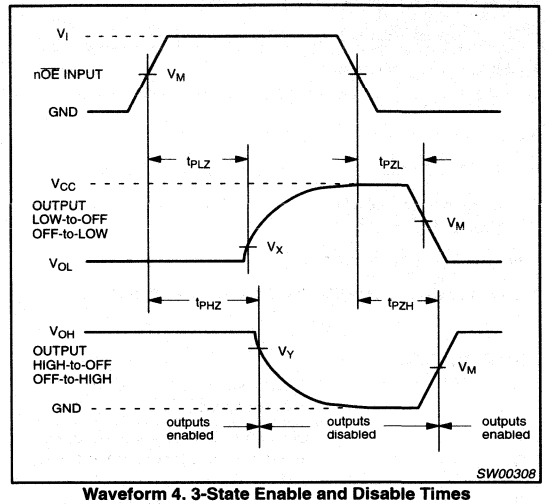
Waveform 1. Clock (nCP) to Output (nQn) Propagation Delays, Clock Pulse Width, and Maximum Clock Pulse Frequency



Waveform 2. Master Reset ($\overline{MR}$) Pulse Width, $\overline{MR}$ to Output propagation Delay and $\overline{MR}$ to Clock Recovery Time

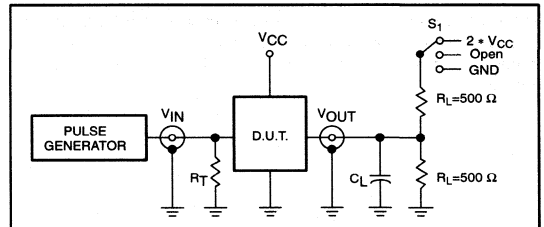


Waveform 3. Data Setup and Hold Times for the D_n or $\overline{CE}$ input to the CP input



Waveform 4. 3-State Enable and Disable Times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

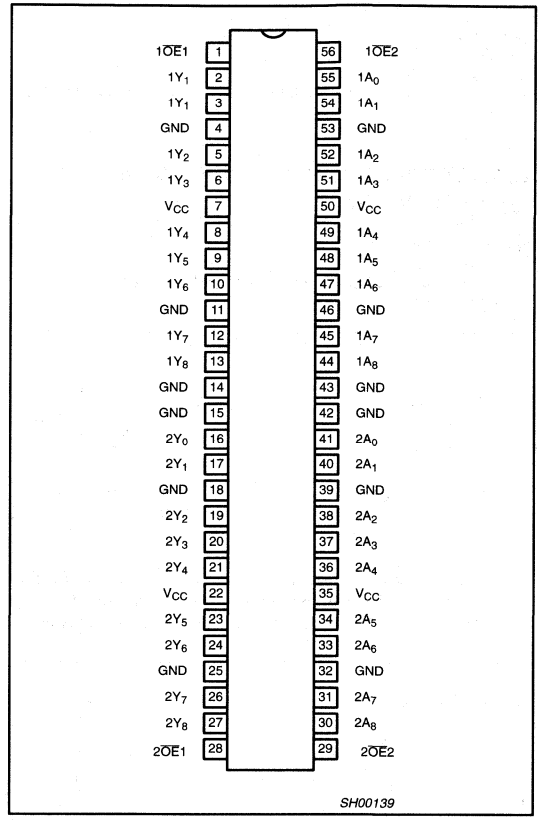
Waveform 5. Load circuitry for switching times

18-bit buffer/driver (3-State) 74ALVCH16825

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C

PIN CONFIGURATION



DESCRIPTION

The 74ALVCH16825 is an 18–bit non-inverting buffer/driver with 3-State outputs for bus-oriented applications.

The 74ALVCH16825 consists of two 9-bit sections with separate output enable signals. For either 9-bit buffer section, the two output enable ($1\overline{OE}1$ and $1\overline{OE}2$ or $2\overline{OE}1$ and $2\overline{OE}2$) inputs must both be LOW for corresponding D outputs to be active. If either output enable input is HIGH, the outputs of that 9-buffer section are in the high impedance state.

The 74ALVCH16825 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.0 2.0	ns
C_I	Input capacitance			4.0	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Output enabled	19	pF
			Output disabled	3	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

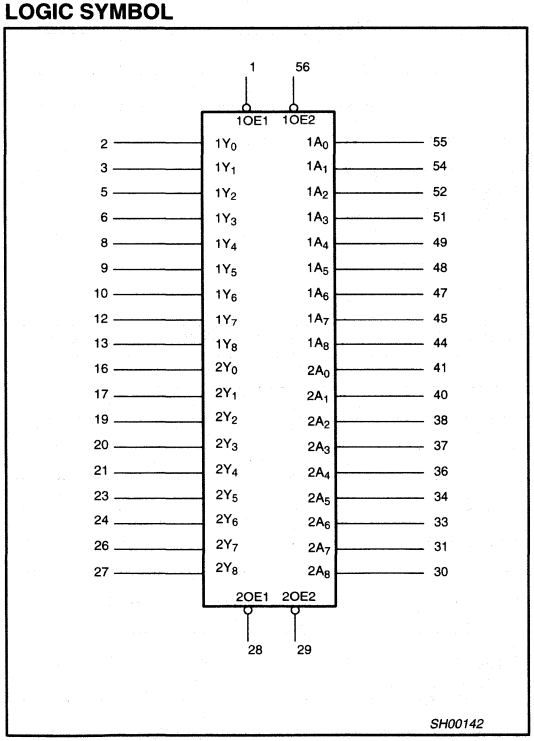
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74ALVCH16825 DGG	ACH16825 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}1$	Output enable input (active LOW)
56	$1\overline{OE}2$	
55, 54, 52, 51, 49, 48, 47, 45, 44	1A0 to 1A8	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13	1Y0 to 1Y8	Data outputs
4, 11, 14, 15, 18, 25, 32, 39, 42, 43, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
28	$2\overline{OE}1$	Output enable input (active LOW)
29	$2\overline{OE}2$	
43, 42, 41, 40, 38, 37, 36, 34, 33, 31	2A0 to 2A8	Data inputs
16, 17, 19, 20, 21, 23, 24, 26, 27	2Y0 to 2Y8	Data outputs

LOGIC SYMBOL

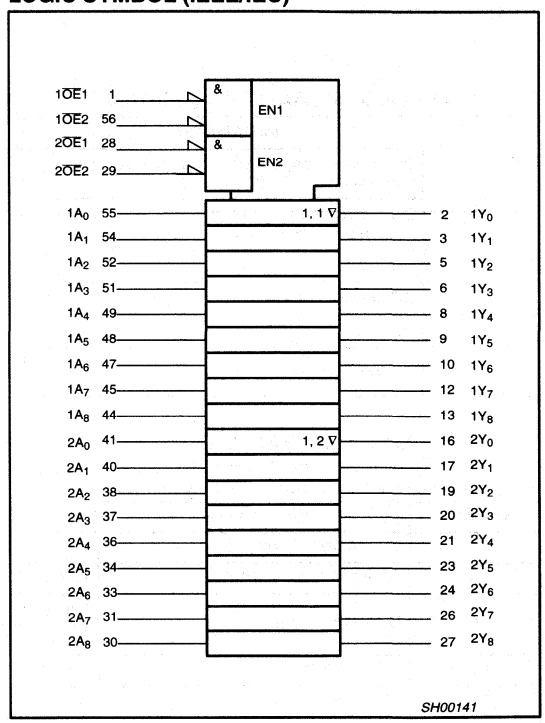


FUNCTION TABLE

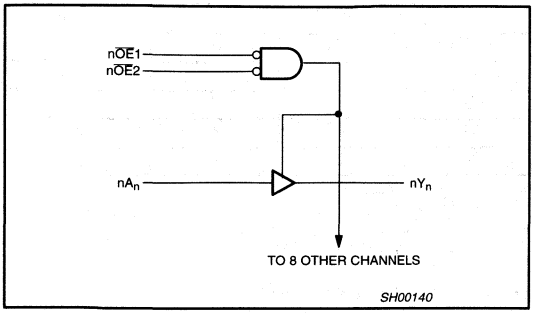
INPUTS			OUTPUT
$n\overline{OE}1$	$n\overline{OE}2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state

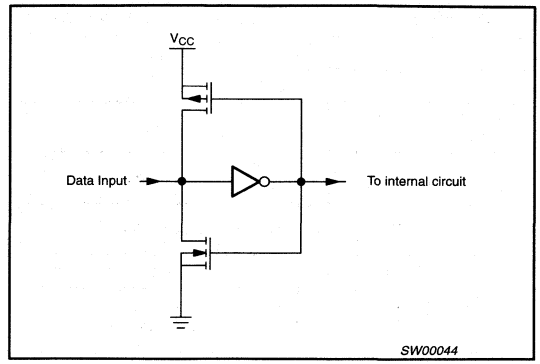
LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[2]	–0.5 to +4.6	V
		For data inputs[2]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; V_I = V_{CC} – 0.6V; I_O = 0		150	750	µA
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 3.6V	500			µA
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 3.6V	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7V			
			MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	2.0	4.1	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$n to nYn	2, 3	1.0	2.9	6.0	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$n to nYn	2,3	1.2	2.2	5.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	2.0	3.4	1.0	2.1	3.9	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$n to nYn	2, 3	1.0	2.8	4.7	1.0	2.9	5.7	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$n to nYn	2, 3	1.3	2.9	4.5	1.3	3.0	4.9	ns

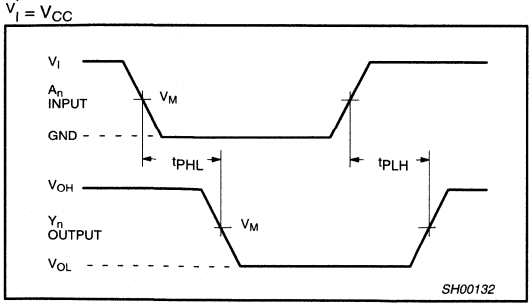
NOTES:
1. All typical values are measured T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

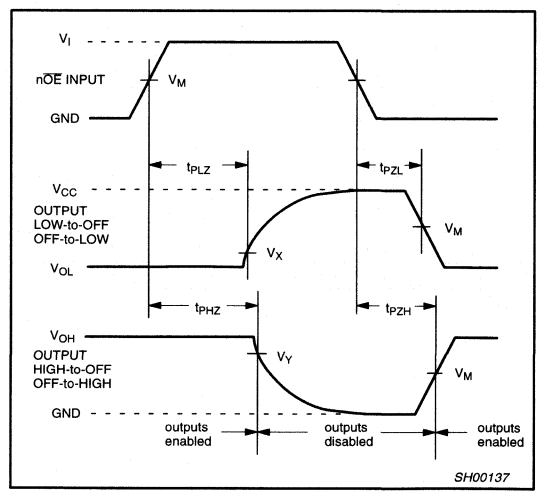
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

V_M = 1.5 V
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = 2.7V
$V_I = V_{CC}$

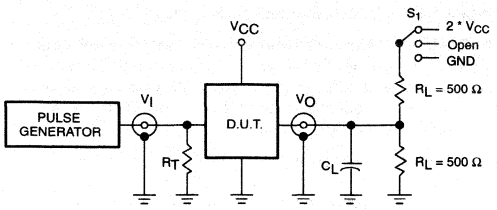


Waveform 1. Input (Dn) to output (Yn) propagation delay



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 3. Load circuitry for switching times

20-bit buffer/line driver, non-inverting (3-State) 74ALVCH16827

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Wide supply voltage range of 1.2V to 3.6V
- CMOS low power consumption
- Direct interface with TTL levels
- Universal bus transceiver with D-type latches and D-type flip-flops capable of operating in transparent, latched, clocked or clocked-enabled mode.
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Current drive ±24 mA at 3.0 V
- All inputs have bus hold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- 3-State non-inverting outputs for bus oriented applications

DESCRIPTION

The 74ALVCH16827 is a 20-bit non-inverting buffer/driver with 3-State outputs for bus oriented applications.

The 74ALVCH16827 consists of two 10-bit sections with separate output enable signals. For either 10-bit buffer section, the two output enable ($1\overline{OE}1$ and $1\overline{OE}2$ or $2\overline{OE}1$ and $2\overline{OE}2$) inputs must both be active. If either output enable input is high, the outputs of that 10-bit buffer section are in high impedance state.

The 74ALVCH16827 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.0 2.0	ns
C_I	Input capacitance			5	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Output enabled	20	pF
			Output disabled	3	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

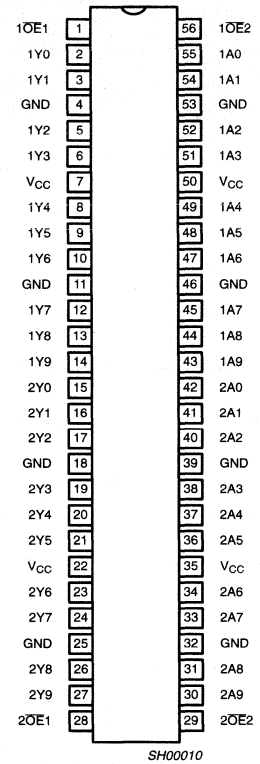
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16827 DGG	ACH16827 DGG	SOT364-1

PIN DESCRIPTION

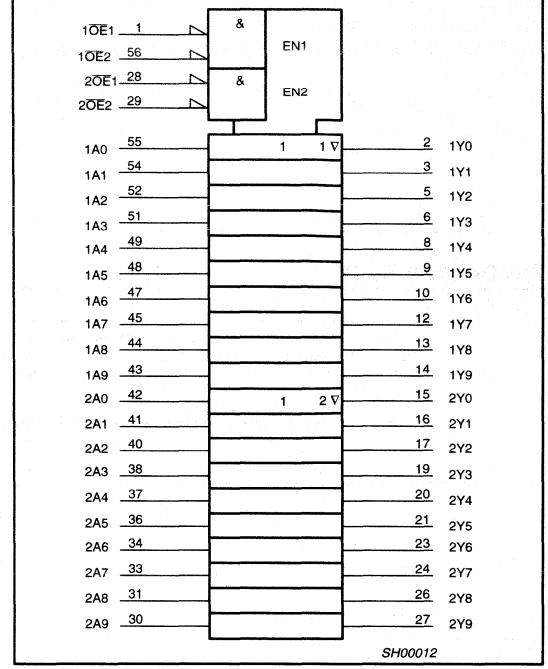
PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 - 1A9 2A0 - 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 - 1Y9 2Y0 - 2Y9	Data outputs
1, 56, 28, 29	$1\overline{OE}0$, $1\overline{OE}1$ $2\overline{OE}0$, $2\overline{OE}1$	Output enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION



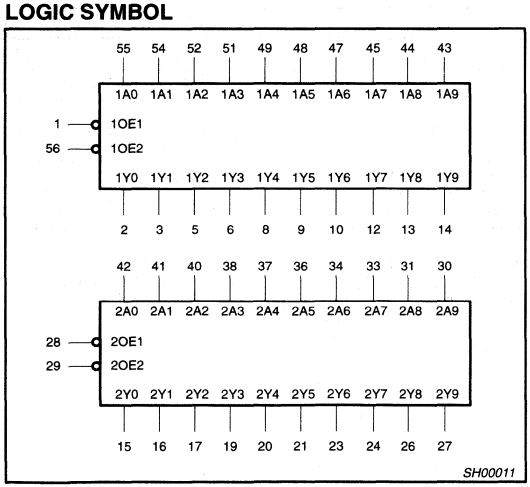
SH00010

LOGIC SYMBOL (IEEE/IEC)



SH00012

LOGIC SYMBOL



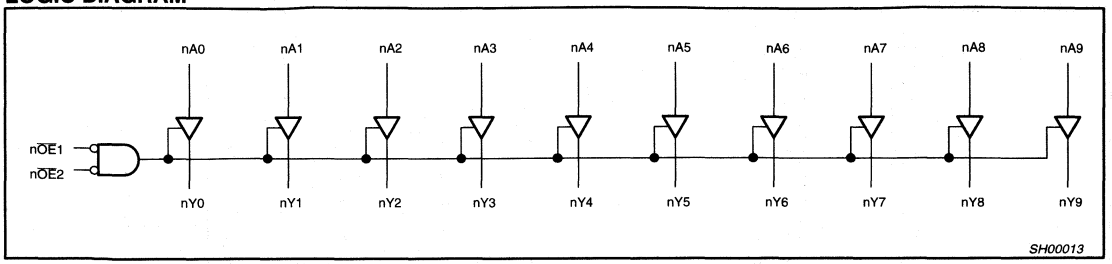
SH00011

FUNCTION TABLE

INPUTS			OUTPUTS
$n\overline{OE}1$	$n\overline{OE}2$	A	Y
L	L	L	L
L	L	H	H
H	H	X	Z
X	H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[2]	–0.5 to +4.6	V
		For data inputs[2]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 3.6V	500			µA
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 3.6V	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5 ± 0.2V			
			MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	2.0	4.1	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$n to nYn	2, 3	1.0	2.9	6.0	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$n to nYn	2,3	1.2	2.1	5.6	ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	2.0	3.4	1.0	2.1	3.9	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$n to nYn	2, 3	1.0	2.5	4.7	1.0	3.0	5.7	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$n to nYn	2, 3	1.3	2.8	4.5	1.3	3.1	4.9	ns

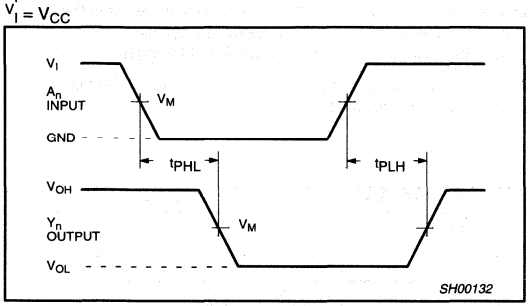
NOTES:
1. All typical values are at V_{CC} T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V.

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

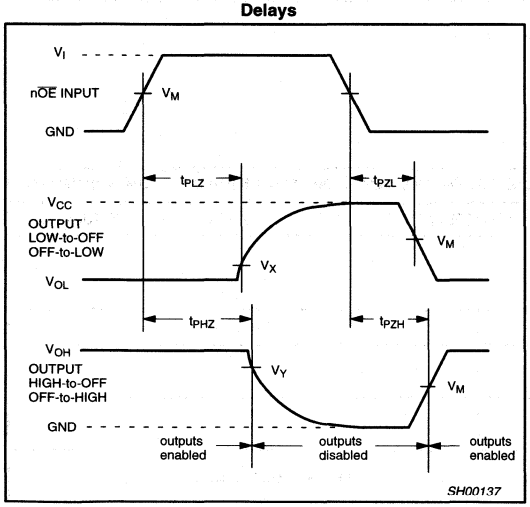
V_M = 0.5 V
$V_X = V_{OL}$ + 0.15V
$V_Y = V_{OH}$ –0.15V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

V_M = 1.5 V
$V_X = V_{OL}$ + 0.3V
$V_Y = V_{OH}$ –0.3V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = 2.7V
$V_I = V_{CC}$

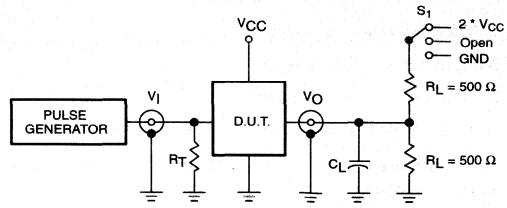


Waveform 1. The Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. The 3-State Output Enable and Disable Times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 3. Load circuitry for switching times

20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

74ALVCH162827

FEATURES

- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Output drive capability 50Ω transmission lines @ 85°C
- Integrated 30 Ω termination resistors

DESCRIPTION

The 74ALVCH162827 high-performance CMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ALVCH162827 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables (n$\overline{OE}$1, n$\overline{OE}$2) for maximum control flexibility.

The 74ALVCH162827 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers and bus receivers/transmitters.

To ensure the high impedance state during power up or power down, $\overline{OEBA}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.0 2.0	ns
C_I	Input capacitance			5	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Output enabled	20	pF
			Output disabled	3	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH162827 DGG	ACH162827 DGG	SOT364-1

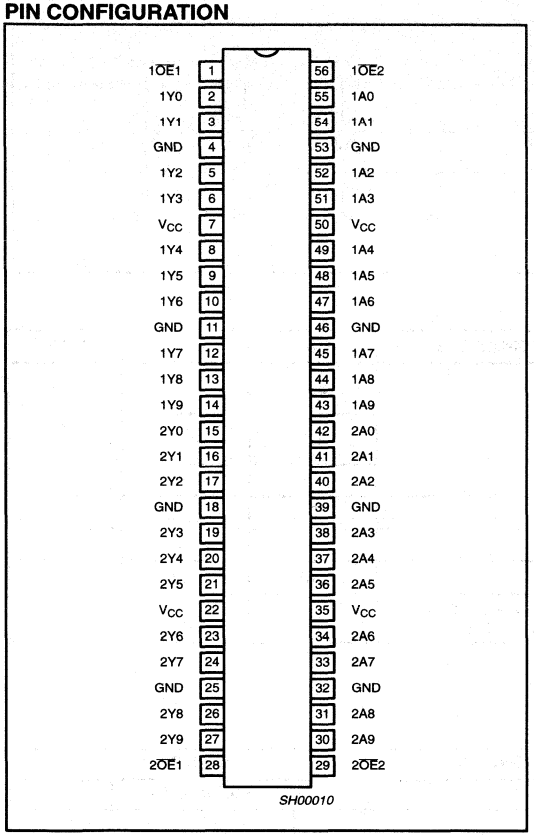
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	1A0 - 1A9 2A0 - 2A9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	1Y0 - 1Y9 2Y0 - 2Y9	Data outputs
1, 56, 28, 29	1$\overline{OE}$0, 1$\overline{OE}$1 2$\overline{OE}$0, 2$\overline{OE}$1	Output enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

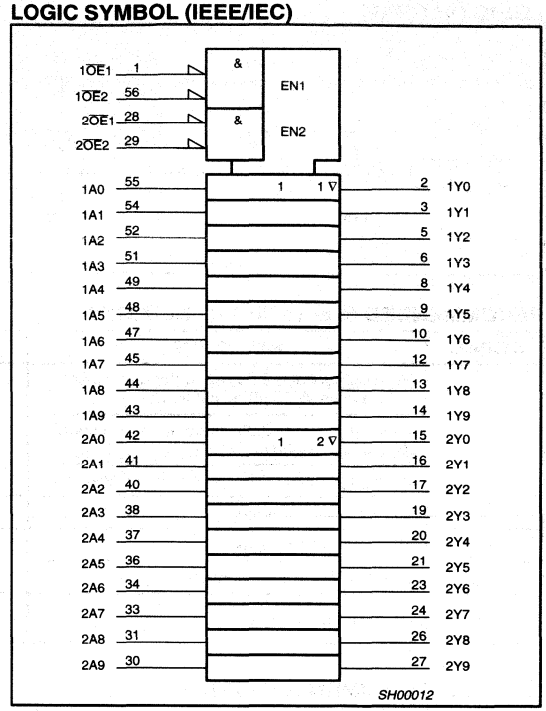
20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State)

74ALVCH162827

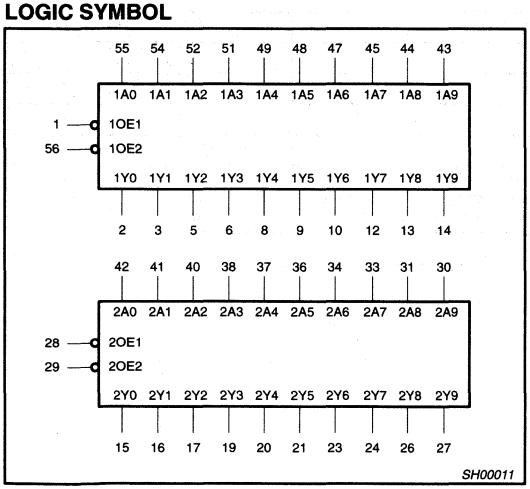
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



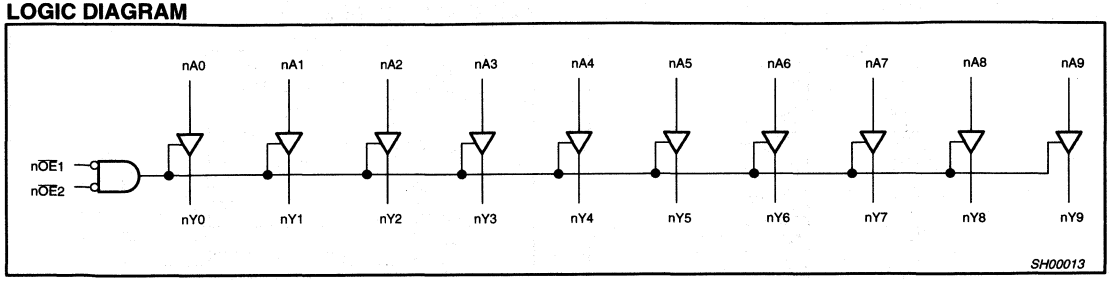
FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
nOEx	nAx	nYx	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

X = Don't care
Z = High impedance "off" state
H = High voltage level
L = Low voltage level

20-bit buffer/line driver, non-inverting, with 30Ω termination resistors (3-State) 74ALVCH162827

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 1	–0.5 to +4.6	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –4mA	V_{CC} – 0.4	V_{CC} – 0.11		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.6	V_{CC} – 0.17		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –4mA	V_{CC} – 0.5	V_{CC} – 0.09		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –8mA	V_{CC} – 0.7	V_{CC} – 0.19		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.6	V_{CC} – 0.13		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 1.0	V_{CC} – 0.27		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 4mA		0.07	0.40	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.11	0.55	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 4mA		0.06	0.40	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA		0.13	0.60	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.09	0.55	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.19	0.80	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA

NOTES:

1. All typical values are at T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5 ± 0.2V			
			MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3				ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$n to nYn	2, 3				ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$n to nYn	2,3				ns

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3							ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$n to nYn	2, 3							ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$n to nYn	2, 3							ns

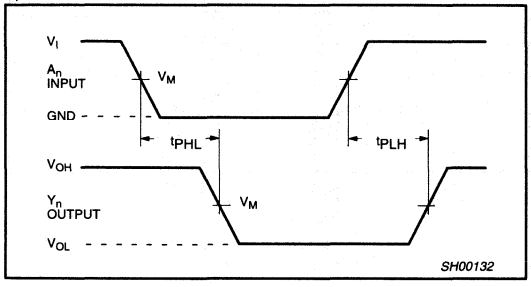
NOTES:
1. All typical values are at V_{CC} T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V.

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

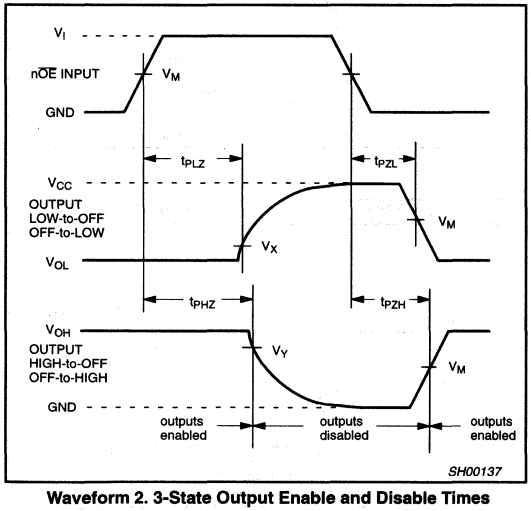
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$

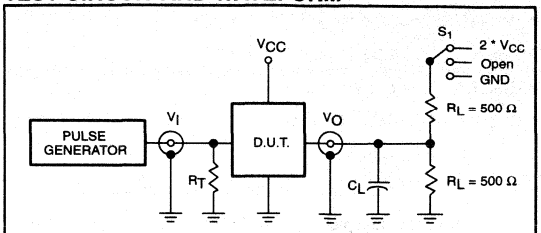


Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 3. Load circuitry for switching times

18-bit universal bus driver with 5V tolerant inputs (3-State)

74ALVC16835

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

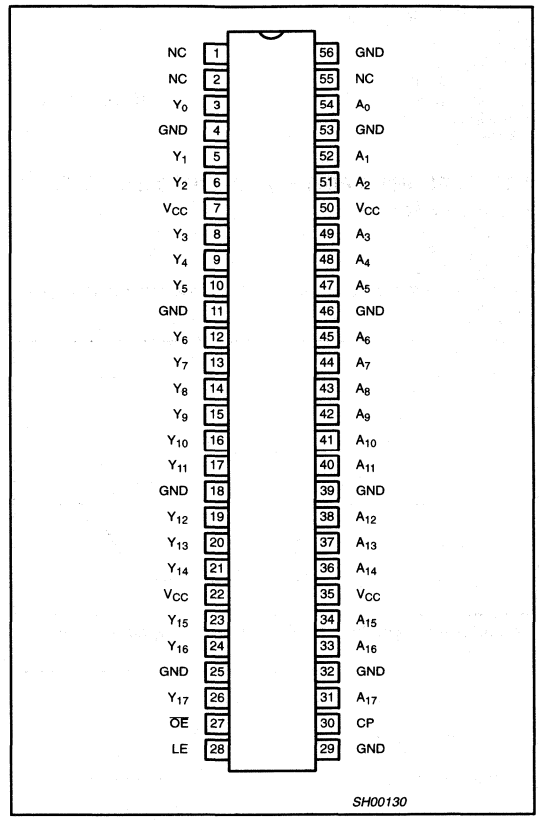
The 74ALVC16835 is a 18–bit universal bus driver. Data flow is controlled by output enable ($\overline{OE}$), latch enable (LE) and clock inputs (CP).

When LE is HIGH, the A to Y data flow is transparent. When LE is LOW and CP is held at LOW or HIGH, the data is latched; on the LOW to HIGH transient of CP the A–data is stored in the latch/flip-flop.

When $\overline{OE}$ is LOW the outputs are active. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF–state. Operation of the $\overline{OE}$ input does not affect the state of the latch/flip-flop.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Yn; LE to Yn; CP to Yn	V_{CC} = 3.3V, C_L = 50pF		2.3 2.6 2.5	ns
F_{max}	Maximum clock frequency	V_{CC} = 3.3V, C_L = 50pF		350	MHz
C_I	Input capacitance			4.0	pF
$C_{I/O}$	Input/Output capacitance			8.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	transparent mode Output enabled Output disabled	 13 3	pF
			Clocked mode Output enabled Output disabled	 22 15	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

18-bit universal bus driver with 5V tolerant inputs (3-State)

74ALVC16835

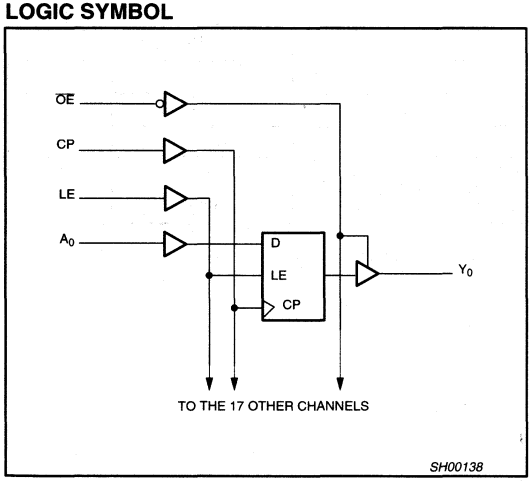
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74ALVC16835 DGG	AC16835 DGG	SOT364-1

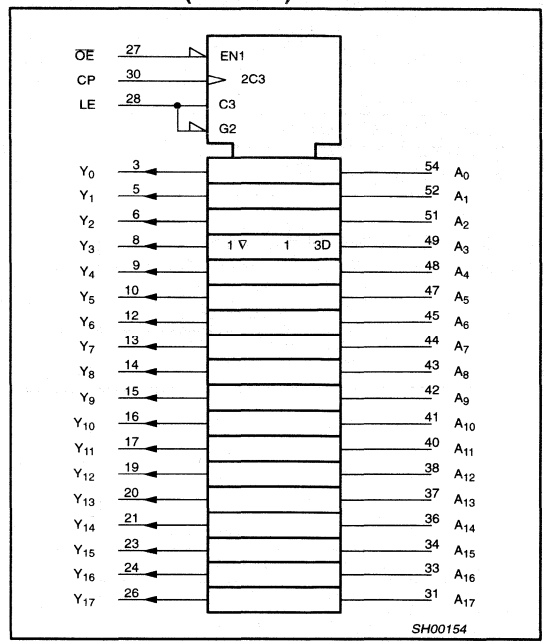
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 55	NC	No connection
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	Y_0 to Y_{17}	Data outputs
4, 11, 18, 25, 32, 39, 46, 53, 56	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}$	Output enable input (active LOW)
28	LE	Latch enable input (active HIGH)
30	CP	Clock input
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	A_0 to A_{17}	Data inputs

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}$	LE	CP	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y_0[1]
L	L	L	X	Y_0[2]

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state
↑ = LOW-to-HIGH level transition

NOTES:
1. Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.
2. Output level before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $I_O = -100\mu A$	$V_{CC} - 0.2$	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = -6mA$	$V_{CC} - 0.3$	$V_{CC} - 0.08$		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = -12mA$	$V_{CC} - 0.6$	$V_{CC} - 0.26$		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $I_O = -12mA$	$V_{CC} - 0.5$	$V_{CC} - 0.14$		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $I_O = -12mA$	$V_{CC} - 0.6$	$V_{CC} - 0.09$		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $I_O = -24mA$	$V_{CC} - 1.0$	$V_{CC} - 0.28$		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $I_O = 100\mu A$		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = 6mA$		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; $I_O = 12mA$		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; $I_O = 12mA$		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; $I_O = 24mA$		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; $I_O = 0$		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC} - 0.6V$; $I_O = 0$		150	750	µA

NOTES:

1. All typical values are at T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7V			
			MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay An to Yn	1, 8	1.0	2.4	4.2	ns
	Propagation delay LE to Yn	2, 8	1.0	2.8	5.0	
	Propagation delay CP to Yn	4, 8	1.0	2.8	5.0	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Yn	7, 8	1.0	2.2	4.0	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Yn	7,8	1.0	2.0	–	ns
t_W	CP pulse width HIGH or LOW	4, 8	2.0	–	–	ns
	LE pulse width HIGH	2, 8	2.0	–	–	
t_{SU}	Set-up time An to CP	6, 8	1.0	–	–	ns
	Set-up time An to LE	6, 8	1.5	–	–	
t_h	Hold time An to CP	3, 8	1.0	–	–	ns
	Hold time An to LE	3, 8	1.0	–	–	
F_{max}	Maximum clock pulse frequency	4, 8	150	300	–	MHz

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay An to Yn	1, 8	1.0	2.3	3.6	1.0	2.7	4.0	ns
	Propagation delay LE to Yn	2, 8	1.0	2.6	4.5	1.0	2.8	5.2	
	Propagation delay CP to Yn	4, 8	1.0	2.5	4.2	1.0	2.7	4.9	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Yn	7, 8	1.0	2.3	4.4	1.0	3.0	5.4	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Yn	7, 8	1.0	2.8	4.1	1.0	3.1	4.6	ns
t_W	CP pulse width HIGH or LOW	4, 8	2.0	–	–	2.0	–	–	ns
	LE pulse width HIGH	2, 8	2.0	–	–	2.0	–	–	
t_{SU}	Set-up time An to CP	6, 8	1.0	–	–	1.0	–	–	ns
	Set-up time An to LE	6, 8	1.5	–	–	1.5	–	–	
t_h	Hold time An to CP	3, 8	1.0	–	–	1.0	–	–	ns
	Hold time An to LE	3, 8	1.0	–	–	1.0	–	–	
F_{max}	Maximum clock pulse frequency	4, 8	150	300	–	200	350	–	MHz

NOTES:

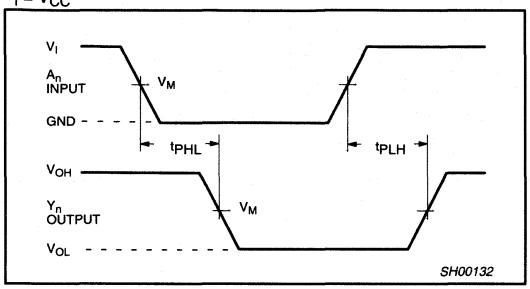
1. All typical values are measured T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

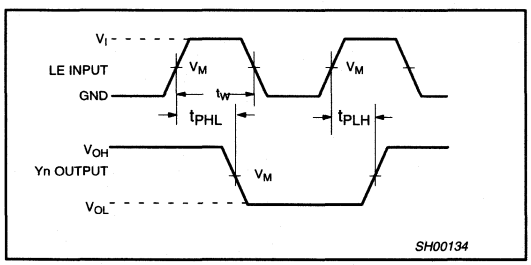
$V_M = 1.5\ V_{CC}$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

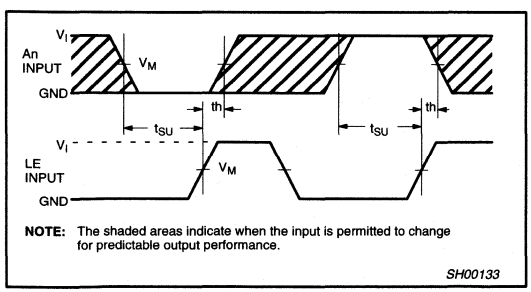
$V_M = 0.5\ V$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$



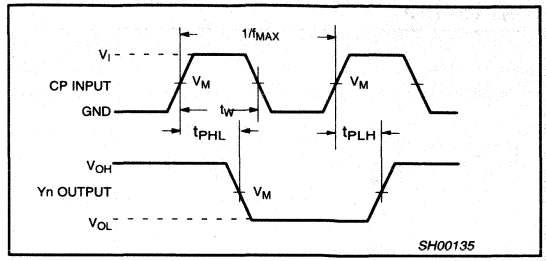
Waveform 1. Input (Dn) to output (Yn) propagation delay



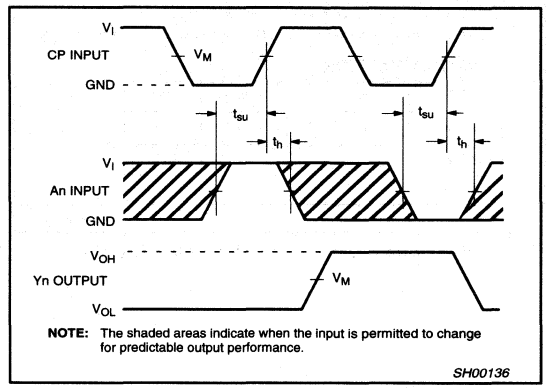
Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Yn) propagation delays.



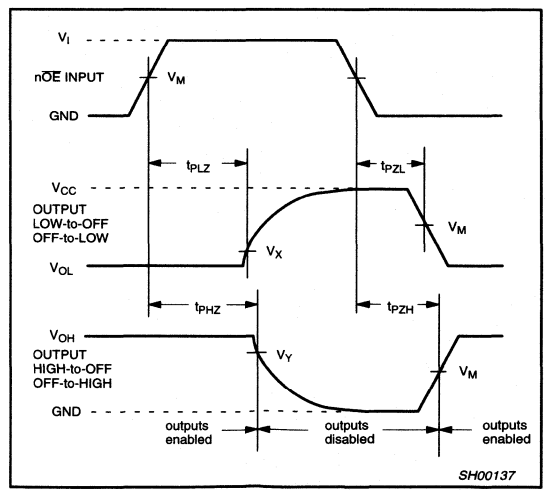
Waveform 3. Data set-up and hold times for the An input to the LE input



Waveform 4. The clock (CP) to Yn propagation delays, the clock pulse width and the maximum clock frequency.

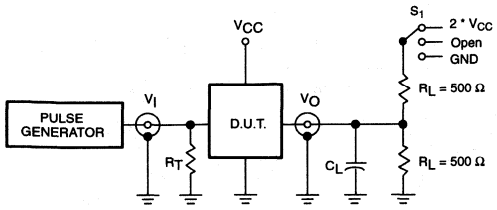


Waveform 5. Data set-up and hold times for the An input to the clock CP input



Waveform 6. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 7. Load circuitry for switching times

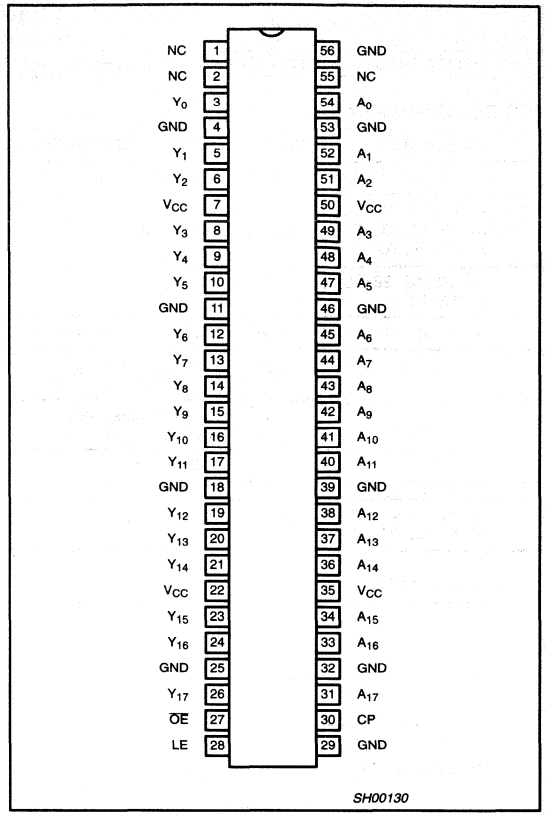
18-bit universal bus driver with 30Ω termination resistors and 5V tolerant inputs (3-State)

74ALVC162835

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Output drive capability 50Ω transmission lines @ 85°C
- Current drive ±24 mA at 3.0 V
- Integrated 30 Ω termination resistors

PIN CONFIGURATION



DESCRIPTION

The 74ALVC162835 is an 18-bit universal bus driver. Data flow is controlled by output enable (OE), latch enable (LE) and clock inputs (CP).

When LE is HIGH, the A to Y data flow is transparent. When LE is LOW and CP is held at LOW or HIGH, the data is latched; on the LOW to HIGH transient of CP the A-data is stored in the latch/flip-flop.

The 74ALVC162835 is designed with 30 Ω_series resistors in both HIGH or LOW output stages.

When $\overline{OE}$ is LOW the outputs are active. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latch/flip -flop.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Yn; LE to Yn; CP to Yn	V_{CC} = 3.3V, C_L = 50pF		2.9 3.5 3.3	ns
F_{max}	Maximum clock frequency	V_{CC} = 3.3V, C_L = 50pF		240	MHz
C_I	Input capacitance			4.0	pF
$C_{I/O}$	Input/Output capacitance			8.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	transparent mode Output enabled Output disabled	10 3	pF
			Clocked mode Output enabled Output disabled	21 15	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

18-bit universal bus driver with 30Ω termination resistors and 5V tolerant inputs (3-State)

74ALVC162835

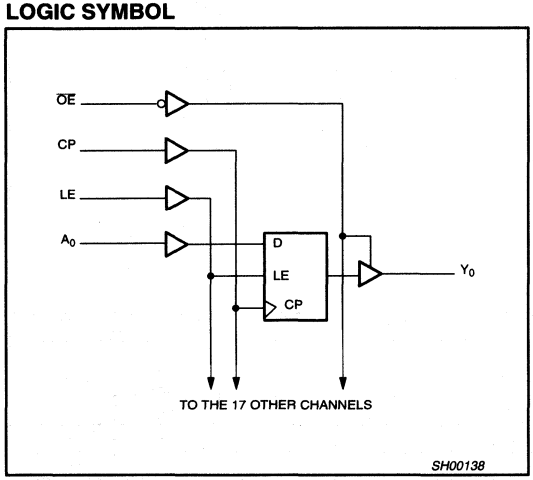
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74ALVC162835 DGG	AC162835 DGG	SOT364-1

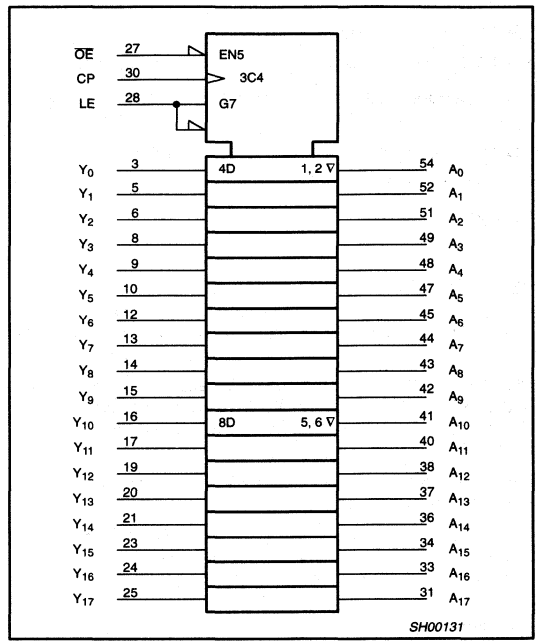
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 55	NC	No connection
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	Y_0 to Y_{17}	Data outputs
4, 11, 18, 25, 32, 39, 46, 53, 56	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}$	Output enable input (active LOW)
28	LE	Latch enable input (active HIGH)
30	CP	Clock input
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	A_0 to A_{17}	Data inputs

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}$	LE	CP	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y_0[1]
L	L	L	X	Y_0[2]

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state
↑ = LOW-to-HIGH level transition

NOTES:
1. Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.
2. Output level before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 1	–0.5 to +4.6	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –4mA	V_{CC} – 0.4	V_{CC} – 0.11		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.6	V_{CC} – 0.17		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –4mA	V_{CC} – 0.5	V_{CC} – 0.09		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –8mA	V_{CC} – 0.7	V_{CC} – 0.19		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.6	V_{CC} – 0.13		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 1.0	V_{CC} – 0.27		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 4mA		0.07	0.40	
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.11	0.55	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 4mA		0.06	0.40	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 8mA		0.13	0.60	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.09	0.55	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.19	0.80	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA

NOTES:

1. All typical values are at T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7V			
			MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay An to Yn	1, 7	1.0	3.5	5.0	ns
	Propagation delay LE to Yn	2, 7	1.3	4.1	5.9	
	Propagation delay CP to Yn	4, 7	1.4	4.0	6.3	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Yn	6, 7	1.4	3.8	6.3	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Yn	6, 7	1.0	2.6	4.7	ns
t_W	CP pulse width HIGH or LOW	4, 7	3.3	1.0	–	ns
	LE pulse width HIGH	2, 7	3.3	0.7	–	
t_{SU}	Set-up time An to CP	5, 7	2.2	0.2	–	ns
	Set-up time An to LE	5, 7	0.6	–0.1	–	
t_h	Hold time An to CP	3, 7	1.3	0.2	–	ns
	Hold time An to LE	3, 7	1.4	0.4	–	
F_{max}	Maximum clock pulse frequency	4, 7	150	190	–	MHz

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay An to Yn	1, 7	1.0	2.9	4.2	1.0	3.3	5.0	ns
	Propagation delay LE to Yn	2, 7	1.3	3.4	5.1	1.3	3.8	5.8	
	Propagation delay CP to Yn	4, 7	1.4	3.3	5.9	1.4	3.7	6.1	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Yn	6, 7	1.1	3.4	5.5	1.1	4.0	6.5	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Yn	6, 7	1.3	3.0	4.5	1.3	3.2	4.9	ns
t_W	CP pulse width HIGH or LOW	4, 7	3.3	0.7	–	3.3	1.2	–	ns
	LE pulse width HIGH	2, 7	3.3	0.6	–	3.3	0.6	–	
t_{SU}	Set-up time An to CP	5, 7	1.4	0.1	–	1.4	0.2	–	ns
	Set-up time An to LE	5, 7	1.5	0.2	–	1.5	0.2	–	
t_h	Hold time An to CP	3, 7	0.6	0.3	–	0.6	0.0	–	ns
	Hold time An to LE	3, 7	1.0	0.3	–	1.0	0.4	–	
F_{max}	Maximum clock pulse frequency	4, 7	150	240	–	150	190	–	MHz

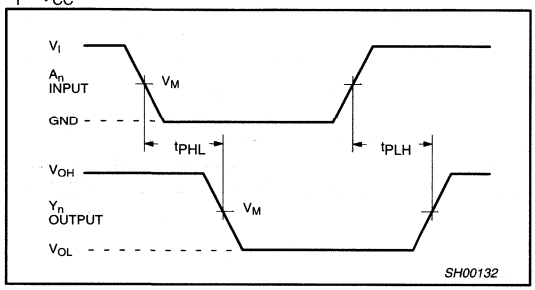
NOTES:
1. All typical values are measured T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

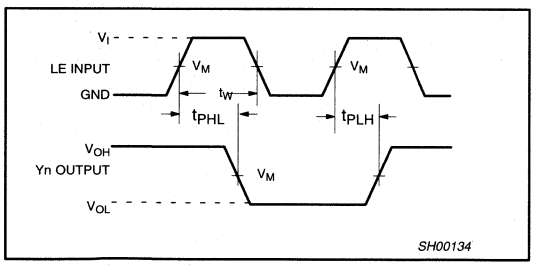
V_M = 1.5 V_{CC}
V_X = V_{OL} + 0.3V
V_Y = V_{OH} −0.3V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = 2.7V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

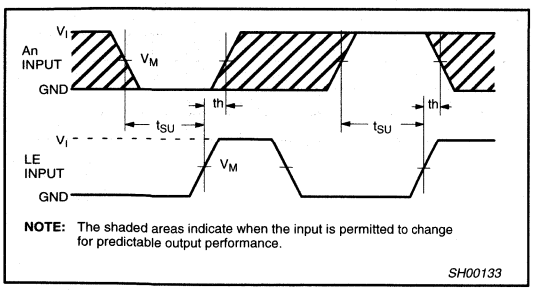
V_M = 0.5 V
V_X = V_{OL} + 0.15V
V_Y = V_{OH} −0.15V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = V_{CC}



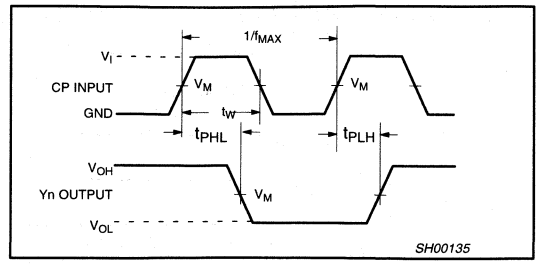
Waveform 1. Input (Dn) to output (Yn) propagation delay



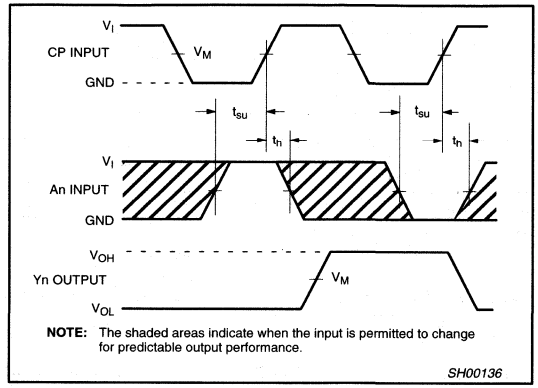
Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Yn) propagation delays.



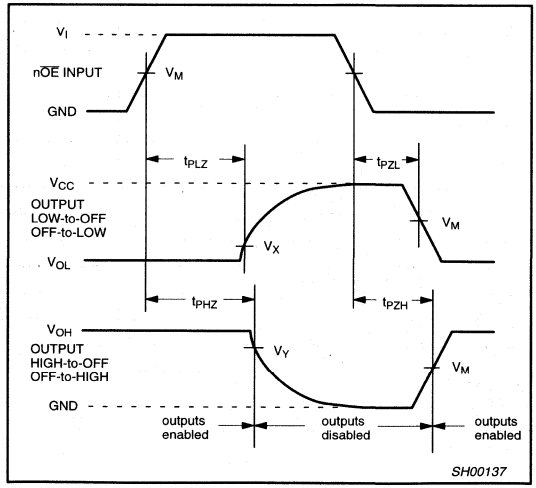
Waveform 3. Data set-up and hold times for the An input to the LE input



Waveform 4. The clock (CP) to Yn propagation delays, the clock pulse width and the maximum clock frequency.

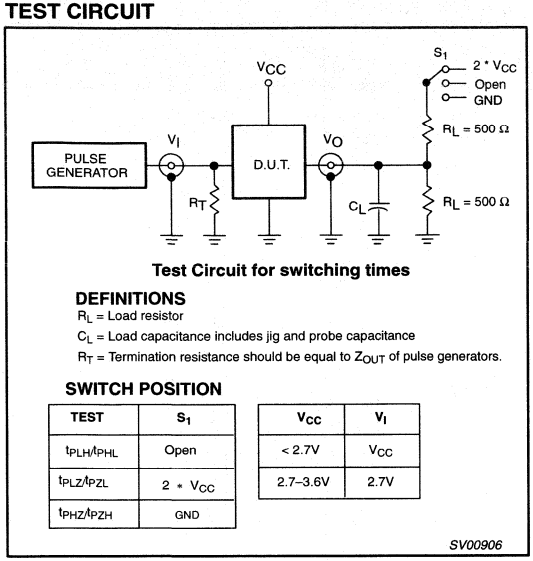


Waveform 5. Data set-up and hold times for the An input to the clock CP input



Waveform 6. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 7. Load circuitry for switching times

20-bit bus interface D-type latch (3-State) 74ALVCH16841

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Wide supply voltage range of 1.2V to 3.6V
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Current drive ±24 mA at 3.0 V
- All inputs have bus hold circuitry
- Output drive capability 50Ω transmission lines @ 85°C
- 3-State non-inverting outputs for bus oriented applications

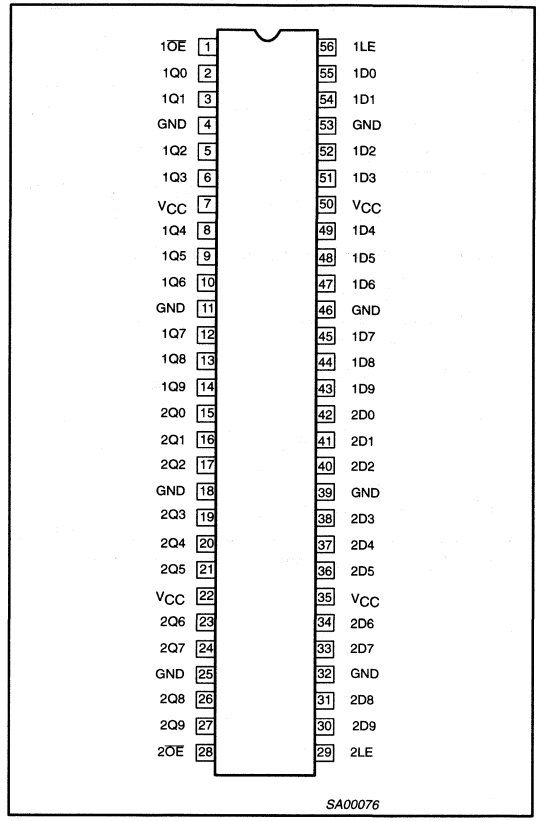
DESCRIPTION

The 74ALVCH16841 has two 10-bit D-type latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. The two sections of each register are controlled independently by the latch enable (nLE) and output enable ($n\overline{OE}$) control gates.

When $n\overline{OE}$ is LOW, the data in the registers appears at the outputs. When $n\overline{OE}$ is High the outputs are in High-impedance OFF state. Operation of the $n\overline{OE}$ input does not affect the state of the flip-flops.

The 74ALVCH16841 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

PIN CONFIGURATION



SA00076

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nD_n to nQ_n	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.5 2.4	ns
t_{PHL}/t_{PLH}	Propagation delay nLE to nQ_n	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.5 2.4	ns
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	Outputs enabled	19	pF
			Outputs disabled	3	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16841 DGG	ACH16841 DGG	SOT364-1

20-bit bus interface D-type latch (3-State) 74ALVCH16841

PIN DESCRIPTION

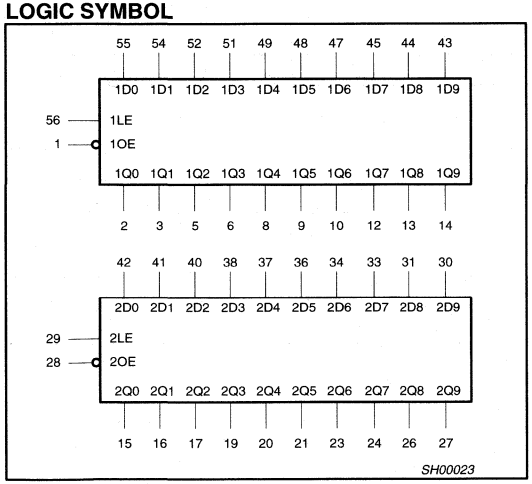
PIN NUMBER	SYMBOL	FUNCTION
1	$1\overline{OE}$	Output enable inputs (active-LOW)
56	1LE	Latch enable inputs (active HIGH)
55, 54, 52, 51, 49, 48, 47, 45, 44, 43	1D0 – 1D9	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13, 14	1Q0 – 1Q9	Data outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
28	$2\overline{OE}$	Output enable inputs (active-LOW)
29	2LE	Latch enable inputs (active HIGH)
42, 41, 40, 38, 37, 36, 34, 33, 31, 30	2D0 – 2D9	Data inputs
15, 16, 17, 19, 20, 21, 23, 24, 26, 27	2Q0 – 2Q9	Data outputs

FUNCTION TABLE

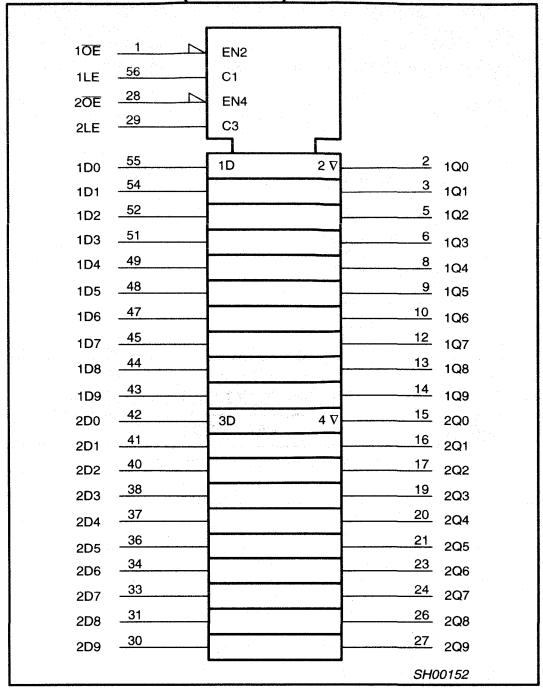
INPUTS			OUTPUT
$n\overline{OE}$	LE	Dx	Q
L	H	L	L
L	H	H	H
L	L	X	Q_0
H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

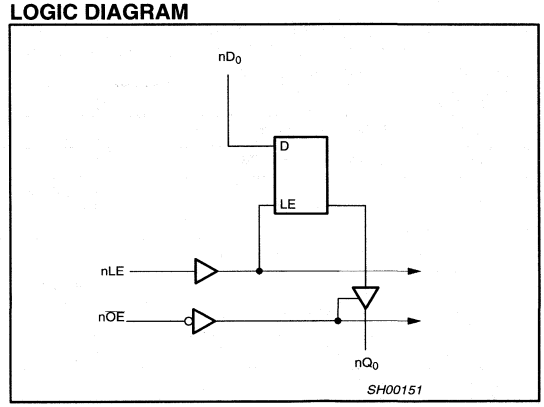
LOGIC SYMBOL



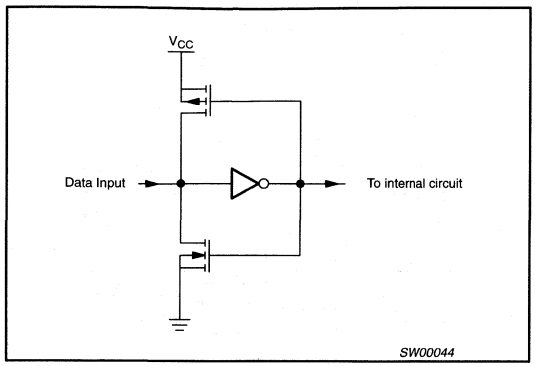
LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 3.6V	500			µA
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 3.6V	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7V			
			MIN	TYP[1]	MAX	
t_{PLH}/t_{PHL}	Propagation delay nD_n to nQ_n	1, 5	1.0	2.5	5.0	ns
t_{PLH}/t_{PHL}	Propagation delay nLE to nQ_n	2, 5	1.0	2.5	5.6	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nQ_n	4, 5	1.0	2.7	6.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nQ_n	4, 5	1.1	2.2	5.3	ns
t_W	nLE pulse width HIGH	2, 5	3.3	1.5	–	ns
t_{SU}	Set up time nD_n to nLE	3, 5	1.3	0.1	–	ns
T_h	Hold time nD_n to nLE	3, 5	1.4	0.3	–	ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PLH}/t_{PHL}	Propagation delay nD_n to nQ_n	1, 5	1.0	2.4	3.9	1.0	2.6	4.7	ns
t_{PLH}/t_{PHL}	Propagation delay nLE to nQ_n	2, 5	1.0	2.4	4.3	1.0	2.6	5.1	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nQ_n	4, 5	1.0	2.3	4.9	1.0	3.1	6.0	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nQ_n	4, 5	1.3	2.9	4.1	1.3	3.1	4.3	ns
t_W	nLE pulse width HIGH	2, 5	3.3	1.5	–	3.3	1.5	–	ns
t_{SU}	Set up time nD_n to nLE	3, 5	1.0	0.6	–	1.1	0.1	–	ns
t_h	Hold time nD_n to nLE	3, 5	1.4	0.2	–	1.7	0.2	–	ns

NOTES:

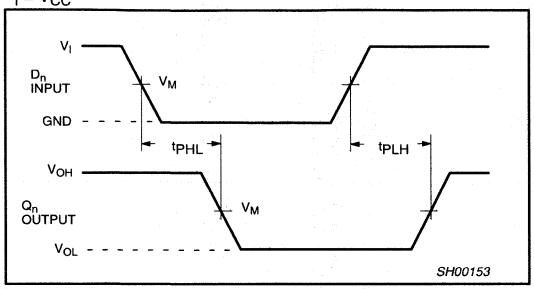
1. All typical values are measured T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

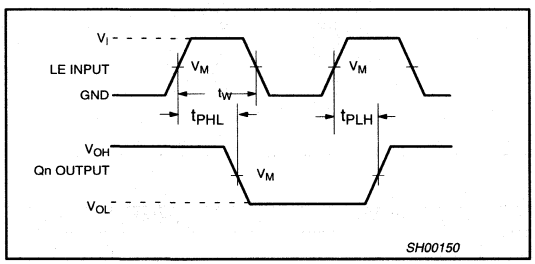
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} - 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

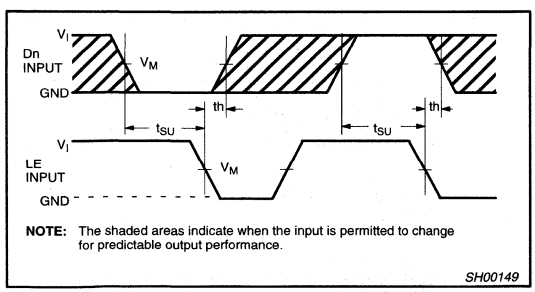
$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$
$V_I = V_{CC}$



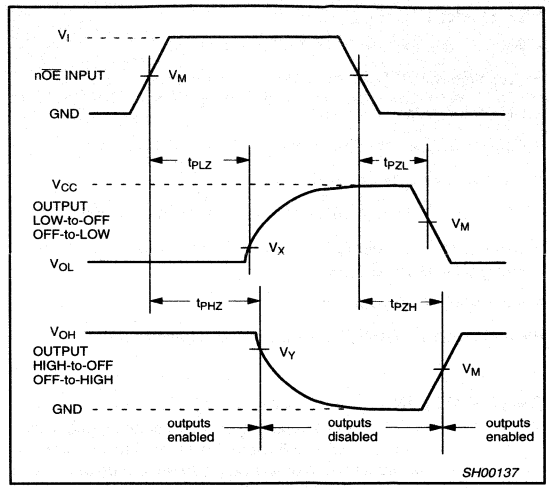
Waveform 1. The input (D_n) to output (Q_n) propagation delay



Waveform 2. The latch enable (LE) pulse width, the latch enable input to output (Q_n) propagation delay

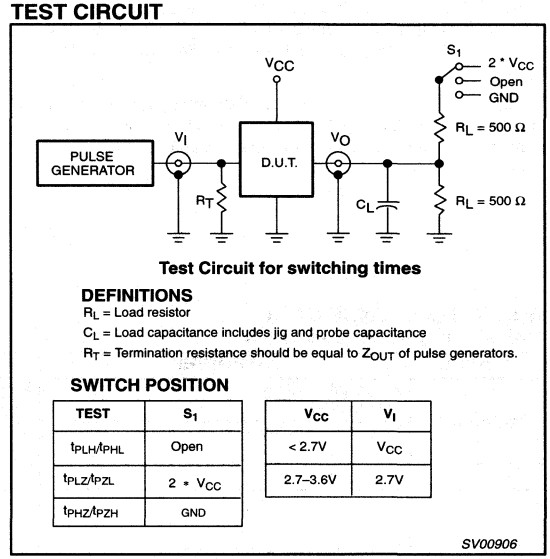


Waveform 3. The data set up and hold times for the D_n input to the LE input



Waveform 4. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

Waveform 5. Load circuitry for switching times

18-bit bus interface D-type latch (3-State) 74ALVCH16843

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C

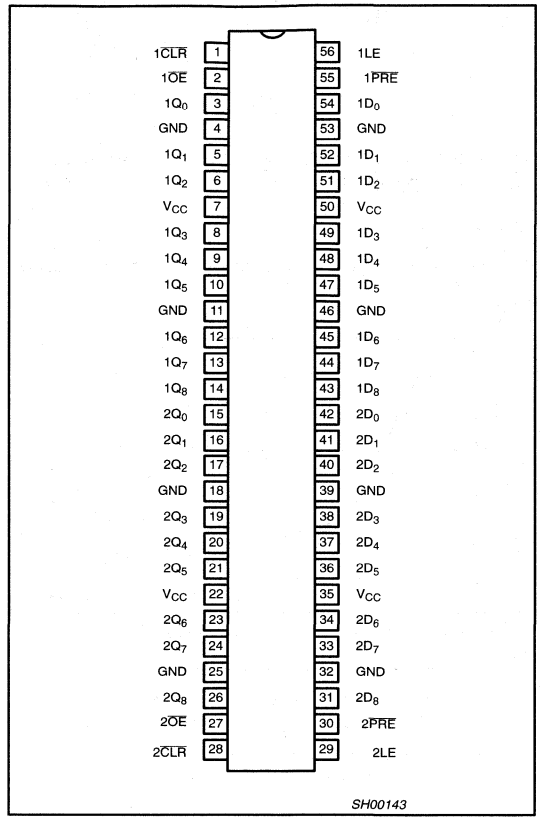
DESCRIPTION

The 74ALVCH16843 has two 9–bit D-type latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. The two sections of each register are controlled independently by the latch enable (nLE), clear (n$\overline{CLR}$), preset (n$\overline{PRE}$) and output enable (n$\overline{OE}$) control gates.

When n$\overline{OE}$ is LOW, the data in the registers appear at the outputs. When n$\overline{OE}$ is HIGH, the outputs are in the high impedance OFF state. Operation of the n$\overline{OE}$ input does not affect the state of the flip-flops.

The 74ALVCH16843 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

PIN CONFIGURATION



SH00143

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nDn to nQn	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.2 2.1	ns
	Propagation delay nLE to nQn	V_{CC} = 2.5V, C_L = 30pF V_{CC} = 3.3V, C_L = 50pF		2.3 2.0	ns
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	transparent mode Output enabled Output disabled	 17 3	pF
			Clocked mode Output enabled Output disabled	 19 9	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

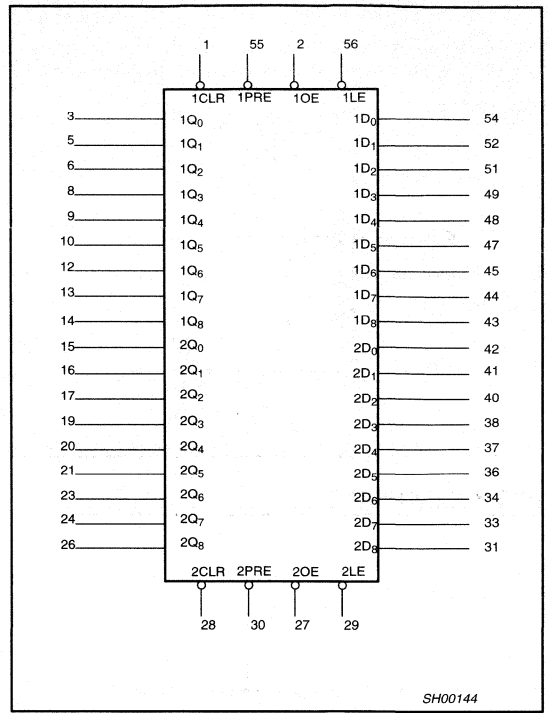
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74ALVCH16843 DGG	ACH16843 DGG	SOT364-1

18-bit bus interface D-type latch (3-State) 74ALVCH16843

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{CLR}$	Clear input (active LOW)
2	$1\overline{OE}$	Output enable input (active LOW)
55	$1\overline{PRE}$	Preset input (active LOW)
56	1LE	Latch enable input (active HIGH)
54, 52, 51, 49, 48, 47, 45, 44, 43	1D0 to 1D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14	1Q0 to 1Q8	Data outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$2\overline{OE}$	Output enable input (active LOW)
28	$2\overline{CLR}$	Clear input (active LOW)
29	2LE	Latch enable input (active HIGH)
30	$2\overline{PRE}$	Preset input (active LOW)
42, 41, 40, 38, 37, 36, 34, 33, 31	2D0 to 2D8	Data inputs
15, 16, 17, 19, 20, 21, 23, 24, 26	2Q0 to 2Q8	Data outputs

LOGIC SYMBOL

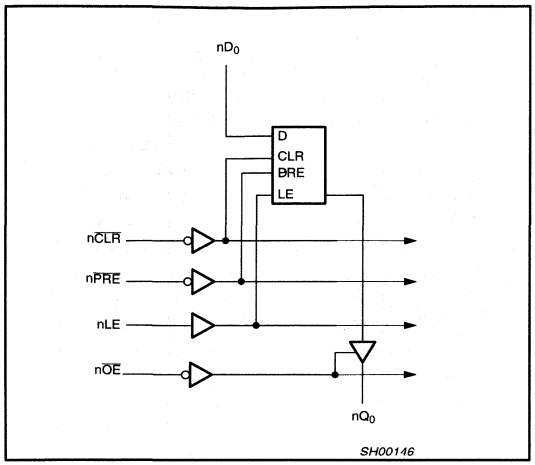


FUNCTION TABLE

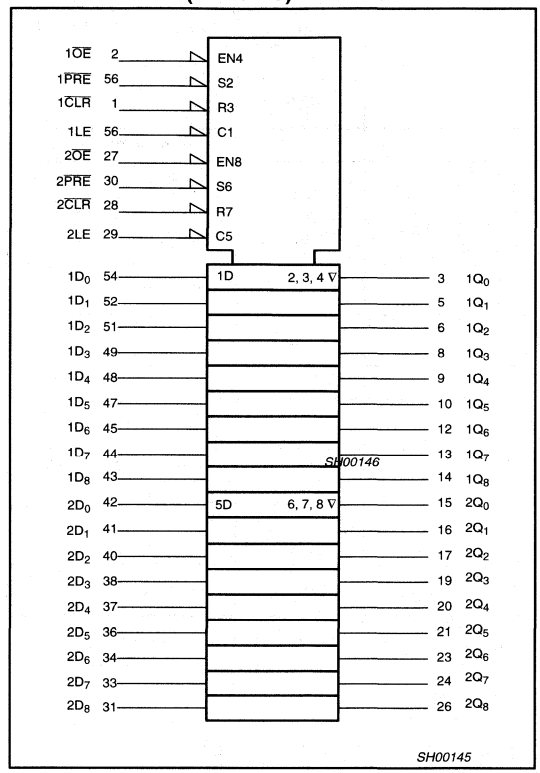
INPUTS					OUTPUT
$n\overline{PRE}$	$n\overline{CLR}$	$n\overline{OE}$	LE	D_X	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	H	X	Q_0
X	X	H	H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state

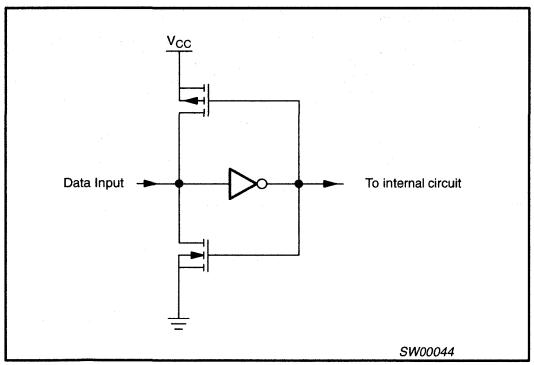
LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[2]	–0.5 to +4.6	V
		For data inputs[2]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; $V_I = V_{CC}$ – 0.6V; I_O = 0		150	750	µA
I_{BHL}[2]	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V	75	150		
I_{BHH}[2]	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V	–75	–175		
I_{BHLO}[2]	Bus hold LOW overdrive current	V_{CC} = 3.6V	500			µA
I_{BHHO}[2]	Bus hold HIGH overdrive current	V_{CC} = 3.6V	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7V			
			MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nDn to nQn	1, 6	1.0	2.2	4.3	ns
	Propagation delay nLE to nQn	2, 6	1.0	2.3	4.6	
	Propagation delay $n\overline{PRE}$ to nQn	1, 6	1.0	2.5	4.8	
	Propagation delay $n\overline{CLR}$ to nQn	1, 6	1.0	2.5	4.8	
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nQn	5, 6	1.0	2.8	5.8	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nQn	5, 6	1.1	2.2	4.3	ns
t_{SU}	Set-up time nDn to nLE	3, 6	0.5	–0.1	–	ns
t_h	Hold time nDn to nLE	3, 6	0.9	0.5	–	ns
t_W	nLE pulse width HIGH	2, 6	1.5	0.5	–	ns
	$n\overline{PRE}$ pulse width LOW	4, 6	1.5	0.5	–	
	$n\overline{CLR}$ pulse width LOW	4, 6	1.5	0.5	–	
t_{REM}	Recovery time $n\overline{PRE}$ to nLE	4, 6	0.5	1.1	–	ns
	Recovery time $n\overline{CLR}$ to nLE	4, 6	0.5	1.0	–	

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			V_{CC} = 3.3 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nDn to nQn	1, 6	1.0	2.1	3.5	1.0	2.3	4.0	ns
	Propagation delay nLE to nQn	2, 6	1.0	2.0	3.5	1.0	2.1	3.9	
	Propagation delay $n\overline{PRE}$ to nQn	1, 6	1.0	2.2	3.8	1.0	2.6	4.5	
	Propagation delay $n\overline{CLR}$ to nQn	1, 6	1.0	2.3	3.9	1.0	2.5	4.3	
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nQn	5, 6	1.0	2.5	4.4	1.0	3.0	5.3	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nQn	5, 6	1.3	2.6	4.0	1.3	2.8	4.4	ns
t_{SU}	Set-up time nDn to nLE	3, 6	0.5	0.0	–	0.5	–0.3	–	ns
t_h	Hold time nDn to nLE	3, 6	0.9	0.5	–	0.9	0.5	–	ns
t_W	nLE pulse width HIGH	2, 6	1.5	0.5	–	1.5	0.5	–	ns
	$n\overline{PRE}$ pulse width LOW	4, 6	1.5	0.5	–	1.5	0.6	–	
	$n\overline{CLR}$ pulse width LOW	4, 6	1.5	0.5	–	1.5	0.5	–	
t_{REM}	Recovery time $n\overline{PRE}$ to nLE	4, 6	1.0	0.4	–	0.8	–0.2	–	ns
	Recovery time $n\overline{CLR}$ to nLE	4, 6	0.8	0.2	–	0.6	–0.4	–	

NOTES:

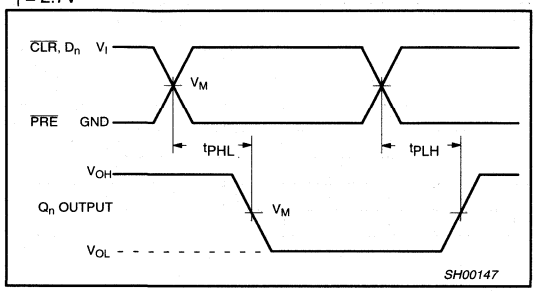
1. All typical values are measured T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

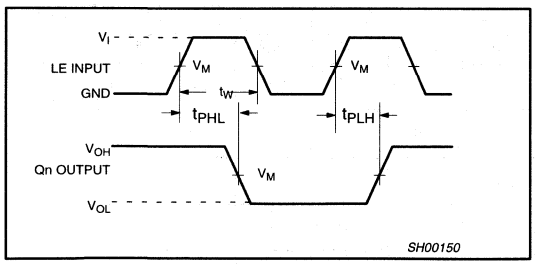
V_M = 0.5 V
$V_X = V_{OL}$ + 0.15V
$V_Y = V_{OH}$ –0.15V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

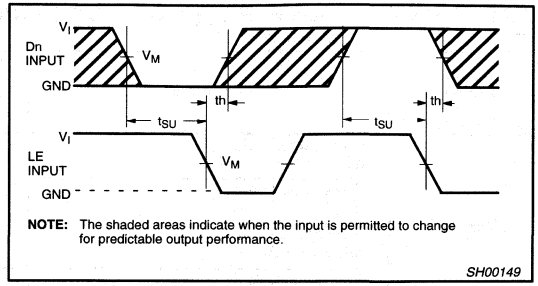
V_M = 1.5 V
$V_X = V_{OL}$ + 0.3V
$V_Y = V_{OH}$ –0.3V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = 2.7V



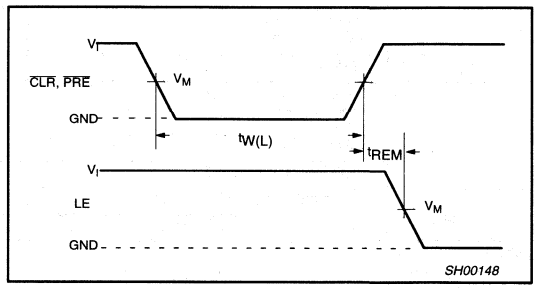
Waveform 1. Data input (Dn) to output (Qn), clear input ($\overline{CLR}$) to output (Qn) and preset input ($\overline{PRE}$) to output (Qn) propagation delay



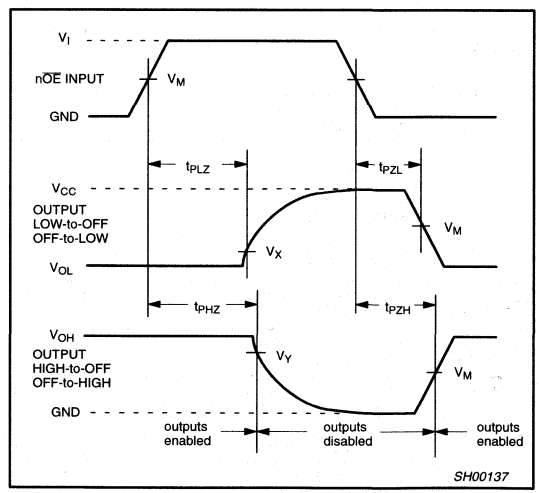
Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delay



Waveform 3. Data set-up and hold times for the Dn input to the LE input

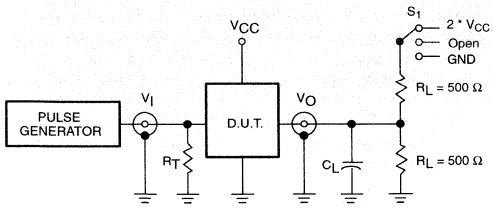


Waveform 4. Clear ($\overline{CLR}$) and preset ($\overline{PRE}$) pulse width, the clear ($\overline{CLR}$) and preset ($\overline{PRE}$) to latch (LE) removal time



Waveform 5. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 6. Load circuitry for switching times

16-bit registered transceiver (3-State) 74ALVCH16952

FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16952 consists of two sections, each containing a dual octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP_{XX}, where X is AB or BA) provided that the clock enable ($\overline{CE}_{XX}$) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the output enable input ($\overline{OE}_{XX}$) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f$ = 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CPnn, to An, Bn	V_{CC} = 3.3V, C_L = 50pF V_{CC} = 2.5V, C_L = 30pF	3.2	ns
f_{MAX}	Maximum clock frequency		350	MHz
C_I	Input capacitance		3.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	30	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVCH16952 DGG	ACH16952 DGG	SOT364-1

FUNCTION TABLE for register An or Bn

INPUTS			INTERNAL Q	OPERATING MODE
An or Bn	CP_{XX}	$\overline{CE}_{XX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

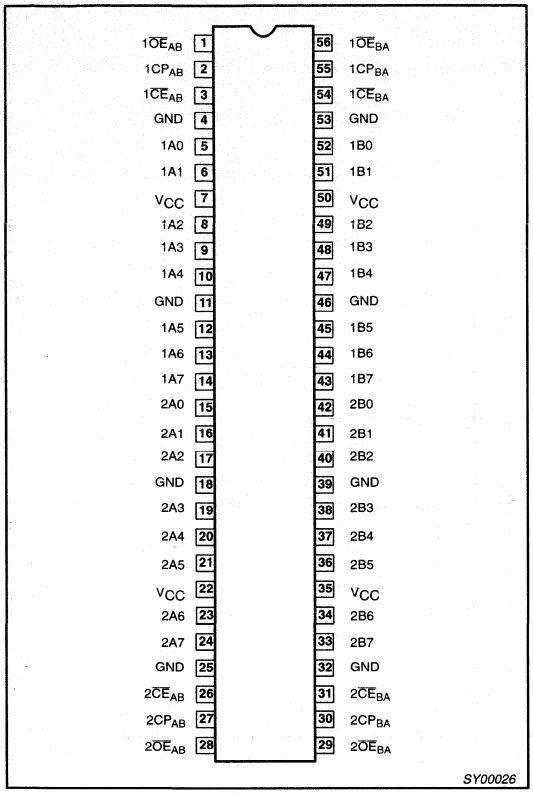
H = HIGH voltage level
L = LOW voltage level
↑ = LOW-to-HIGH transition

FUNCTION TABLE for output enable

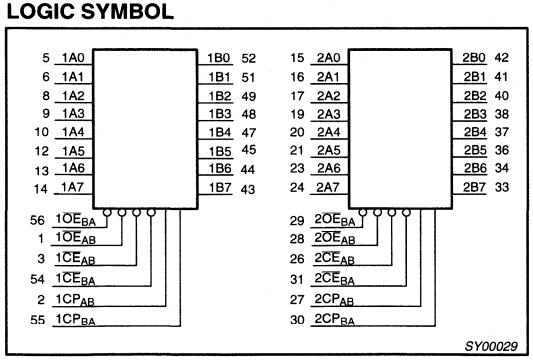
INPUTS	INTERNAL Q	An or Bn OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	Enable outputs

NC = no change
X = don't care
Z = high impedance OFF-state

PIN CONFIGURATION



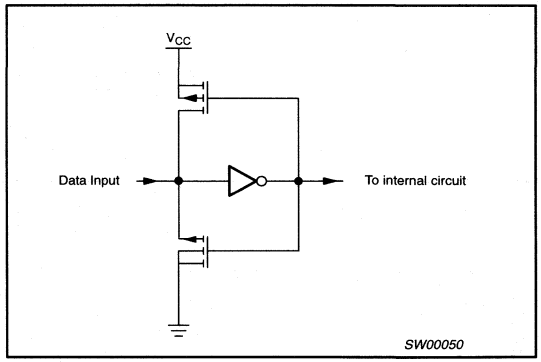
LOGIC SYMBOL



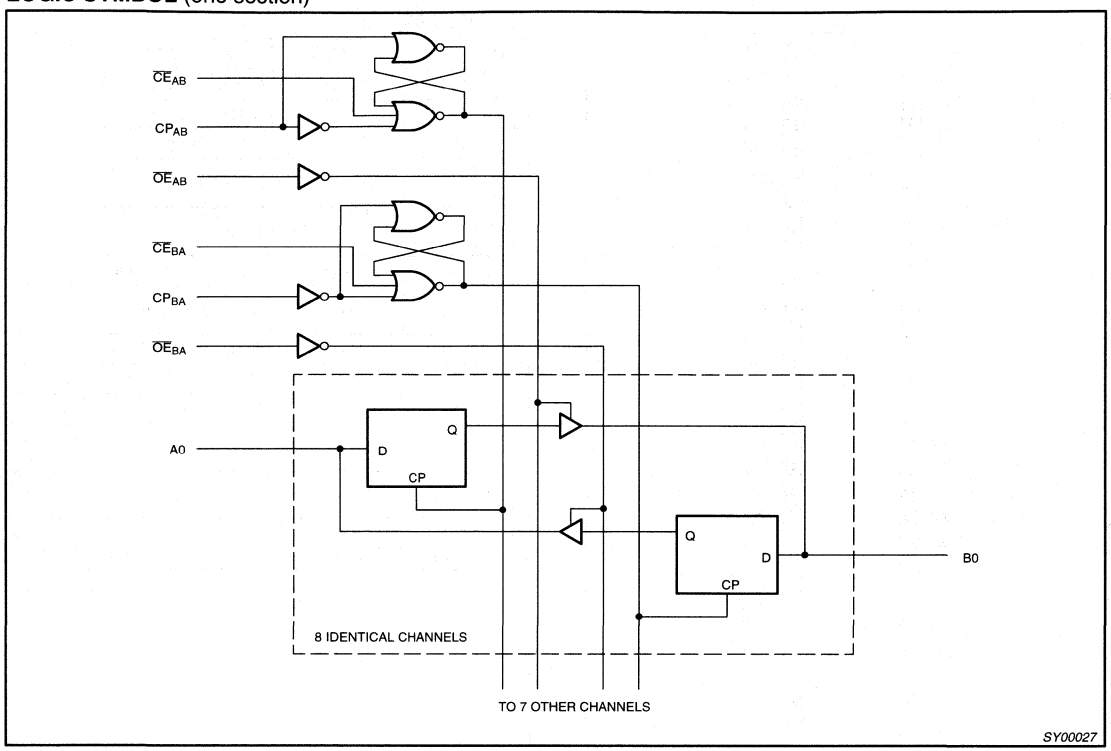
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	n$\overline{OE}_{AB}$	Output enable A-to-B
2, 27	nCP_{AB}	Clock input A-to-B
3, 26	n$\overline{CE}_{AB}$	A-to-B enable
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	Data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2B0 to 2B7	Data inputs/outputs
29, 56	n$\overline{OE}_{BA}$	Output enable B-to-A
30, 55	nCP_{BA}	Clock input B-to-A
31, 54	n$\overline{CE}_{BA}$	B-to-A enable
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	Data inputs/outputs

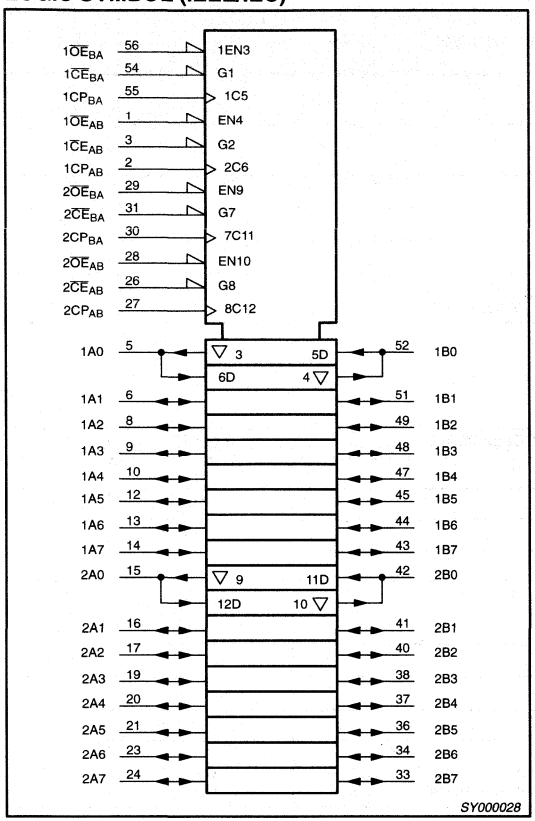
BUSHOLD CIRCUIT



LOGIC SYMBOL (one section)



LOGIC SYMBOL (IEEE/IEC)



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7V	1.7	1.2		V
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{iL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7V		1.2	0.7	V
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08		
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.26		
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC} – 0.09		
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.07	0.40	V
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.15	0.70	V
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND		0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.7 to 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6V; V_I = V_{CC} or GND; I_O = 0		0.2	40	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3V to 3.6V; V_I = V_{CC} – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 3.6V[2]	500			µA
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 3.6V[2]	–500			µA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.5V ± 0.2V			
			MIN	TYP	MAX	
t_{PLH}/t_{PHL}	Propagation delay nCP_{AB} to nBn, nCP_{BA} to nAn	3	1.0		4.1	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nAn, nBn	4	1.0		5.4	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAn, nBn	4	1.0		5.3	ns
t_W	Pulse width HIGH or LOW nCP_{AB}, nCP_{BA}	3	3.3			ns
t_{SU}	Set up time An or Bn before CP_{AB}	3	1.7			ns
	Set up time CE_{AB} or CE_{BA} before CP_{AB}	3	1.2			
t_h	Hold time An or Bn after CP_{AB}	3	0.6			ns
	Hold time An or Bn after CP_{AB}	3	1.1			
F_{max}	Maximum clock pulse frequency	3	150			MHz

NOTE:
1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f$ = 2.5ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay nCP_{AB} to nBn, nCP_{BA} to nAn	1, 4	1.0		3.9	1.0		4.6	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}$ to nAn, nBn	2, 4	1.0		4.4	1.0		5.3	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}$ to nAn, nBn	2, 4	1.1		4	1.4		4.4	ns
t_W	Pulse width HIGH or LOW nCP_{AB}, nCP_{BA}	3, 4	3.3			3.3			ns
t_{SU}	Set up time An or Bn before CP_{AB}	3, 4	1.5			1.9			ns
	Set up time CE_{AB} or CE_{BA} before CP_{AB}	3, 4	1			1			
t_h	Hold time An or Bn after CP_{AB}	3, 4	0.8			0.6			ns
	Hold time An or Bn after CP_{AB}	3, 4	1.1			0.9			
F_{max}	Maximum clock pulse frequency	1, 4	150			150			MHz

NOTES:
1. All typical values are at T_{amb} = 25°C.
2. V_{CC} = 3.3V

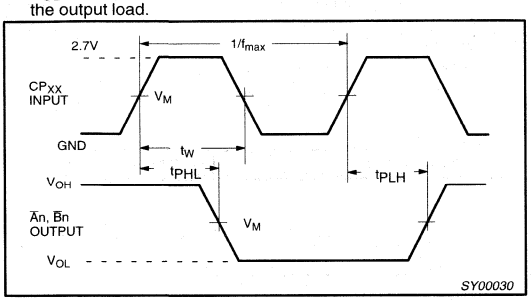
AC WAVEFORMS

V_{CC} = 2.3 TO 2.7 V RANGE

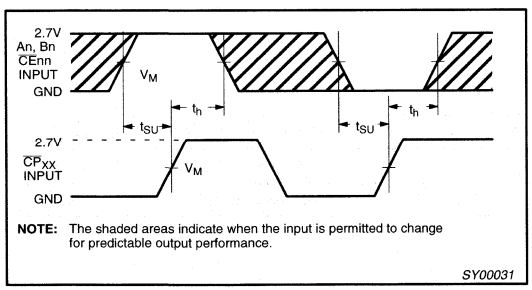
1. V_M = 0.5 V
2. $V_X = V_{OL}$ + 0.15V
3. $V_Y = V_{OH}$ – 0.15V
4. $V_I = V_{CC}$
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

V_{CC} = 3.0 TO 3.6 V RANGE AND V_{CC} = 2.7 V

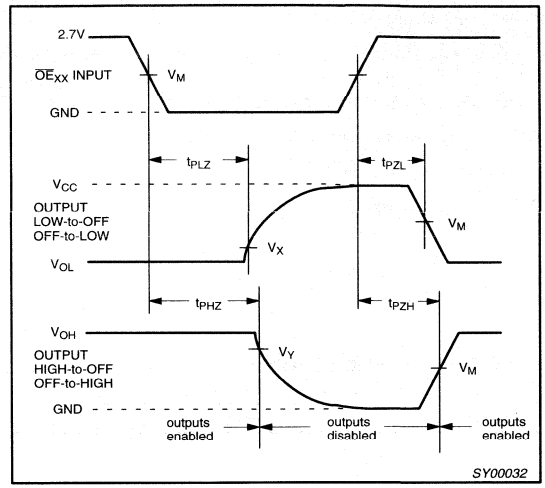
1. V_M = 1.5 V
2. $V_X = V_{OL}$ + 0.3V
3. $V_Y = V_{OH}$ – 0.3V
4. V_I = 2.7 V
5. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.



Waveform 1. Clock input (CP_{BA}, CP_{AB}) to output ($\overline{B}n$, $\overline{A}n$) propagation delays, the clock pulse width and the maximum clock pulse frequency.

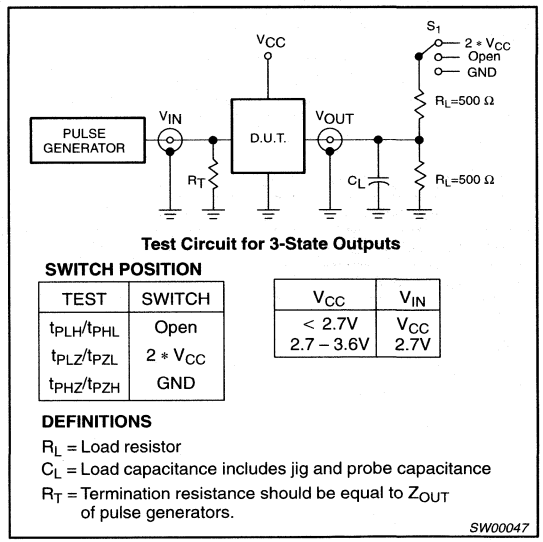


Waveform 2. Set-up and hold times for the An, Bn and $\overline{CE}_{XX}$ inputs.



Waveform 3. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Load circuitry for switching times

16-bit dual supply translating transceiver (3-State) 74ALVC164245

FEATURES

- Wide supply voltage range
  - A port: 1.2 to 3.6V
  - B port: 1.2 to 5.5V
- Complies with JEDEC standard no. 8-1A
- Control inputs voltage range from 2.7V to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74ALVC164245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC164245 is a 16-bit (dual-octal) translating transceiver and is designed to interface between a 5V bus and 3V bus in a mixed 3V/5V supply environment. This device can be used as two 8-bit transceivers or one 16-bit transceiver. The direction control inputs (1DIR, 2DIR) determine the direction of the data flow. nDIR (active HIGH) enables data from nA ports to nB ports. nDIR (active LOW) enables data from nB ports to nA ports. The output enable inputs ($1\overline{OE}$, $2\overline{OE}$), when HIGH, disable both nA and nB ports by placing them in a high impedance OFF-state. The nB ports interface with the 5V bus. The nA ports interface with the 3V bus. In suspend mode, when one of the supply voltages is zero, there will be no current flow from the non zero supply towards the zero supply. $V_{CC1} \geq V_{CC2}$ (except in suspend mode).

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nB nB to nA	C_L = 50pF V_{CC1} = 5.0V V_{CC2} = 3.3V	 3.7 3.1	ns
C_I	Input capacitance		5	pF
$C_{I/O}$	Input/output capacitance		10	pF
C_{PD}	Power dissipation capacitance	V_I = GND to V_{CC}[1]	20	pF

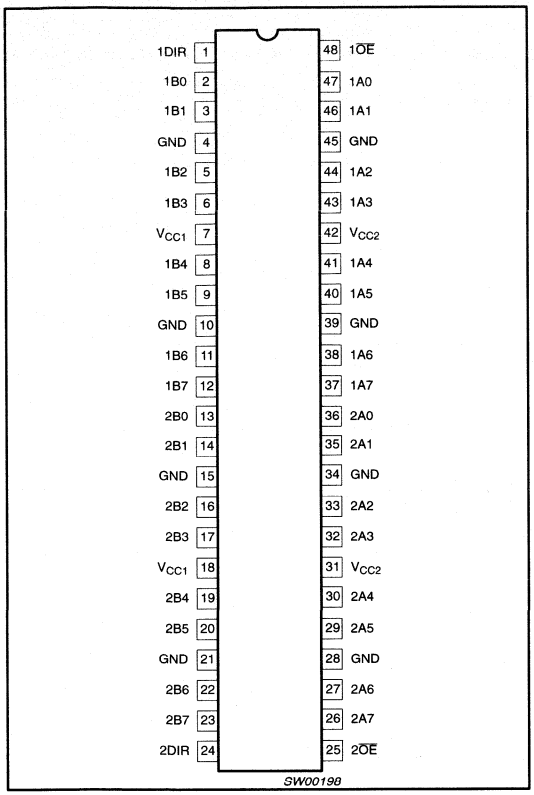
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

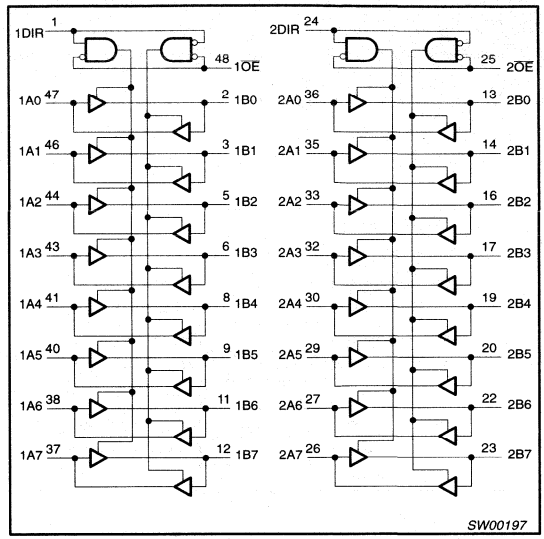
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74ALVC164245 DL	AC164245 DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74ALVC164245 DGG	AC164245 DGG	SOT362-1

PIN CONFIGURATION



LOGIC SYMBOL



FUNCTION TABLE

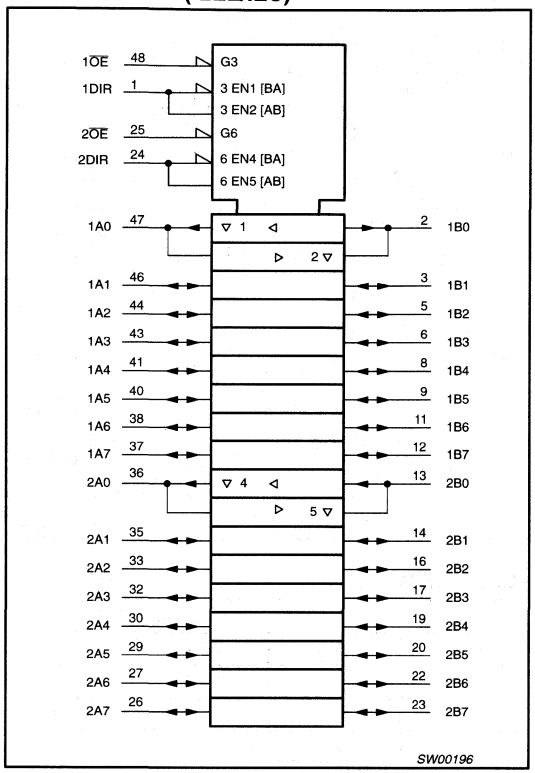
INPUTS		OUTPUTS	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	Direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	GND
7, 18	V_{CC1}	Positive supply voltage (5V bus)
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	Data inputs/outputs
24	2DIR	Direction control
25	$2\overline{OE}$	Output enable input (active LOW)
26, 27, 29, 30, 32, 33, 35, 36	2A7 to 2A0	Data inputs/outputs
31, 42	V_{CC2}	Positive supply voltage (3V bus)
37, 38, 40, 41, 43, 44, 46, 47	1A7 to 1A0	Data inputs/outputs
48	$1\overline{OE}$	Output enable input (active LOW)

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC1}	DC supply voltage (B Port)		–0.5 to +6.0	V
V_{CC2}	DC supply voltage (A Port)		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 3	–0.5 to +5.5	V
$V_{I/O}$	DC input voltage range for I/Os		–0.5 to V_{CC} +0.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 3	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–60 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink SO (SSOP) –plastic mini-pack (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC1}	DC supply voltage (for max. speed performance) (B Port)	$V_{CC1} \geq V_{CC2}$	2.7	5.5	V
V_{CC2}	DC supply voltage (for max. speed performance) (A Port)	$V_{CC1} \geq V_{CC2}$	2.7	3.6	V
V_{CC1}	DC supply voltage (for low-voltage applications) (B Port)	$V_{CC1} \geq V_{CC2}$	1.5	5.5	V
V_{CC2}	DC supply voltage (for low-voltage applications) (A Port)	$V_{CC1} \geq V_{CC2}$	1.5	3.6	V
V_I	DC Input voltage range		0	5.5	V
$V_{I/O}$	DC Input voltage range for I/Os	A Port	0	V_{CC2}	V
$V_{I/O}$	DC Output voltage range for I/Os	B Port	0	V_{CC1}	V
V_O	DC Output voltage range	A Port	0	V_{CC2}	V
V_O	DC Output voltage range	B Port	0	V_{CC1}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC2} = 2.7 to 3.0V V_{CC2} = 3.0 to 3.6V V_{CC1} = 3.0 to 4.5V V_{CC1} = 4.5 to 5.5V	0 0 0 0	20 10 20 10	ns/V

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage (B Port)	V_{CC} = 4.5 to 5.5V (Note 2)	2.0			V
	HIGH level Input voltage (A Port)	V_{CC} = 2.7 to 3.6V (Note 2)	2.0			
V_{IL}	LOW level Input voltage (B Port)	V_{CC} = 4.5 to 5.5V (Note 2)			0.8	V
	LOW level Input voltage (A Port)	V_{CC} = 2.7 to 3.6V (Note 2)			0.8	
V_{OH}	HIGH level output voltage (B Port)	V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 0.8			
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			
	HIGH level output voltage (A Port)	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –24mA	V_{CC} – 1.0			
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.6	V_{CC}		
V_{OL}	LOW level output voltage (B Port)	V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	V
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
		V_{CC} = 4.5V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	
	LOW level output voltage (A Port)	V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA			0.55	
		V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND Control pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins (B Port)	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND		±0.1	±15	µA
	Input current for common I/O pins (A Port)	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND		±0.1	±15	
I_{CC}	Quiescent supply current (B Port)	V_{CC} = 5.5V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	µA
	Quiescent supply current (A Port)	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.2	40	
ΔI_{CC}	Additional quiescent supply current per input pin (B Port)	V_{CC} = 4.5V to 5.5V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA
	Additional quiescent supply current per control pin (A Port)	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	

NOTES:
1. All typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V and T_{amb} = 25°C.
2. If V_{CC2} <2.7V, the switching levels at all inputs are not TTL compatible.

AC CHARACTERISTICS

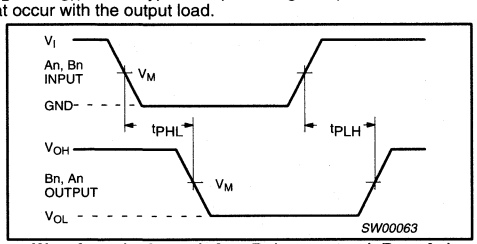
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC1} = 5.0V ±0.5V V_{CC2} = 3.3V ±0.3V		V_{CC1} = 5.0V ±0.5V V_{CC2} = 2.7V		
			MIN	MAX	MIN	MAX	
t_{PHL} t_{PLH}	Propagation delay nAn to nBn	1	1	5.8		5.9	ns
t_{PHL} t_{PLH}	Propagation delay nBn to nAn	1	1.2	5.8		6.7	ns
t_{PZH} t_{PZL}	3-State output enable time n$\overline{OE}$ to nAn	2	1	8.9		9.3	ns
t_{PZH} t_{PZL}	3-State output enable time n$\overline{OE}$ to nBn	2	2.1	9.5		9.2	ns
t_{PHZ} t_{PLZ}	3-State output disable time n$\overline{OE}$ to nAn	2	2	9.1		10.2	ns
t_{PHZ} t_{PLZ}	3-State output disable time n$\overline{OE}$ to nBn	2	2.9	8.6		9	ns

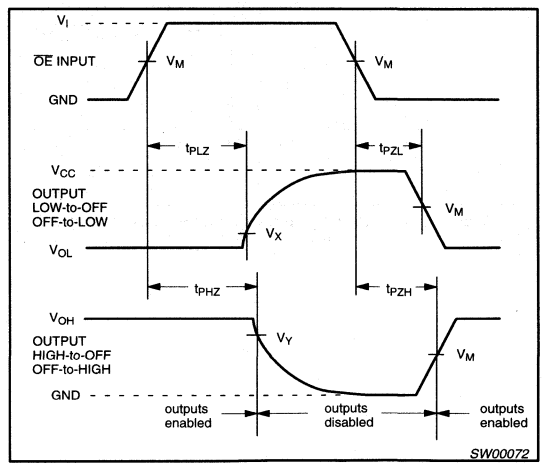
NOTE:
1. All typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V and T_{amb} = 25°C.
2. All typical values are at V_{CC1} = 5.0V, V_{CC2} = 2.7V and T_{amb} = 25°C.

AC WAVEFORMS

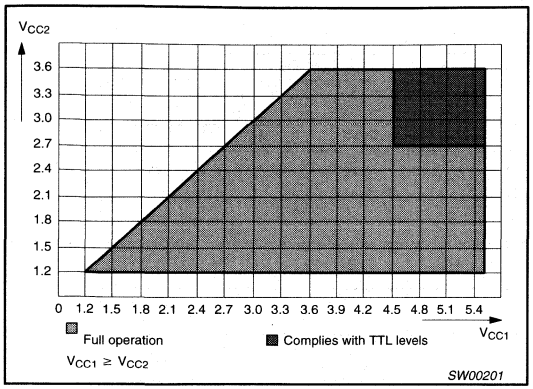
V_M = 1.5V at $V_{CC} \leq$ 3.6V
V_M = 0.5 * V_{CC1} at $V_{CC1} \geq$ 4.5V.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \leq$ 3.6V
$V_X = V_{OL} + 0.1 * (V_{OH} - V_{OL})$ at $V_{CC1} \geq$ 4.5V
$V_Y = V_{OH}$ –0.3V at $V_{CC} \leq$ 3.6V
$V_Y = V_{OH} - 0.1 * (V_{OH} - V_{OL})$ at $V_{CC1} \geq$ 4.5V
V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load.



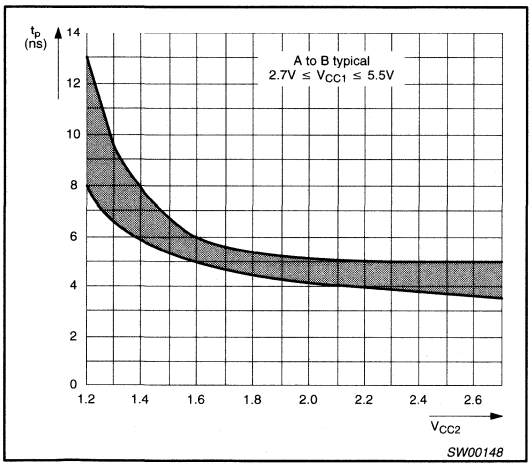
Waveform 1. Input (nAn,nBn) to output (nBn, nAn) propagation delays



Waveform 2. 3-State enable and disable times

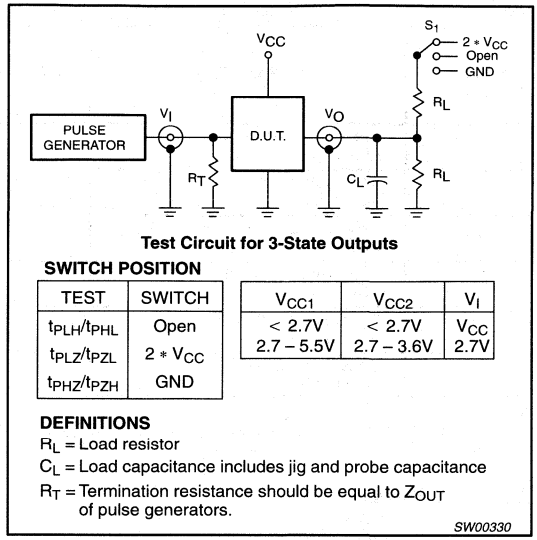


Waveform 3. Supply operating area



Waveform 4. Propagation delay as a function of the supply voltage, V_{CC2}

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 * V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC1}	V_{CC2}	V_I
< 2.7V	< 2.7V	V_{CC}
2.7 – 5.5V	2.7 – 3.6V	2.7V

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00330

Waveform 5. Load circuitry for switching times

Section 6
Application Notes

Advanced Low Voltage CMOS Logic

CONTENTS

Ground and V_{CC} Bounce of High-Speed Integrated Circuits AN223

Author: Mike Stevens

INTRODUCTION

The purpose of this paper is to give a general description of what ground and V_{CC} bounce are, why it is they are tested, and a detailed description of how they are tested.

WHY SHOULD GROUND AND V_{CC} BOUNCE BE TESTED?

Ground and V_{CC} bounce testing is done to evaluate what effect switching more than one output simultaneously has on the performance of the integrated circuit. This effect becomes important in any high-performance line of circuits because the propagation delays and output edge rates are very fast. This can cause ground bounce and V_{CC} bounce, described as Voltage Output Low Peak (V_{OLP}) and Voltage Output High Valley (V_{OHV}), respectively.

Fast edge rates of the output drivers can team up with internal parasitic lead inductance and the output load to produce unwanted side effects of noise on the outputs. This noise or ringing will occur on both a static and a switching output. This ringing can be substantial enough to cross the input triggering threshold of a subsequent device, which in turn can cause a system to perform unpredictably and unreliably.

GENERAL CONSIDERATIONS

There are two factors to consider when testing ground and V_{CC} bounce: the test fixture and test methods. Both are of equal importance for accuracy, repeatability, and correlation.

These tests determine the magnitude of the peaks and valleys on the low and high static output levels during multiple output switching. V_{OHV} refers to the minimum voltage "valley" on an output in the high level state. V_{OLP} refers to the maximum voltage "peak" on an output in the low level state. Figure 5 shows a typical example of what V_{OLP} and V_{OHV} look like, and also defines the points where V_{OLP} and V_{OHV} are measured.

For circuits with a single output or a single complementary output, the circuit is set up so that the pin under test is switching and the V_{OLP} and V_{OHV} levels are then measured at the points on the waveform as shown in Figure 5.

The most accurate way to determine the actual voltage dropped across the package lead inductance is to measure the magnitude of the ringing while the tested output is in the steady state. To evaluate the worst case, the V_{CC} should be at the maximum operating range, usually 5.5V, which will produce the highest V_{OH} levels. The higher V_{OH} level will create more dynamic switching current to flow through the lead inductance and produce a larger voltage ring on the outputs.

For further information see references.

GROUND BOUNCE METHOD

V_{OLP} is usually evaluated on the output pin furthest from the ground pin with the longest package lead length. The static output is in the low state and the switching outputs going from high to low. Examine the waveform and record the level of V_{OLP} as defined by Figure 5.

V_{OLP} should not be evaluated on the output adjacent to the ground pin. Mutual lead inductance will effectively reduce the magnitude of the output ringing by a factor of two.

V_{CC} BOUNCE METHOD

V_{OHV} is usually evaluated on the output pin furthest from the V_{CC} pin with the longest package lead length. The static output is in the high state and the switching outputs going from low to high. Examine the waveform and record the level of V_{OHV} as defined by Figure 5.

V_{OHV} should not be evaluated on the output adjacent to the ground pin. Mutual lead inductance will effectively reduce the magnitude of the output ringing by a factor of two.

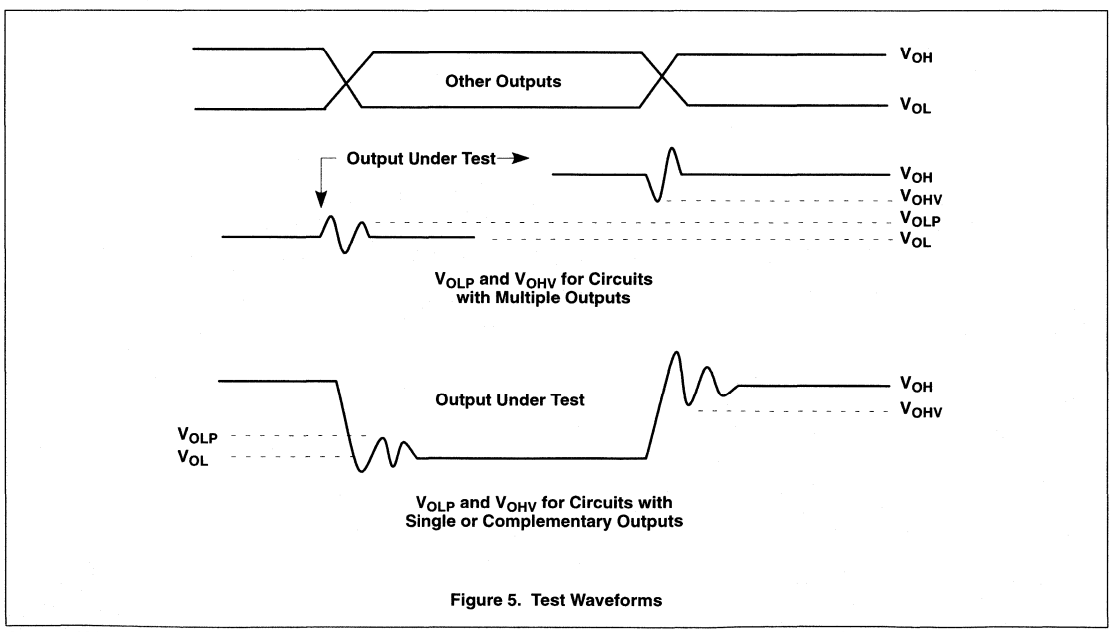


Figure 5. Test Waveforms

Ground and V_{CC} Bounce of High-Speed Integrated Circuits AN223

V_{OLP} VS. V_{IN} METHOD

Set up the V_{OLP} test and sweep the static input from 0.0V to 1.5V in 100mV increments, taking measurements at each point. Comparison data can be taken on a variety of ICs using the same set-up and test fixture. Plotting this data in graph form will show how the ICs compare with each other for input noise sensitivity during simultaneous switching. The same test can be performed on V_{CC} bounce.

TEST FIXTURES AND SET UP PROCEDURES

Refer to Table 1 for a complete list of test equipment and hardware. The test fixture will be the same one used for standard AC testing. This is a high-frequency PC board fixture featuring adequate internal ground and V_{CC} planes as well as 50Ω micro strip line for all signal paths and close proximity loading. The test fixture should have V_{CC} decoupling of at least 100µF, 0.1µF, 0.01µF and 1000pF. For a complete discussion of fixturing requirements including grounding, bypassing and general high-frequency testing requirements refer to the Application Note entitled "Testing and Specifying FAST Logic" (FAST Data Manual: AN202) and "Printed Circuit Board Test Fixtures for High-Speed Logic" (ABT Data Manual: AN602).

Pulse Generator Set Up

(Refer to "Test Circuit and Waveforms" in the appropriate data book for voltage levels and edge rates.)

Voltage levels: V_{IH}=3.0V, V_{IL}=0.0V
Threshold voltage levels: V_{IH}=2.5V, V_{IL}=0.5V
Rise and fall times: (t_R/t_F) = 2.5ns (10% to 90%)
Frequency: 1MHz @ 50% duty cycle

The pulse generator should be set up to provide simultaneous switching of the input signals. ("Simultaneous" is defined as all the input pins of the device seeing a given signal at the same moment in time.)

The preferred method is to drive each input with a separate pulse generator channel. Each input signal should be terminated with 50Ω resistor as close to the input pin as possible. The Tektronix HFS9009 data generator provides channel delays with 1ps resolution on the edge placement accuracy. The input skew from channel to channel should be set up with a maximum limit of ±50ps, but the target is less than ±30ps. The greater the input skew is, the worse the correlation will be. For example, using ±100ps produces about 50mV error (5%) for V_{OLP} and ±250ps produces about 100mV error (10%) for V_{OLP}. Therefore, it becomes very important to use a tight input skew to produce accurate and repeatable data.

The second method is to use a ganged type configuration, where one pulse generator signal is used to drive all inputs. This method is employed when the number of device inputs exceeds the number of pulse generator channels. The input signal should be terminated with 50Ω and then branched out equally to all inputs needing the input signal. Line lengths from the termination to the device pin should be kept as short as possible and of equal lengths. The input edge rates should be as close as possible to the data manual specifications.

General Set Up

All outputs should be loaded with the standard 50pF, 500Ω AC load.

When applicable, plots should be taken on at least one part and data values should be taken on three parts. The one part used for plots should have typical characteristics for the sample as a whole.

V_{CC} BOUNCE TESTING

Voltage Output High Valley (V_{OHV})

Measure the V_{OHV} level on an output held high during simultaneous switching. (Non-storage type devices only.)

The output to be evaluated for V_{OHV} should be the pin farthest from the V_{CC} pin. If there are two equidistant pins, record data on both outputs and plot only the worst-case output. Also, if more than one mode/path exists, all should be checked, but only the worst case tested. The output should be evaluated on the Low to High transition of the switching outputs.

1. V_{CC} = 5.5V, Temp = –55°C and V_{CC} = 5.0V, Temp = 25°C
2. Three parts are tested and plots should be taken on one of the parts.
3. The input conditions should be set so that the output under test is a static high.
4. Switch the remaining outputs simultaneously from low to high and record V_{OHV}.
5. Plot waveforms of a switching input, the high output, and a switching output.

Repeat steps 4 through 5 for the following other modes:

- High to Low
- 3-State to Low (if possible)
- Low to 3-State (if possible)
- High to 3-State (if possible)
- 3-State to High (if possible)

GROUND BOUNCE TESTING

Voltage Output Low Peak (V_{OLP})

Measure the V_{OLP} level on an output held low during simultaneous switching. (Non-storage type devices only.)

Table 17. Equipment Requirements (Hardware)

DEVICE	CHARACTERISTICS	MODEL
Digital Oscilloscope	1GHz bandwidth, 50Ω channels and cables	TEK11402
Data Generator	36 channel, 1ps edge placement resolution	TEK HFS9009
Temperature Forcing Unit	-55°C to +125°C (Thermonics)	T2420
Power Supply	4 channel, 0V–20V @ 5A	HP6632A
Test Fixture	High frequency (900MHz); Controlled 50Ω impedance; Full ground and V_{CC} planes; Sufficient V_{CC} decoupling (Chip caps and Tantalum caps)	SIG SD8807.27

Ground and V_{CC} Bounce of High-Speed Integrated Circuits AN223

GROUND BOUNCE TESTING Voltage Output Low Peak (V_{OLP}) (CONTINUED)

The output to be evaluated for V_{OLP} should be the pin farthest from the Ground pin. If there are two equidistant pins, record data on both outputs and plot only the worst-case output. Also, if more than one mode/path exists, all should be checked, but only the worst case tested. The output should be evaluated on the High to Low transition of the switching outputs.

1. V_{CC} = 5.5V, Temp = –55°C
   V_{CC} = 5.0V, Temp = 25°C
2. Three parts are tested and plots should be taken on one of the parts.
3. The input conditions should be set so that the output under test is a static low.
4. Switch the remaining outputs simultaneously from high to low and record V_{OLP}.
5. Plot waveforms of a switching input, the low output, and a switching output.

Repeat steps 4 through 5 for the following other transitions:

- Low to High
- 3-State to Low (if possible)
- Low to 3-State (if possible)
- High to 3-State (if possible)
- 3-State to High (if possible)

NOISE IMMUNITY COMPARISON TESTING V_{OLP} VS. V_{IN}

Set up the V_{OLP} test and measure V_{OLP} while incriminating the static input voltage. (Non-storage type devices only).

The output to be evaluated for V_{OLP} should be the pin farthest from the ground pins. If there are two equidistant pins, record data on the worst-case output. Also, if more than one mode/path exists, all should be checked, but only the worst case tested. The output should be evaluated on the falling edge of the switching outputs.

1. V_{CC} = 5.5V, Temp = –55°C and
   V_{CC} = 5.0V, Temp = 25°C
2. One part of each variety to be tested.
3. Evaluate V_{OLP} while the other outputs switch simultaneously from high to low.
4. Increment V_{IN} on the static input from 0.0V to 1.5V in 100mV increments and record V_{OLP} at each increment. Graph data for all parts as V_{OLP} vs. V_{IN} (V_{IN} on X axis, and V_{OLP} on the Y axis). Use a power supply output to drive the static input.

As long as the testing set-up and the fixture are identical, this graph will show an accurate comparison of ground bounce sensitivity among the parts. (The same test can be performed on V_{OHV} by setting up the V_{OHV} test and sweeping the static input from 3.0V to 1.5V in 100mV increments.)

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10. "Test Fixtures for High-Speed Logic" (AN203), *FAST Data Manual*, Sunnyvale, CA: Signetics Corp., 1989.
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Interfacing 3V and 5V applications AN240

Authors: Tinus van de Wouw (Nijmegen) / Todd Andersen (Albuquerque)

1.0 THE NEED FOR INTERFACING BETWEEN 3V AND 5V SYSTEMS

Many reasons exist to introduce 3V[2] systems, notably the lower power consumption for mobile applications and the introduction of parts that use technologies with such fine geometries that 5V is simply not allowed any more.

The introduction of the 3V standard as supply voltage has resulted in many design activities for digital systems. Very often, however, there is a gradual transition from 5V to 3V, since not always are all required components available, or the system is rather complex so that 3V is introduced in part of a system. As an example, customers wish to use an existing and proven CPU, while a new, more complex ASIC with added features can only be made with 3V. Or vice versa!

With the introduction of new standards such as 2.2-2.7V or even 1.7V we expect that interfacing between systems that use different supply voltages will be an actual issue for many years to come. This application note specifically addresses the interfacing between 3V and 5V systems, but the results can be applied for interfacing between other voltage levels as well.

We will discuss how one can ensure reliable information exchange and how to prevent current flow between both supply voltages when interfacing logic with memories, ASICs, PLDs and microprocessors at different supply voltages.

2.0 LEVEL SHIFTING - INPUT AND OUTPUT LEVELS

We obviously want a reliable signal transfer from the 5V system to the 3V system and vice versa. This implies that the output voltages should be such that the input levels are exceeded.

2.1 TTL and CMOS Switching Levels

As a reminder, digital circuits have input levels defined: one voltage (V_{IL}) below which the circuit certainly sees it as a logical "0" and another voltage (V_{IH}) above which the input is guaranteed "1".

Digital circuits normally come in two versions:

- TTL levels: V_{IL} = 0.8V, V_{IH} = 2.0V
- CMOS levels: $V_{IL} = 0.3 * V_{CC}$, $V_{IH} = 0.7 * V_{CC}$.
  For systems with V_{CC} = 5.0 ± 0.5V this practically means:
  V_{IL} = 1.35V, V_{IH} = 3.85V.

2.2 Level Shifting from 5V to 3V

All 5V families have an output voltage swing that is large enough to drive 3V reliably. As described in Section 4.0, outputs may be as high as 3.5V for many "TTL" output stages, to the full 5V for many CMOS outputs. Therefore, as far as switching levels are concerned, there are no problems in interfacing from 5V to a 3V system.

2.3 Level Shifting from 3V to 5V

All 3V logic families deliver practically the full output voltage swing of 3V, so they can drive TTL switching levels without problems (see Fig. 1).

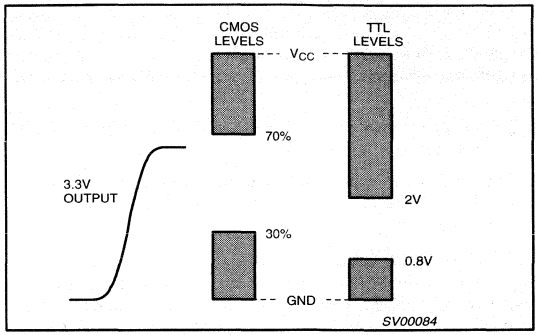

Figure 1. Switching Levels

One issue remains: a 3V system driving a 5V one that has CMOS input levels. This cannot be reliably done by standard 3V logic families, even when using pull-up resistors, simply because under worst case conditions, the output voltage is not high enough to guarantee that the signal will be seen as a logical "1". Philips Semiconductors developed special dual V_{CC} levelshifters to address that situation (see Section 6.0).

3.0 INPUT STRUCTURES OF DIGITAL CIRCUITS

Before discussing further issues on 3-5V interfacing we should start by investigating the inputs of digital circuits in order to understand what care one should take to prevent problems.

3.1 ESD Input Protection Circuits

Virtually all inputs of a digital circuit contain an ESD protection circuit that prevents damage against electrostatic discharge. This circuit is present between the physical input pin and the active circuit. Two popular schemes are given in Fig. 2.

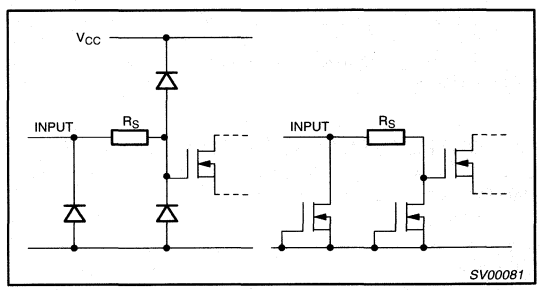

Figure 2. ESD Protection Circuits

The classic CMOS scheme as shown left provides protection against negative zaps by the diodes to ground. Positive zaps are clamped by the diode to V_{CC}. The real disadvantage is that the maximum input voltage of such a circuit is limited to V_{CC} + 0.5V. For a V_{CC} of 3V the allowed input voltage is too low for direct interfacing to most 5V systems.

2. We use the expression "3V" when a supply voltage is used between 2.7 and 3.6V.

Modern low voltage circuits use a double transistor circuit as shown right that was pioneered in our ABT families. Two transistors (Bipolar or MOS) act as fast Zener diodes protecting against positive zaps. Now, there is no diode to V_{CC} and the maximum input voltage is not limited by V_{CC}.

Typically, such circuits have a breakdown voltage between 7 and 10V, easily allowing input voltages from any 5V system.

LV is the only family that employs a classic protection circuit, all other Philips Semiconductors low voltage logic families have the dual transistor protection circuit.

3.2 Bus Hold Circuits

ALVC, LVC16 and LVT families use bus hold circuits as shown in Fig. 3. A bus hold circuit holds the input at the most recent value when the input is left floating by using a small MOS transistor as pull-up or pull-down device.

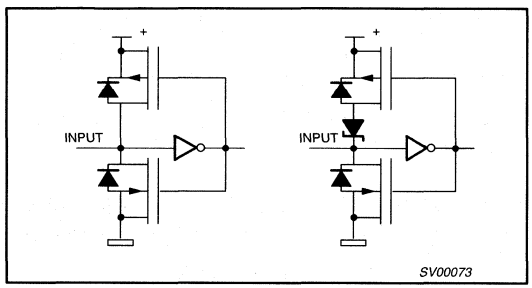

Figure 3. Bus hold circuits

A bus hold circuit for CMOS as shown left has also a diode between the input and V_{CC} which is formed by the intrinsic diode between the source and drain of the upper PMOS. This means that for ALVC and LVC16 the input voltage is limited to V_{CC} + 0.5V.

A different bus hold circuit is used in LVT parts as shown right due to the versatility of the QUBiC process which allows the use of a series Schottky diode so that there is no current path to V_{CC} in the bus hold circuit used for LVT.

4.0 OUTPUT STAGES OF DIGITAL CIRCUITS

Output structures of digital circuits (see Figs. 4 and 8) determine the output voltage swing. Circuits may swing between GND and V_{CC} or the swing may be limited by voltages developed internally.

Also, output structures determine the behavior when the output pin is taken above V_{CC}, which may be the case when two outputs are tied together on a common bus.

4.1 Bipolar Output Stage

A typical bipolar output structure does not have the full output voltage swing. When a 5V output is active HIGH, the output voltage is limited to $V_{CC} - 2 * V_{BE}$ (= approx. 3.6V). Therefore, quite often, interfacing with 3V systems works without currents flowing from the 5V supply into the 3V supply, or the current is so low that there is no real problem.

4.2 CMOS output stage

The output for a typical CMOS part swings fully between GND and V_{CC}.

One important point to note is that there is an intrinsic diode between the source and the drain of the upper PMOS as shown in Fig. 4. This may cause a current to flow from the output to V_{CC} when the voltage on the output pin is lifted higher than one diode voltage above V_{CC}.

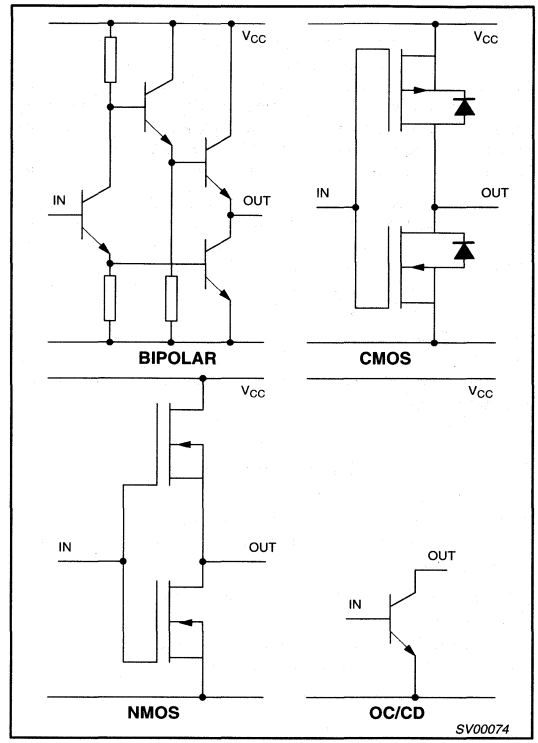

Figure 4. Typical digital output structures

4.3 Other MOS Output Structures

Some other MOS output stages such as many SRAM and DRAM circuits may have a circuit that shows a behavior similar to a bipolar output stage. An example is given Fig. 4: the upper NMOS limits the output voltage to $V_{CC} - V_{TH}$ (= approx. 3.5V). Such a circuit often works fine when driving 3V systems.

4.4 Open Collector/Open Drain

Some parts have an "Open Collector" or "Open Drain" output stage and there is no internal circuit to pull the output high. Normally a pull-up resistor connects the output to a voltage that can be higher than V_{CC}. Obviously such parts allow easy interfacing, but for speed reasons the pull-up resistor often needs to be relatively small, so the use of pull-up resistors increases power losses.

4.5 The BiCMOS Output

A BiCMOS output combines the advantages of bipolar (i.e. high output drive, low noise) and CMOS (full output voltage swing, low standby current). The output stage of Philips Semiconductors BiCMOS parts has some specific features that will be discussed in Section 6.1.

5.0 CURRENT FLOW FROM +5V TO +3V OR TO GROUND

A particular issue to address is the flow of current from the 5V power supply to the 3V supply. Then, the 3V supply may be charged up to a higher voltage which is potentially hazardous, affecting all connected 3V ICs. In addition the current provides extra power losses and may damage parts, although normally the driver capability is such that no damage occurs.

One other issue to study is the behavior of parts when either the 5V or 3V supply line is made 0V (suspend or power-down mode). In such a case high currents may flow from V_{CC} to ground.

5.1 Current Flow from the 5V Supply into a 3V Input

In mixed mode systems there is always data transmission from 5V to 3V. In such a case a 5V output drives a 3V input circuit. A potentially damaging current can only flow when two conditions are met: first, the 5V driver should be able to deliver current when the output voltage exceeds approximately 3.5V; second, the input circuit of the 3V part driven should have a current path from its input pin to V_{CC}. One has to carefully consider both aspects and check especially for a current path from the inputs of 3V parts to V_{CC}. Even with 5V parts that have limited output voltage swings, considerable currents may flow under worst case conditions.

5.2 Transceivers

The 3V part driven is often a transceiver, so the 'input' is effectively an input paralleled by an output. This means that the behavior of an output when its voltage exceeds V_{CC} is also important. More specifically, a CMOS transceiver has its output's intrinsic diode tied to V_{CC} that still provides a current path even when the part is in 3-State.

A similar situation may occur in the case of bus contention, when both outputs try to drive the bus HIGH. Fig. 5 shows the current paths via the active part and via the intrinsic diode of a CMOS output stage.

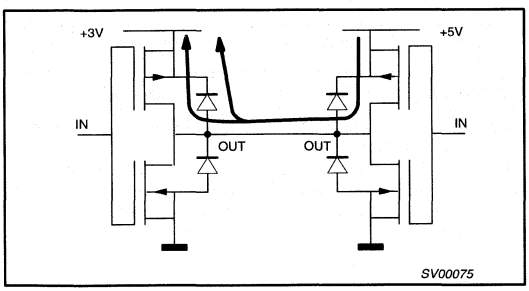

Figure 5. Currents from +5 to +3V

5.3 Suspend Mode or Power-down Mode

For energy savings parts of systems may be powered down, i.e., the supply voltage is made zero (called suspend mode or power-down mode) and the same observations can be made as above. In general, when a part allows 5V on its output under normal operating conditions, it also can withstand 5V on its output when V_{CC} is made zero. This is not always the case, however, especially for some competitive dual V_{CC} level shifters (see Section 6.1).

5.4 Summarizing Current Flow

When looking at unwanted currents from the 5V supply to the 3V supply, or in the case of suspend or power-down mode, we should study the following:

- The output capability of the driver (with V_{CC} = 5V)
- The input circuit of the driven part

When the driven part is a transceiver, we also have to look at:

- The behavior when the part is in 3-State: is there a diode to V_{CC}?
- Its output characteristics when the part is active HIGH in the case of bus contention.

6.0 PHILIPS SEMICONDUCTORS LOW VOLTAGE LOGIC FAMILIES

Philips Semiconductors has a wide range of logic families optimized for operation at 3V. Below we only discuss the properties for level shifting between 3 and 5V systems; other data can be found in the databook or brochures. In addition SPICE simulation models are available (see Section 7.0).

6.1 Main Interfacing Properties per Family

LV, which is derived from HCMOS, has a classical ESD protection circuit with a diode to V_{CC}; therefore its input interfacing capabilities are limited. The input voltage should not exceed V_{CC} + 0.5V (see Fig. 2 and Fig. 6) or the input current should be limited. As a result, one may use 5V outputs with a low drive capability as input for LV, or TTL outputs with a limited output voltage such as DRAM outputs described in Section 4.0. Obviously this is strongly dependent on the circuit layout of the driving 5V device.

LV has a standard CMOS output with a diode between the output and V_{CC}, so its output voltage is limited to V_{CC} + 0.5V.

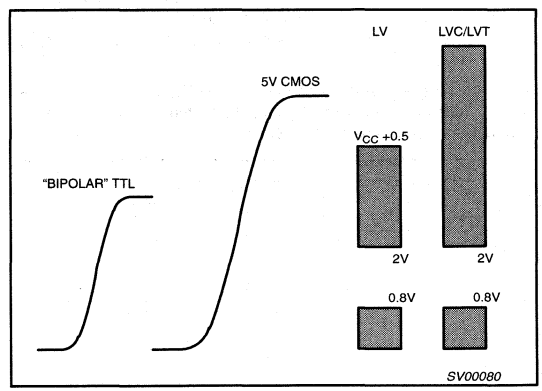

Figure 6. 5V Driving 3V

LVC has an input circuit without a diode to V_{CC}. Unidirectional devices, i.e., all parts that are not transceivers, can perfectly interface between 3V and 5V without any difficulty (see Fig. 6). Transceiver circuits, as described in Section 4.0, have a diode to V_{CC} in the output stage and have therefore limitations similar to LV.

The output voltage of LVC is limited to V_{CC} + 0.5V since it has a standard CMOS output with a diode between the output and V_{CC}.

Currently being introduced[3] is an enhancement to the LVC parts that have 3-State capability: 5V I/O tolerant (see Fig. 7). It works by dynamically tying the back gate to the highest possible voltage, either V_{CC} or V_{OUT}, such that the diode is never forward biased. This patented feature allows 5V on its output when the part is in 3-State. When the part is active HIGH, obviously there is still a current path from the output to V_{CC} via the active PMOS.

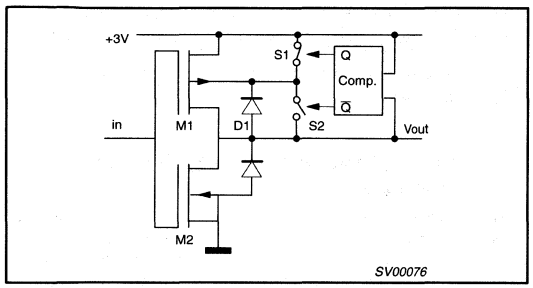

Figure 7. New LVC Output Structure

LVC16 parts have a bus hold circuit as described below under ALVC, limiting the 5V input tolerance to control pins only.

HLL behaves identical to LVC. Due to its high speed and high drive, the output is not 5V tolerant.

ALVC has an ESD protection circuit similar to LVC, but also employs bus hold circuits on its data inputs (i.e. not on its control inputs) as described in Section 3.2. Therefore, both unidirectional and bidirectional devices have the same limitations as LV. Its control inputs, such as OE and DIR, may be driven from both 3V and 5V. For speed reasons we do not plan a 5V tolerant version.

LVT uses QUBiC with its versatility in internal component options. LVT's bus hold has a built-in Schottky diode that prevents any currents from the input to V_{CC}, as is the case for the bus hold used in ALVC.

In its output stage (see a simplified circuit in Fig. 8) the output diode to V_{CC} is eliminated using a Schottky diode, making LVT fully 5V compatible when the part is in 3-State.

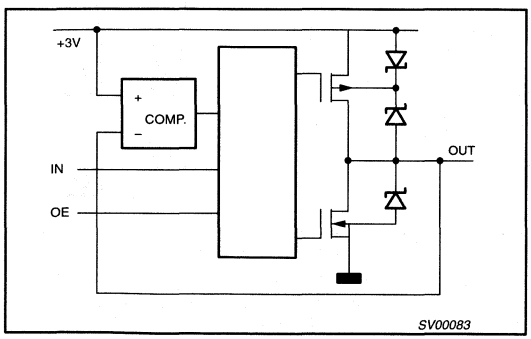

Figure 8. LVT's Output Circuit

Moreover, a special circuit has been incorporated that switches off the current path to V_{CC} when the output is pulled more than approximately 0.5V above V_{CC}. A comparator simply switches off the output stage, disregarding the state of the inputs and the control pins. This feature, called 'overvoltage protection', makes LVT fully 5V compatible and makes LVT the ideal choice for all sorts of mixed mode systems. There are no basic limitations in using LVT in mixed mode systems.

When the output voltage of LVT is lifted above V_{CC}, a current will flow, shown in Fig. 9. As one can see, where competitive devices have a current that can be considerable, a current of approximately 30mA is sufficient to toggle the overvoltage protection. The value of 30mA appears to be a good optimum to prevent noise signals from triggering the protection circuit. This implies that a simple pull-up resistor is not sufficient to pull the output into protection mode.

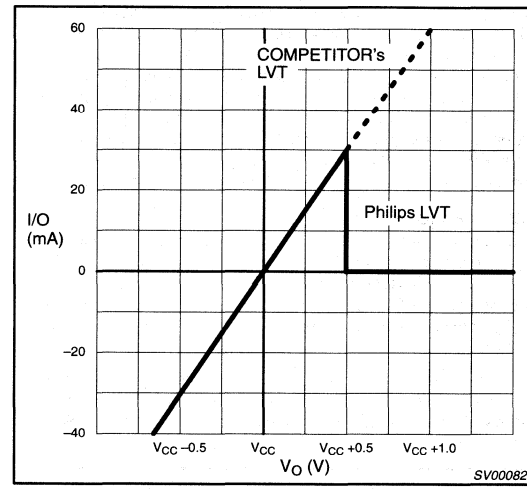

Figure 9. LVT I/O Current

It should be noted that this figure is valid when the output is active HIGH. When the output is in 3-State, no currents will flow.

Dual V_{CC} level shifters (74LVC4245 and 74ALVC164245, 8 and 16 bits resp.) are CMOS transceivers fed from both 3V and 5V supplies. The level shifting is done internally and the parts have full output voltage swings at both sides (see Fig. 10), making them ideal for level shifting purposes, especially when driving 5V CMOS levels.

3. First part available early 1996.

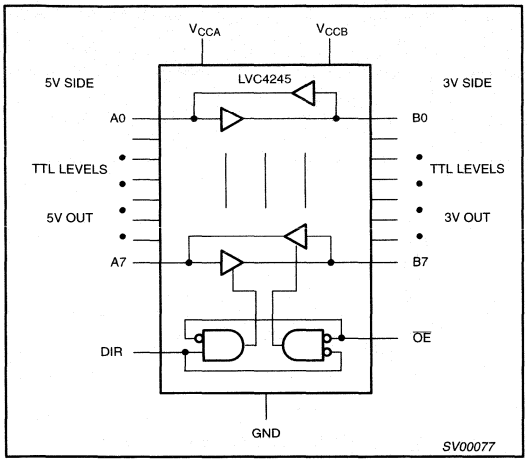

Figure 10. 74LVC4245

Dual V_{CC} level shifters are superior alternatives to the sometimes used input pull-up resistors, blocking diodes and other circuits that normally degrade speed and/or noise margins.

6.2 Summarizing Low Voltage Logic Interfacing Capabilities

Table 18 below sums up the input and output capabilities of our logic families and their behavior at suspend/power-down mode.

Table 18.

FEATURE		LV	LVC	LVC16 ALVC	LVT LVT16	DUAL V_{CC} LEVEL SHIFTERS
Drive 5V TTL levels		✓	✓	✓	✓	✓
Drive 5V CMOS levels		–	–	–	–	✓
5V on Input		–	✓	–	✓	✓[2]
5V on Control pins		–	✓	✓	✓	✓
5V on Output	when in 3-State	–	–/✓[1]	–	✓	✓[2]
	when active HIGH	–	–	–	✓	✓[2]
Suspend/power down mode		–	–/✓[1]	–	✓	–

NOTES:
1. Feature to be introduced early 1996 for 3-State LVC parts.
2. Valid for side working from the +5V supply side when V_{CC} = 5V

6.3 Unidirectional Dataflow from 5V to 3V

Fig. 11 gives the situation for unidirectional data flow from 5V to 3V. Any 5V TTL part can basically drive the 5V tolerant inputs of LVC, HLL and LVT. The other families need a dual V_{CC} level shifter to prevent current flow from the 5V supply into the inputs of the 3V logic.

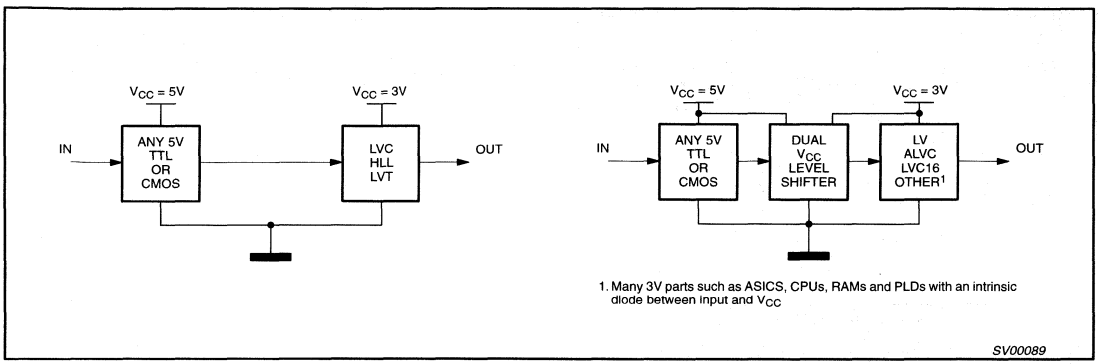

Figure 11. 5V Drivers to 3V Receivers

6.4 Unidirectional Dataflow from 3V to 5V

Fig. 12 Shows that driving 5V TTL can be done from any 3V logic family. When driving 5V CMOS levels, a dual V_{CC} level shifter is required to increase the output voltage swing.

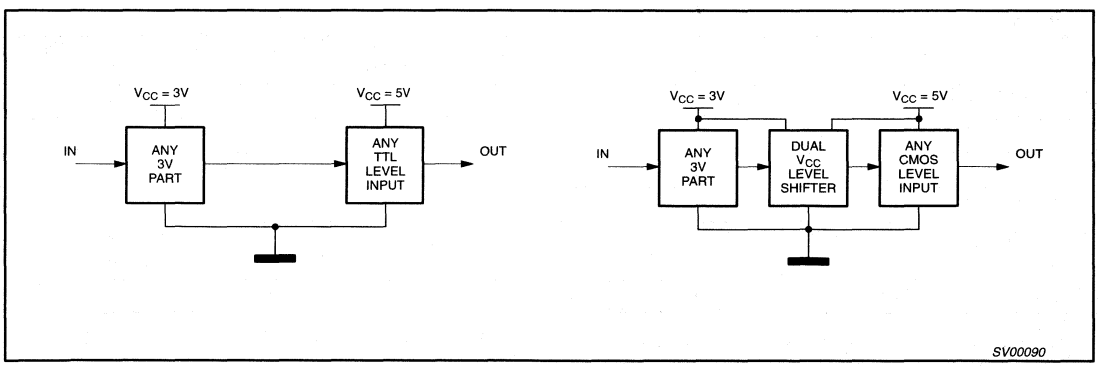

Figure 12. 3V Drivers to 5V Receivers

6.5 Bidirectional Data Communication Between 5V and 3V Systems

In many cases the data communication is bidirectional, both from 3V to 5V and from 5V to 3V. Parts that operate in both directions may be transceivers, but also other parts with a combined input/output (I/O), as shown in Fig. 13.

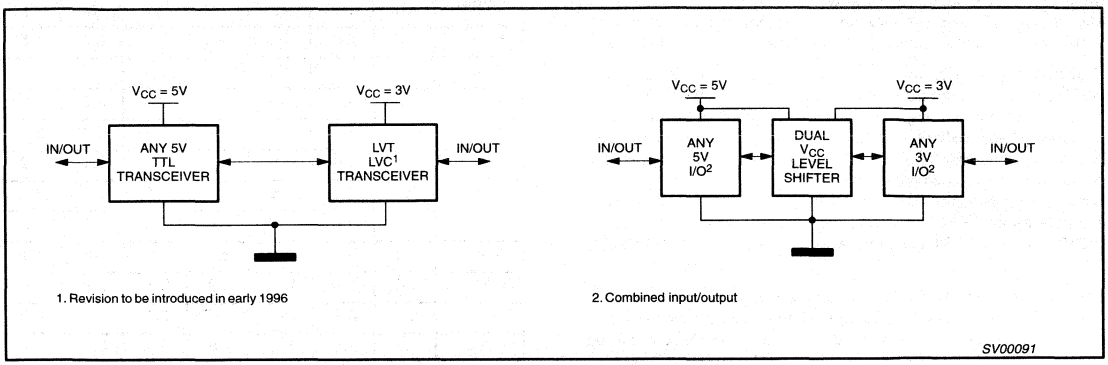

Figure 13. 5V Transceivers on Common Bus with 3V Transceivers

When either LVT or LVC with 5V tolerant outputs is used, a direct communication can be established between these and any 5V TTL level transceiver. When other low voltage families or parts with I/O are used, the dual V_{CC} levelshifters provide the transceiver function with built-in level shifting and preventing current flows between power supplies.

7.0 REFERENCES AND FURTHER READING

AUTHOR AND TITLE	ORDER NO.	ORDER NO. USA
Brian Martin, *Tips for straddling the 3V to 5V Fence* (EDN, Apr 4, 1994)	—	98 2902 010
Tinus van de Wouw, Rob Croes and Yong-in Shin, *Considerations for interfacing with Philips 3V HLL/LV with 5V ICs in mixed mode systems*, 1993	9398 706 29011	98 2902 003
Philips Semiconductors, Data Handbook IC24, *Low Voltage CMOS and BiCMOS families*, 1995	9398 652 71011	98 2902 002 02
Philips Semiconductors, *SPICE I/O models for 5V and 3.3V Standard Logic Families*, 1995	9397 750 00119	9397 750 00119

8.0 CONCLUSION

This report gives many details on how to properly communicate between 3V and 5V systems. Special characteristics of Philips Semiconductors low voltage logic families often allow easy and worry-free translation of data from one system to the other.

Transmission lines and terminations with Philips Logic families

AN246

Author: Mike Magdaluyo, Logic Products Group

INTRODUCTION

With increasing systems speeds and faster logic families, interconnect characteristics have become significant. The signal transition times of faster families can increase transmission line effects on printed circuit board traces and cables. If not taken into consideration, signal degradation can cause data errors in a system.

Previous logic families with slower rise and fall times such as LS and HCMOS were not as severely affected by this issue if line lengths were not too long. For example, an HCMOS buffer with a 5 ns edge will start exhibiting transmission line effects when a circuit board trace is longer than a foot. However, with newer families, even relatively short trace lengths become very important. This application note will briefly review transmission line concepts and evaluate transmission line effects with Philips 5 volt and 3 volt BiCMOS and CMOS logic families such as ABT, AC(T), ALVC, LVC, LVT, and ALVT.

For more detailed information on transmission lines, there are many other resources to refer to. The terms line or transmission line will refer to a cable or printed circuit trace medium and will be regarded as equivalent for electrical purposes, though their construction varies in real applications.

CRITICAL LINE LENGTH

An interconnect is considered electrically long when the round trip propagation delay of the interconnect from the driver to the load is equal to or greater than the transition time of the driver's rise or fall time. At this point, transmission line effects become significant. Using 160ps per inch as a nominal propagation delay for 50 Ω stripline medium and a nominal 0.9 ns rise time for a lightly loaded ABT driver with 15 pF loading, the critical line length is

Eq. 1

$$\text{Critical line length} = 2 \times \frac{t_{pd}}{t_r}$$

$$= 2 \times \frac{160 \text{ ps / in.}}{0.9 \text{ ns}}$$

$$= 2.8 \text{ in.}$$

For this example, traces shorter than this can be treated as lumped elements. Traces equal to or longer than this length should be modeled as distributed elements. Table 1 shows critical line lengths at various line impedances for different Philips' logic families. Assumptions are light loading of 15 pF and a nominal 8 nH per inch characteristic inductance for a PC board trace. Formulas to determine line impedance are shown in the following section.

Table 1. Maximum trace length in inches with 15pF loading

Family	tr ns	tf ns	100 Ω	70 Ω	50 Ω	35 Ω	25 Ω
HC	2.9	2.9	18.1	12.7	9.1	6.3	4.5
AHC	2.1	1.6	10.0	7.0	5.0	3.5	2.5
AC	1.2	1.7	7.5	5.3	3.8	2.6	1.9
ALS	2.7	1.7	10.6	7.4	5.3	3.7	2.7
FAST	4.0	1.4	8.8	6.1	4.4	3.1	2.2
ABT	0.9	1.2	5.6	3.9	2.8	2.0	1.4
LVT	0.8	0.6	3.8	2.6	1.9	1.3	0.9
ALVT	0.8	0.7	4.4	3.1	2.2	1.5	1.1
LVC	1.8	1.8	11.3	7.9	5.6	3.9	2.8
LV	2.9	2.9	18.1	12.7	9.1	6.3	4.5
ALVC	1.2	1.1	6.9	4.8	3.4	2.4	1.7

As you can see, using faster edge families even with relatively short traces still requires consideration of transmission line effects.

CHARACTERISTIC LINE IMPEDANCE AND CAPACITIVE LOADING

A transmission line has distributed series inductance and distributed capacitance throughout its length, and can be modeled as shown in Figure 1. The line has characteristic inductance and capacitance per unit length, l, where L_O is in Henries per inch, and C_O is in farads per inch.

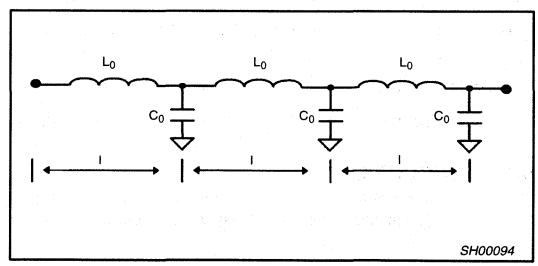

Figure 1. Circuit equivalent for a transmission line

Transmission lines and terminations with Philips Logic families

Typical characteristic impedances on PC boards can be from 50 Ω to 100 Ω. The impedance can be determined by

Eq. 2

$$Z_O = \sqrt{\frac{L_O}{C_O}}$$

where L_0 and C_0 are the characteristic inductance and capacitance per unit length of the trace.

The line propagation delay can be determined by

Eq. 3

$$T_O = \sqrt{L_O C_O}$$

Distributed capacitive loads lower the effective impedance of a transmission line and increase the line propagation delay. Consider a bus structure with equally spaced loads of the same value as in Figure 2. The capacitors represent the input capacitance of each receiver.

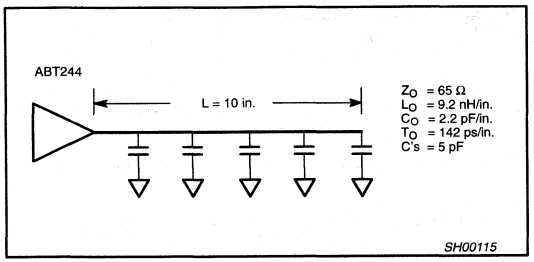

Figure 2. Equally spaced capacitive loads

If the driver's rise or fall time is longer than the electrical length of the spacing between the loads, the effects of individual capacitors distribute evenly across the waveform edge. This adds capacitance to the line's characteristic capacitance. The board interconnect at the receiver pin has capacitance also: via, connector, etc., and the values are added to the receiver's capacitance to form a lumped value. Suppose the interconnect capacitance is 5 pF, then the lumped distributed capacitance is 10 pF per every 2 inches or 5 pF per inch. The new line impedance, Z_O', can be calculated and will be

Eq. 4

$$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_{LU}}{C_O}}}$$

$$= \frac{65\ \Omega}{\sqrt{1 + \frac{5\ \text{pF/ in.}}{2.2\ \text{pF/ in.}}}}$$

$$= 36\ \Omega$$

where C_{LU} = load capacitance per unit length, pF/in.

Likewise, the new line propagation delay will be

Eq. 5

$$T_O' = T_O \times \sqrt{1 + \frac{C_{LU}}{C_O}}$$

$$= 142\ \text{ps/in.} \times \sqrt{1 + \frac{5\ \text{pF/ in.}}{2.2\ \text{pF/ in.}}}$$

$$= 257\ \text{ps/in.}$$

Since the effective line impedance can be reduced with more loading, a driver with sufficient source and sink capability should be chosen to drive that particular impedance. This is discussed in the next section.

INCIDENT WAVE SWITCHING AND DRIVER I-V CHARACTERISTICS

When launching a pulse down the line, the driver needs sufficient current to change the voltage on the line. For TTL level input receivers, the guaranteed V_{IH} and V_{IL} levels are 2.0 V and 0.8 V. This means that the leading edge incident wave launched down the line should meet those levels to switch all receivers on the line and switch them only once. The drive current required is

Eq. 6

$$I_{AV} \text{ at } V_{OH} = \frac{V_{IH}\ \text{min} - V_{OL}\ \text{typ}}{Z_O'}$$

Eq. 7

$$I_{AV} \text{ at } V_{OL} = \frac{V_{OH}\ \text{typ} - V_{IL}\ \text{max}}{Z_O'}$$

As an example of incident wave switching capability, refer back to the bus structure in Figure 2. The effective line impedance is 34 Ω. Using Equations 6 and 7, the drive current required to switch the line is determined as follows:

$$I_{AV} \text{ at } V_{OH} = \frac{V_{IH}\ \text{min} - V_{OL}\ \text{typ}}{Z_O'}$$

$$= \frac{2\ \text{V} - 0.2\ \text{V}}{36\ \Omega}$$

$$= 50\ \text{mA}$$

and

$$I_{AV} \text{ at } V_{OL} = \frac{V_{OH}\ \text{typ} - V_{IL}\ \text{max}}{Z_O'}$$

$$= \frac{3.4\ \text{V} - 0.8\ \text{V}}{36\ \Omega}$$

$$= 72\ \text{mA}$$

ABT products are rated for +32 mA source current at 2 V and –64 mA sink current at 0.55 V. By referring to I-V curves you can determine if the dynamic drive current is enough to switch the line on the incident wave. From the following curves in Figures 3 and 4, note that the –76 mA at 2 V and +167 mA at 0.8 V satisfies the requirements in the above formulas. To compare the drive strength of other product families, Figures 5 through 9 show IOL and IOH currents for a typical '244 driver for the ABT16, ALVC, ALVT, LVC, LVT, and LVT16 families.

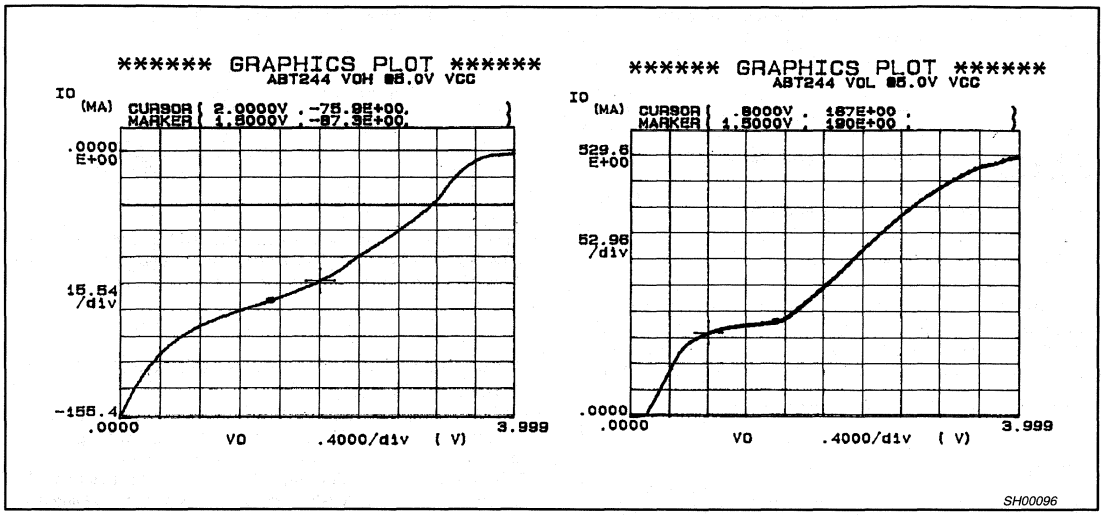

Figure 3. ABT244 I-V curves

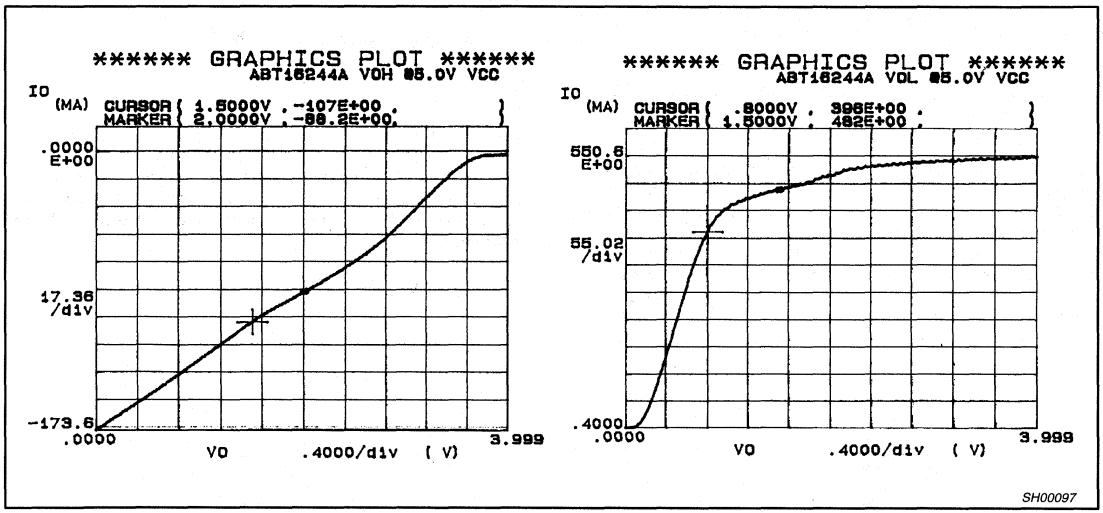

Figure 4. ABT16244 I-V curves

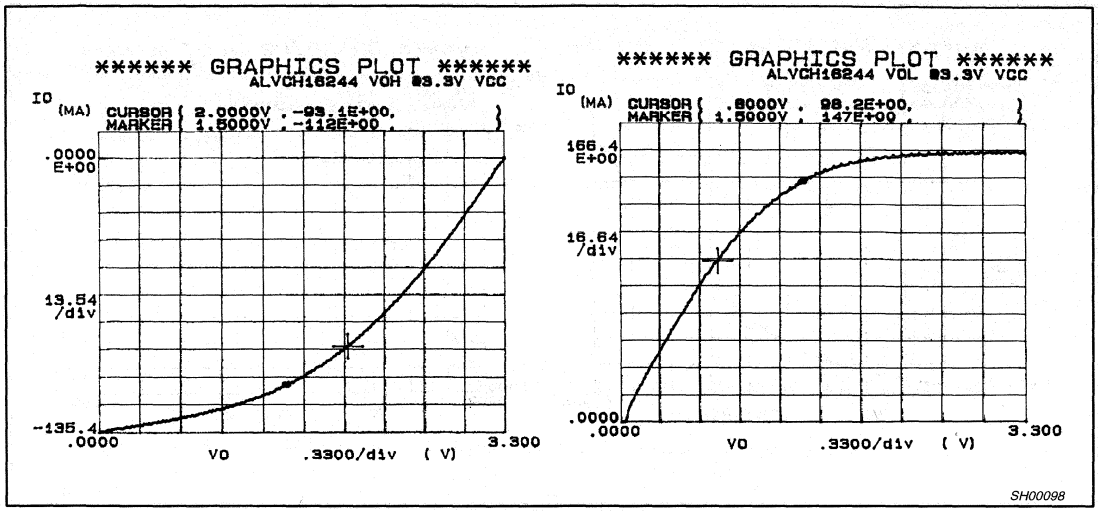

Figure 5. ALVC16244 I-V curves

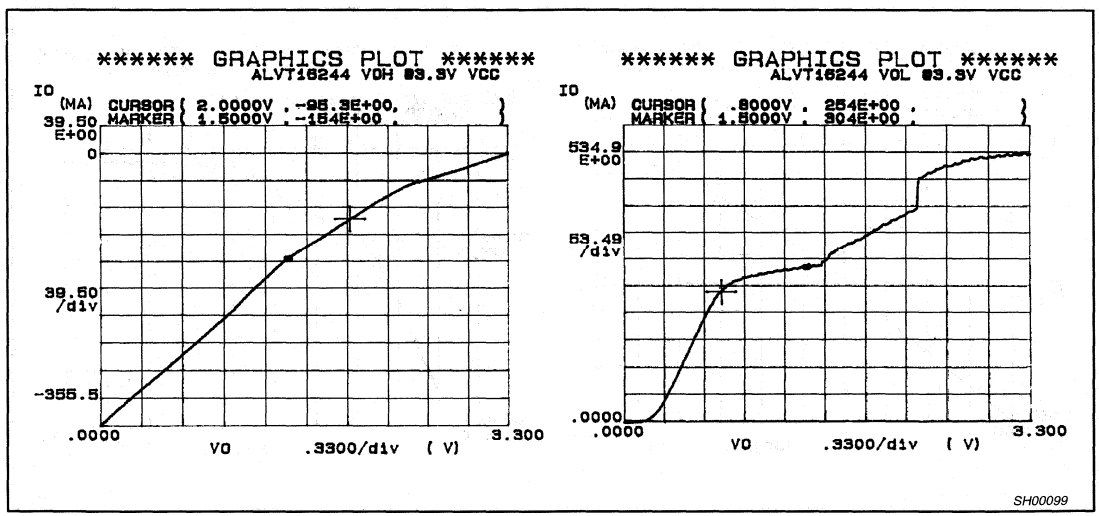

Figure 6. ALVT16244 I-V curves

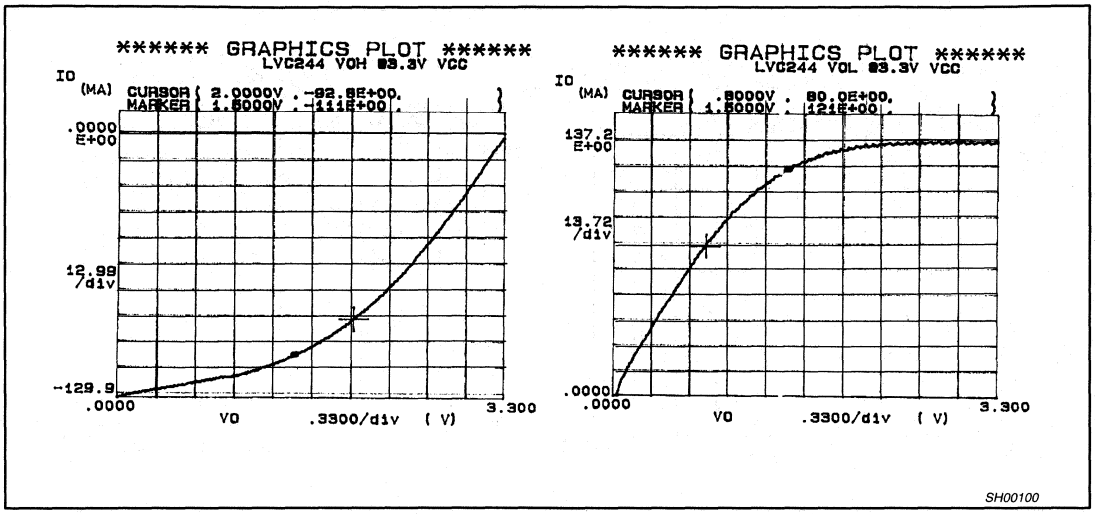

Figure 7. LVC244 I-V curves

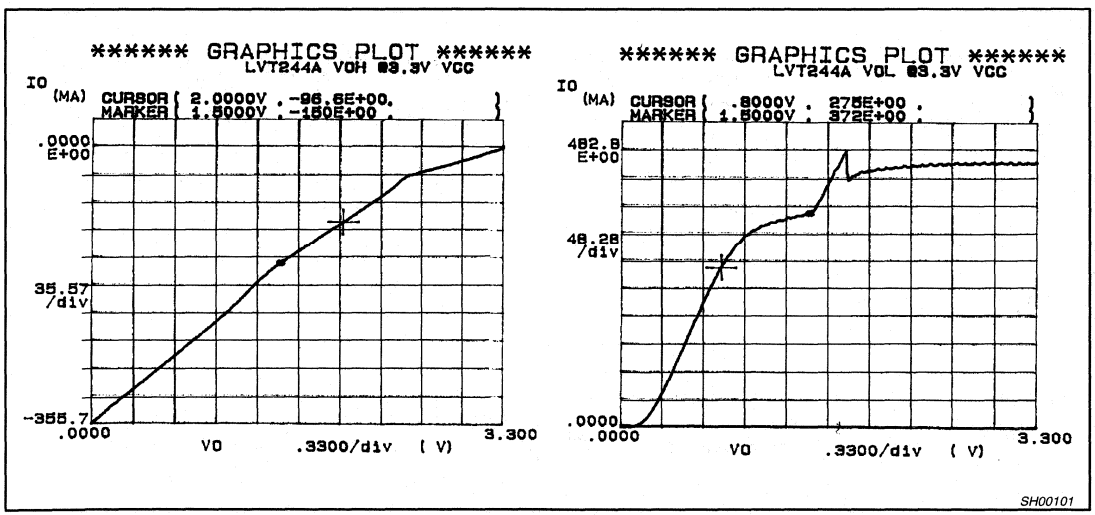

Figure 8. LVT244 I-V curves

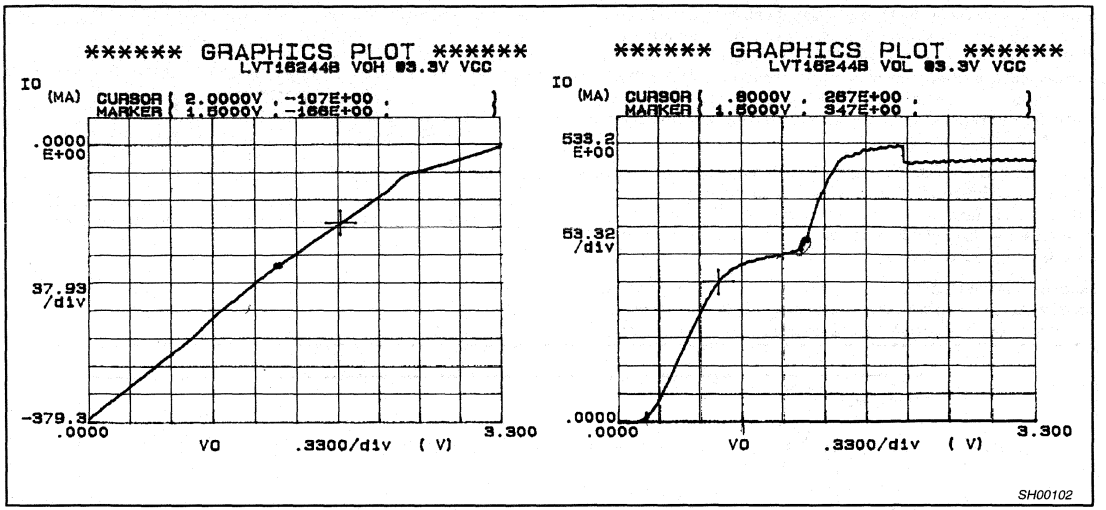

Figure 9. LVT16244 I-V curves

Based on the I-V curves, all families have good drive current in the logic high state, and ABT(16), ALVT, and LVT(16) BiCMOS families have considerably stronger drive than the other families in the logic low state. The BiCMOS families have been optimized to drive backplanes. The other CMOS families are suitable for local buses and driving point-to-point loads. The following table shows recommended minimum line impedances that can be driven by the buffer/drivers of various Philips logic families:

Table 2. Minimum line impedance for logic families

Logic Family	Minimum Z_O
ABT(16)	35 Ω
AC/ACT	50 Ω
ALS(–1)	65 Ω
FAST	50 Ω
LVT(16)	35 Ω
ALVT	35 Ω
LVC(16)	50 Ω
ALVC	50 Ω

REFLECTIONS FROM IMPEDANCE MISMATCHES

Since a driver has non-zero output impedance, its impedance along with the line impedance form a voltage divider. The incident wave launched down the line is a portion of the driver's voltage. When the wave encounters an impedance change from either the line or a receiver input, a portion of the wave is reflected back towards the driver ($V_{reflected}$) which is determined by the reflection coefficient r. The reflected portion is also added to the incident wave which continues propagating down the line ($V_{transmitted}$). The relationship of these voltages are shown in the following equations:

Eq. 8

$$\rho = \frac{(Z_{load} - Z_O)}{(Z_{load} + Z_O)}$$

Eq. 9

$$V_{reflected} = V_{incident} \times \rho$$

Eq. 10

$$V_{transmitted} = V_{incident} + V_{reflected}$$

Since driver and line impedances are usually mismatched, a reflection occurs at the driver and travels back towards the load. The reflection coefficient at the driver is determined by Equation 11:

Eq. 11

$$\rho = \frac{(Z_{driver} - Z_O)}{(Z_{driver} + Z_O)}$$

This volley of wave reflections continues, with reflections getting smaller as the signal waveform settles.

During the reflection period, the waveform may have a stairstep response—in the case of a driver's impedance higher than the line's—or it may have a "ringy" response—in the case of a driver's impedance lower than the line's. To predict the signal integrity of a waveform you can use reflection charts or Bergeron plots, but they can be cumbersome.

Transmission lines and terminations with Philips Logic families

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Another tool that is useful for evaluating these effects is SPICE models. Philips Semiconductors offers free models for our FAST, ALS, HCMOS, ABT, ABT16, ALVC, ALVT, LV, LVC, LVT, and LVT16 product families to aid in signal integrity evaluation. The models help reduce design time by eliminating time consuming efforts of reflection and Bergeron diagrams, and they also help predict signal integrity prior to board layout.

As an example, the circuit in Figure 10 was modeled and the results are shown in Figure 11. A pulse was fed into the ALVC16244 and the input and output waveforms were observed. This example illustrates the effect of reflections due to the mismatch of the driver impedance (around 10 Ω) and the transmission line.

Note that the overshoot and undershoot in Figure 11 may not be acceptable to drive other 3V device inputs or DRAM's. To reduce the overshoot and undershoot, line termination will be necessary.

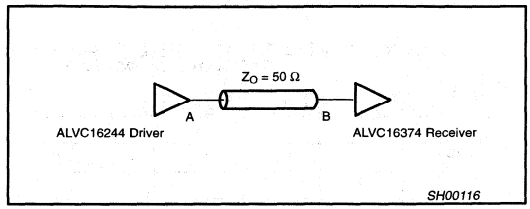

Figure 10. ALVC16244 driving ALVC16374 receiver

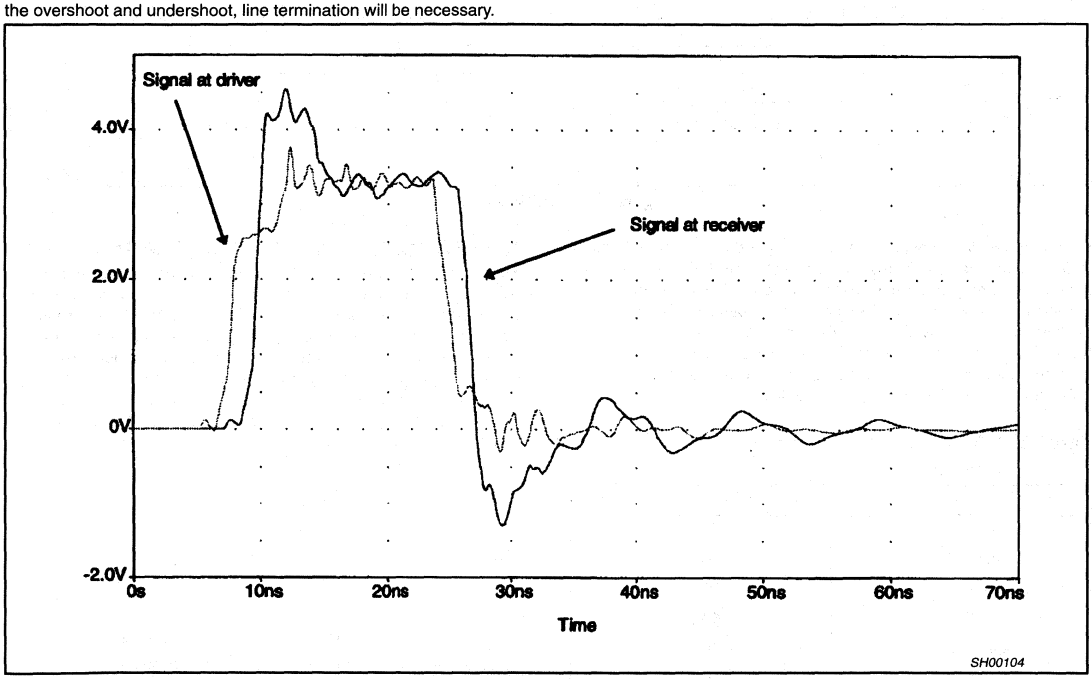

Figure 11. SPICE simulation for the circuit in Figure 10.

TERMINATION CONSIDERATIONS AND TECHNIQUES

As shown earlier, impedance mismatches between the source, line and load can cause reflections. These reflection can cause signal delays, such as the case of a stairstep type of response which requires additional line delays to reach sufficient switching threshold levels, mis-clocking from non-monotonic edges, or excess voltage/current on inputs. A signal should be terminated if it won't settle on time, if it produces overshoot or undershoot that violates the receivers input voltage or current ratings, or if it drives edge-sensitive asynchronous inputs and has non-monotonic edges. Several termination schemes can be used depending on drive current capability, power dissipation requirements, and incident wave switching requirements.

There are two basic approaches to line termination: source termination and end termination. Both schemes will result in a stable signal at the far end of the line after one line delay. Source termination, however, results in a stable signal up to two line delays for loads at intermediate points on the line and at the source. More details of each scheme follows.

Source Terminations Methods

Figure 12 shows the configuration of a source terminated daisy chain line.

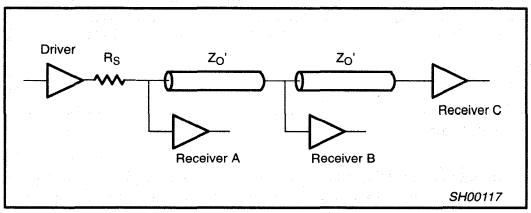

Figure 12. Source termination configuration

The concept of this termination method is to try and match the loaded line impedance with the sum of the driver output and series resistor impedances. The series resistor value is equal to Z_O' minus the driver impedance. The resistor should be located as close to the driver as possible.

Since the sum of the driver impedance and series resistor equals the line impedance, a half-height wave travels down the line from the voltage divider effect. Assuming a reflection coefficient approaching +1 at the end of the line, the reflection adds to the half-height wave, and the voltage at the last receiver is at near full amplitude. The wave amplitude at the first and intermediate receivers, however, are half-height and require up to one additional line delay for the reflected wave to reach the series terminator and add to the initial wave. Figure 13 shows a SPICE simulation of the reflections for this circuit and termination method.

Note that the last receiver is first to switch to the full signal amplitude, while the first receiver is the last to reach full amplitude. This means that any edge-sensitive asynchronous signals should be located at the end of the line. Non-monotonic edges at the beginning and intermediate points along the line could cause false clocking of devices. Also, drivers at the beginning and at intermediate points need to be able to tolerate roughly twice the settling time.

As you can see, this termination method is not very good for lines with daisy chain topologies. Source terminators work well, though, for single receiver, point-to-point loads and star type of topologies. They work well to dampen overshoot and undershoot.

Source terminators dissipate no quiescent power. The AC power dissipation can be estimated by:

Eq. 12

$$P \approx f_{2T}\left(\frac{\Delta V}{2R}\right)^2$$

where f = pulse frequency
where T = one-way line delay
ΔV = V_{OH}–V_{OL}
R = termination resistance

This approximation works if the pulse interval is greater than twice the line delay. For shorter pulse intervals, you can assume a worst case of DV/2 across the termination resistor at all times. With its low power dissipation, series termination is recommended for low voltage logic.

As mentioned previously, the sum of source impedance and the series terminator should match the loaded line impedance. Since output impedances are different in the logic low and high states, there needs to be a compromise when choosing the termination resistance. It's probably better to slightly overdrive the line by choosing a smaller resistor to ensure fast enough edge transitions to a valid logic level. Typical values in applications range from 22 Ω to 33 Ω. Philips offers ABT, ALVC, ALVT, LVC, and LVT parts with built-in series terminators that have equivalent output impedances of 30 Ω. These parts save board space by eliminating the need for a terminating resistor. Part types are designated by a "2" prefix before the part type number, e.g., 74ABT2245.

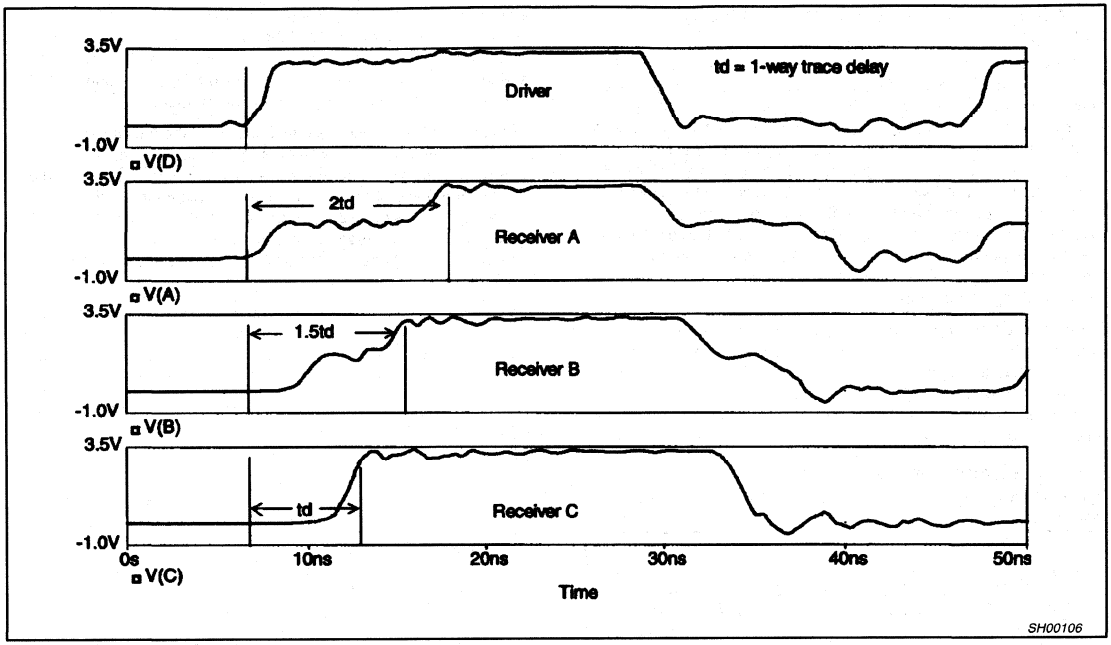

Figure 13. Reflections from source termination

Other Series Termination Schemes

Figure 14 shows a series termination used with a star stub topology.

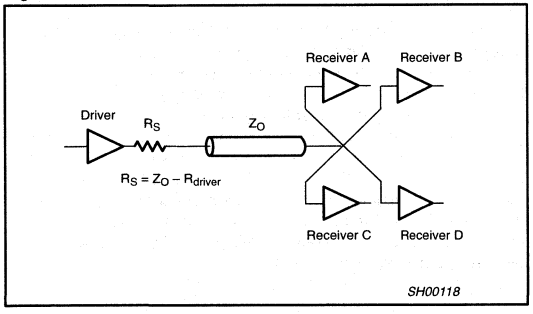

Figure 14. Series termination with star stub routing

Stub electrical lengths should be very short, about 10% of the signal edge, to prevent reflections. This method is useful for terminating clocks and other asynchronous signals if stubs are of equal length/delay. Terminating methods for some alternative star routing is shown in Figure 15.

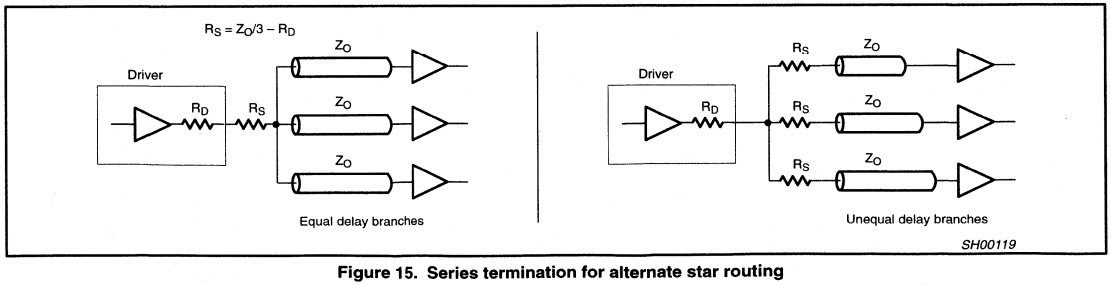

Figure 15. Series termination for alternate star routing

Figure 16 shows another method of series termination.

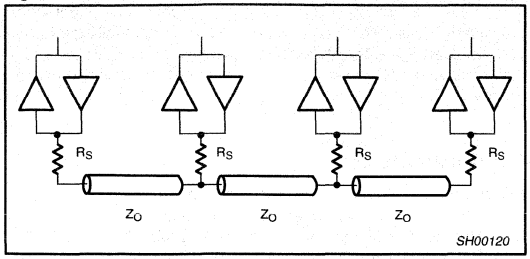

Figure 16. Series stub termination

Note that the drivers at the end will be driving RS + Z_O. Drivers in the middle should be strong enough to drive RS + Z_O/2. Again, keep stub lengths short.

End Terminations

End terminated line are recommended for distributed loads, and several methods can be used such as parallel, AC, and diode clamp methods. Figure 17 shows two parallel termination schemes.

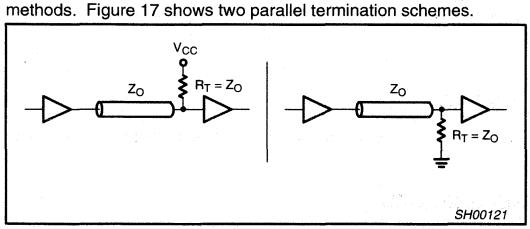

Figure 17. Parallel terminations

With this method, the termination resistance is matched to the effective line impedance. The advantage is that this method allows for incident wave switching. The disadvantages are that you need an extremely strong driver and it consumes high static power.

To reduce the drive requirements and power dissipation for this configuration, a more practical parallel Thevenin termination is shown in Figure 18 can be used.

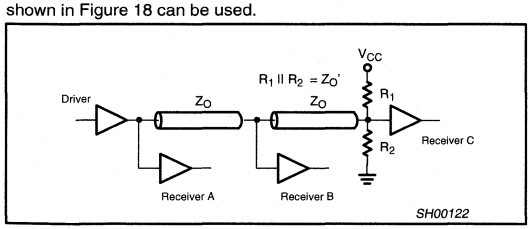

Figure 18. Daisy chain topology with split resistor Thevenin termination

This method is suitable for ABT, LVT, and ALVT families but not recommended for low voltage CMOS logic if power dissipation is a concern. The termination is placed at the end of the line as close to the receiver as possible.

If this termination technique is used on LVC and ALVC drivers, take precaution not to connect the pull-up resistor to a 5 volt supply in a mixed 3 volt/5 volt system. This can cause 5 volt supply current to flow to the 3 volt supply through the upper PMOS transistor's parasitic diode of the driver output during the active high state.

If used on a 3-State bus, avoid biasing the receiver input at its threshold switching voltage which is about 1.5 V for BiCMOS and CMOS TTL level inputs. Inputs left floating around the threshold region can consume excessive current or cause oscillations. You can use the following formula to determine values for R1 and R2 if they are not equal:

Eq. 13

$$R_1 = Z_O \frac{V_{CC}}{V_T} \text{ and } R_2 = Z_O \frac{V_{CC}}{V_{CC} - V_T}$$

where V_T = termination voltage.

A good termination voltage to choose is 2.5 V for TTL thresholds.

Assuming a 50% duty cycle, the average power dissipation of the resistors will be:

Eq. 14

$$P = 0.5 \times \left(\frac{V_{OH}^2 + V_{OL}^2}{2R_2} + \frac{(V_{CC} - V_{OH})^2 + (V_{CC} - V_{OL})^2}{2R_1} \right)$$

Another method to reduce quiescent power dissipation is AC termination shown in Figure 19. This method is recommended for distributed loads or when static power consumption is a concern.

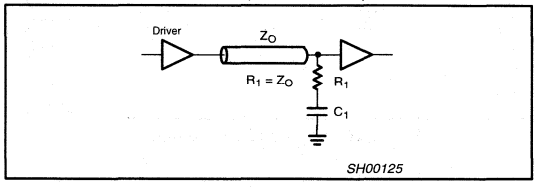

Figure 19. AC termination

No DC current flows during quiescent high or low logic levels, but an AC current path is available through C1 to terminate the line. Choose XC to be a small percentage of Z_O at the operating frequency of:

Eq. 15

$$f = \frac{1}{2T_r}$$

where T_r is the faster of the rise or fall time

Also, for DC balanced signals with 50% duty cycle, choose C such that $Z_O C$ is much greater than the pulse period. For DC imbalanced signals, choose C such that $Z_O C$ is much greater than the rise time but much smaller than half the pulse period.

Provided that the duty cycle is 50%, the average voltage across C1 is midway between the driver high and low output levels. R1 will also have half the voltage swing always across it. The power dissipation across R1 will be:

Eq. 16

$$P = \frac{\left(V_{OH} - \frac{V_{OL}}{2}\right)^2}{Z_O}$$

$$= \frac{(V_{OH} - V_{OL})^2}{4Z_O}$$

Another method of end termination is shown in Figure 20.

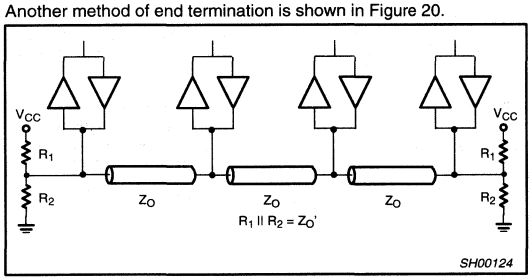

Figure 20. Party bus dual termination

The same principles should be applied to this method as in the Thevenin termination. Note that drivers will need to be strong, such as the BiCMOS devices, since they will have to drive half the value of Z_O.

The last method of end termination discussed in this paper is diode clamp termination shown in Figure 21:

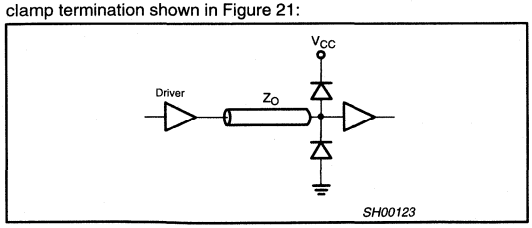

Figure 21. Diode clamp termination

The advantages are that it dissipates no power and it adds no delay to the net. The method is good to clamp overshoot and undershoot provided that it is fast enough to react to the rising or falling edge. The disadvantage is that it won't limit overshoot on 5 volt TTL drivers such as ABT. Also, it can't guarantee monotonicity on weak drivers.

CONCLUSION

Philips Semiconductors offers various advanced CMOS and BiCMOS families for high speed bus applications. This paper discussed aspects of transmission line effects with these families. Critical line length, line impedance, loading, and drive capability of different product families was examined. Impedance mismatches and reflections were discussed along with various termination solutions. Considerations of these various factors will help solve signal integrity issues in a design, and these factors need to be considered with their tradeoffs to satisfy the system design needs.

To help make design efforts easier, Philips Semiconductors offers free SPICE models for our 3V and 5V product families to aid in signal integrity evaluation. The models help reduce design time by eliminating time consuming efforts of reflection and Bergeron diagrams, and they also help predict signal integrity prior to board layout.

ACKNOWLEDGEMENTS

Thanks to Tinus van de Wouw and Jeff West for their help and data.

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The behaviour of integrated bus hold circuits AN2022

Author: Tinus van de Wouw, Philips Semiconductors, Nimegen

INTRODUCTION

The problem with floating or unused CMOS inputs as a general rule is that they must not be left floating otherwise due to gradual charging of the gate input capacitance, they may cause the following:

- There may be a static current flowing through the input stage, causing unnecessary excessive power dissipation.
- When the input voltage reaches the threshold level, the device may start high frequency oscillations causing heat generation that may eventually damage the part.

Therefore, as a standard solution, all unused (open or floating) inputs are simply connected to GND or V_{CC} to prevent these adverse effects.

In certain testing conditions, inputs may be left open, but certainly in bus applications, it may happen that inputs are effectively floating when all devices driving the bus are in 3-state. One should ensure that all inputs are defined "0" or "1" to prevent excessive heat dissipation or unwanted high frequency oscillations.

THE SOLUTIONS

The following are several solutions including their added costs, components counts, and effectiveness:

Static Pull-up/Pull-down Resistors

Static pull-up/pull-down resistors are a solution used very often to define the state of unused CMOS inputs when the bus is not driven by any device. Although these resistors cause additional power dissipation and increase component count, they are very effective. However, when using today's narrow pitch packages such as TSSOP48-56, there may not even be enough space to add these pull-up/pull-down resistors on the PCB.

External Bus Hold Circuit

An external bus hold circuit (see Figure 1) is another solution which uses an inverter and resistor between its input and output. This circuit connects the input to GND or V_{CC} depending on the state of the input and holds the bus in this state, hence its name "bus hold". Although this circuit reduces excessive power dissipation caused by static pull-up/pull-down resistors described earlier, it significantly adds to the component count and costs.

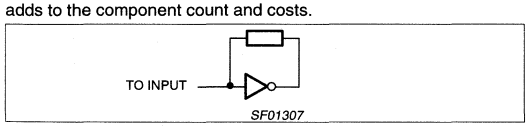


Figure 1. External Bus Hold Circuit

Integrated Bus Hold Circuit

Philips Semiconductors has applied integrated bus hold circuits (see Figure 2) for a number of logic families. Integrated bus hold circuits minimize additional power dissipation and provide additional component count internally at no extra cost for the device.

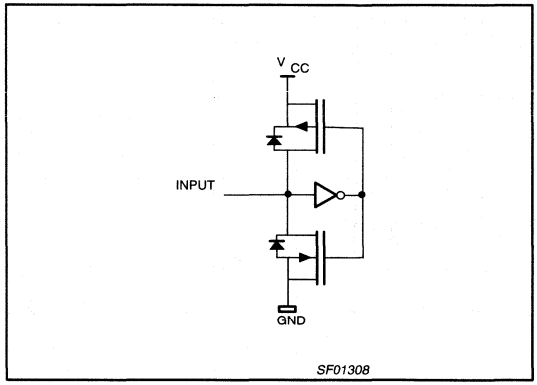


Figure 2. Integrated Bus Hold Circuit

The integrated Bus Hold circuit acts like dynamic pull-up/pull-down resistors as follows:

- When the input is at "0", the output of the inverter is at "1" so that the lower FET is ON and acts like a pull-down resistor.
- Similarly, when the input is at "1", the upper FET is activated and acts like a pull-up resistor.

When the input voltage varies, an input current will flow into or out of the input circuit (see Figure 3), so that when the input voltage rises, the input current will slowly increase, since the lower FET is conducting. Around the threshold level, the upper FET will then start conducting and the lower FET will stop conducting. Then the input current will reverse direction (input current flows out of the integrated bus hold circuit) slowly decreasing until the input voltage is at V_{CC}.

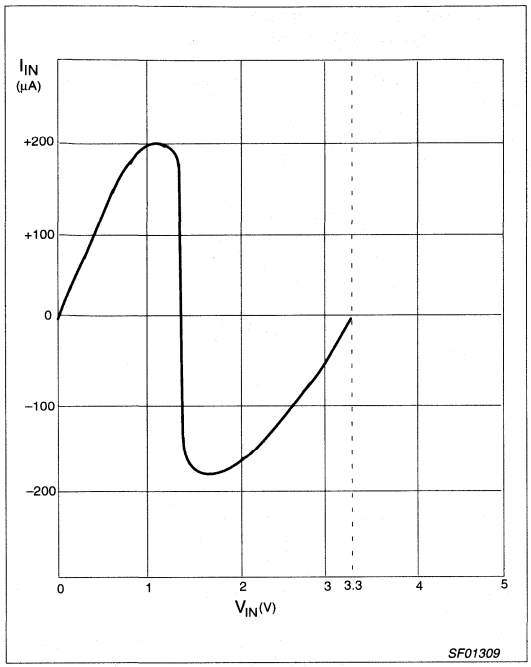


Figure 3. Input Voltage (V_{IN}) vs. Input Current (I_{IN})

Description

The following parameters describe the behaviour of the integrated bus hold circuit:

- IBHL (for LVT called I_{HOLD}) is the bus hold LOW sustaining current, that specifies an input current below which the bus hold circuit is keeping the input voltage lower than the 0.8V TTL switching level.
- Similarly, input current (IBHH), the bus hold HIGH sustaining current will yield an input voltage higher that 2.0V when the input is at "1".
- IBHLO is the bus hold LOW overdrive current. When the input is driven with this current, the input will change from a "0" to a "1".
- Similarly, IBHHO specifies the input current that will change the input from a "1" to a "0".

INTEGRATED BUS HOLD CIRCUITS FOR 5V TOLERANT DEVICES

The circuit discussed in Figure 2 is the integrated bus hold circuit in its basic form as it is used in logic devices such as the ALVC.

However, logic transceiver functions that have 5V tolerant outputs also require the integrated bus hold circuits to be 5V tolerant. For such cases, the bus hold circuits have been provided with additional components to enable bus hold circuits to handle 5V operation.

Philips Semiconductors has provided two such solutions, the bus hold with Schottky diode and with dynamic backgate switching (see Figure 4) as follows:

Bus Hold with Schottky Diode

The standard solution for LVT devices uses a series Schottky diode (see Figure 4), which effectively blocks the current path from the input to V_{CC}.

Bus Hold with Dynamic Backgate Switching

The standard solution for LVCHXXXA devices is called dynamic backgate switching (see Figure 4), where the MOSFET is switched OFF when the input voltage exceeds V_{CC} and the current path through the diode is blocked by some switches.

Both bus hold circuits behave quite differently as shown in the V_{IN}/I_{IN} characteristics (see Figure 5) as follows:

- The input current for LVT (with Schottky diode) becomes zero when the input exceeds ($V_{CC} - V_{Fdiode}$).
- Whereas for LVCHXXXA devices with dynamic backgate switching have a hysteresis effect. When the input voltage exceeds (V_{CC} + 0.6V), the input FET is turned off, so the input current becomes zero. The upper FET is turned on again when the voltage becomes lower than (V_{CC} – 0.6V).

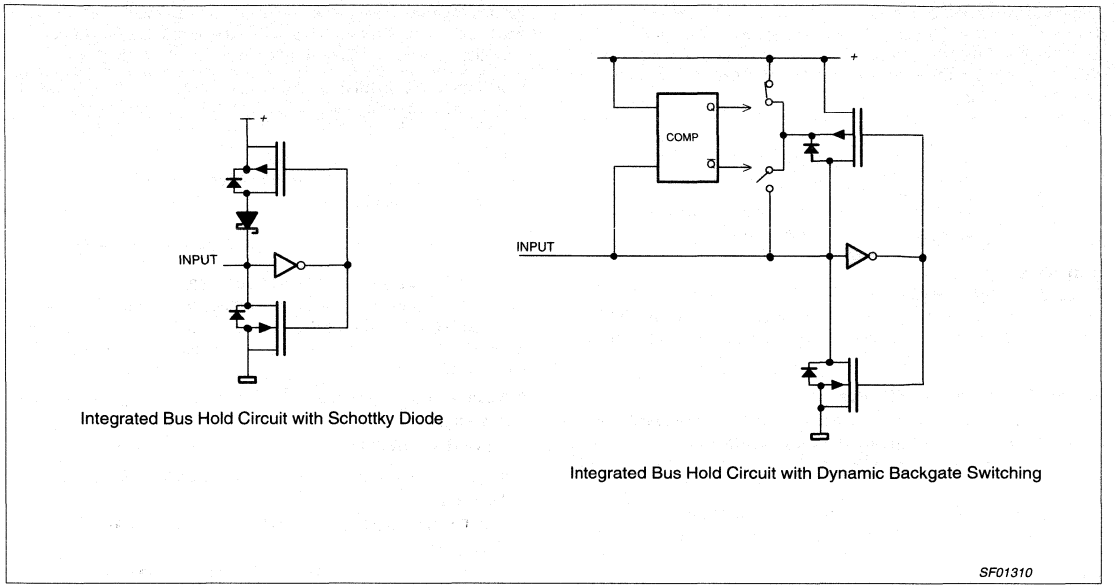


Figure 4. Integrated Bus Hold Circuits with Schottky Diode and Dynamic Backgate Switching

DRIVING A BUS HOLD CIRCUIT

The input current is so low that virtually any part is capable of delivering enough current to toggle quite a number of paralleled inputs. At Philips Semiconductors we have performed tests with one (1) 74LV244 device (with 8mA output drive) driving from 0 to 10 74LVC244As (without integrated bus hold circuits) and compared them with 0 to 10 74LVCH244As (with integrated bus hold circuits). These tests showed that the effects of integrated bus hold circuits on the total propagation delay are negligible.

As a rule of thumb, adding one (1) integrated bus hold circuit gives an extra propagation delay of about 40 ps, so that one (1) LV device driving 10 integrated bus hold circuits will give an extra delay of 0.4ns. Families with a higher output drive will have a propagation delay that is proportionally shorter. For instance, one 74LVC244 (24mA driver) will have an extra propagation delay of about 15ps per integrated bus hold circuit load.

When applying parts with integrated bus hold circuits in backplane buses, where the total current flowing in the bus are so high, the desired effects of integrated bus hold circuits may be negligible. The current that an integrated bus hold circuit can handle is by far insufficient to pull an active bus high ("1") or low ("0"). Only after all reflections are at a minimum can the integrated bus hold circuit become effective. Additionally, for crosstalk situations, the bus hold may be incapable of holding the bus to the required "1" or "0" state.

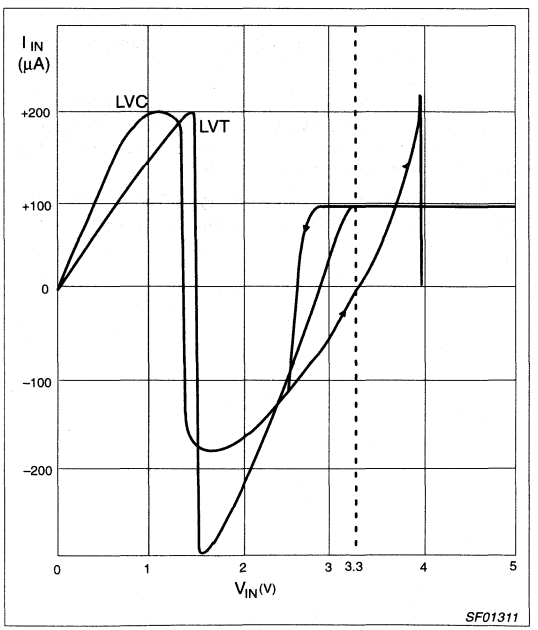


Figure 5. V_{IN} vs I_{IN} for 5V tolerant Integrated Bus Hold Circuits

The behaviour of integrated bus hold circuits AN2022

In some applications, the bus should become HIGH when all outputs driving the bus are in 3-state. In such cases, you should use a termination resistor, (R_T pulled-up to V_{CC}) which is low enough to overrule all the bus holds connected to that circuit. R_T is calculated as follows from equation 1:
EQUATION 1

$$R_T < \frac{V_{CC} - V_{TH}}{IBHHO}$$

where V_{TH} is the switching level HIGH
IBHHO is the maximum overdrive current; the typical value is about a factor of two lower

Example

With a V_{CC} of 5V, IBHHO = 500μA and TTL switching levels (i.e. V_{TH} = 2V), the termination resistor value should be less than 6kΩ. Therefore, when more inputs are connected to the bus, this value is proportionally lower.

Power Dissipation Effects

Since a bus hold effectively forms a pull-up or pull-down resistor, it will dissipate extra power when the input changes state. Additionally, the driver must deliver extra current which creates more dissipation in the driver.

Using conservative assumptions, you can calculate the following parameters from equation 2 for low voltage families when $2.7V < V_{CC} < 3.6V$:
EQUATION 2

$$P_{BH} \leq f \times T_T \times \frac{I_{HOLD} \times V_{CC}}{2}$$

where P_{BH} is the dissipation in the bus hold circuit itself
T_T is the average of the rise and fall times of the input signal
f is the frequency of the input signal

One important consequence of the above equation is that the dissipation of bus hold is dependent on the input rise and fall times which are primarily determined by the output drive capability of the driving component and the capacitive load.

The frequency, f in the equation is normally NOT equal to the clock frequency, it is an effective input frequency. For example, if the input is HIGH for a long time, the dissipation during that time is essentially zero. Therefore, you should estimate the number of transitions based on a practical occurrence of "0's" and "1's".

From equation 2, if IBHHO = 500μA and V_{CC} = 3.3V, the following worst case dissipation value in μW can be determined from equation 3 as follows:
EQUATION 3

$$P_{BH} \leq f \times T_T$$

where f is in MHz and
T_T is in ns

Typically, the power dissipation is about half the value of P_{BH}.

Family Survey and Nomenclature

Philips Semiconductors has integrated bus hold circuits in some advanced BiCMOS and CMOS families which are identified by the letter "H" in its the part number (the exceptions are LVT and LVT16 families) as follows:

- A standard bus hold circuit with current path to V_{CC} is built in the following:
  - **LVCH** and **ALVCH**
- An enhanced bus hold circuit without current path to V_{CC} is built in the following:
  - **LVT**, **LVT16**, **ABTH**, and **ABTH16** using a Schottky diode arrangement
  - The 5 Volt tolerant **LVCXXXA** devices that use dynamic backgate switching.
- Families such as **LV**, **LVC**, **HLL**, **ABT**, **ABT16**, and all **5V CMOS** have no bus hold circuits.

Conclusion

This application note discusses the effects of bus hold circuits as applied by Philips Semiconductors in their advanced CMOS and BiCMOS logic families. Logic devices with bus hold circuits can have floating (open) inputs without any negative effects. They have a low power dissipation compared with using static pull-up or pull-down resistors and most importantly because they are integrated, they do not increase component count, keep costs low, and optimize the available space on the PCB.

Section 7

Advanced Low Voltage CMOS Logic

CONTENTS

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when though-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1. Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260°C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24V) to the lead(s) of the package, below the seating plane or not more than 2mm above it. If the temperature of the soldering iron bit is less than 300°C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400°C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2. Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapor phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250°C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45°C.

Table 3. Suitability of surface mounted packages for various soldering methods

Rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at and angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, only consider wave soldering for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4mm**, e.g., SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2 and SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260°C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150°C within 6 seconds. Typical dwell time is 4 seconds at 250°C.

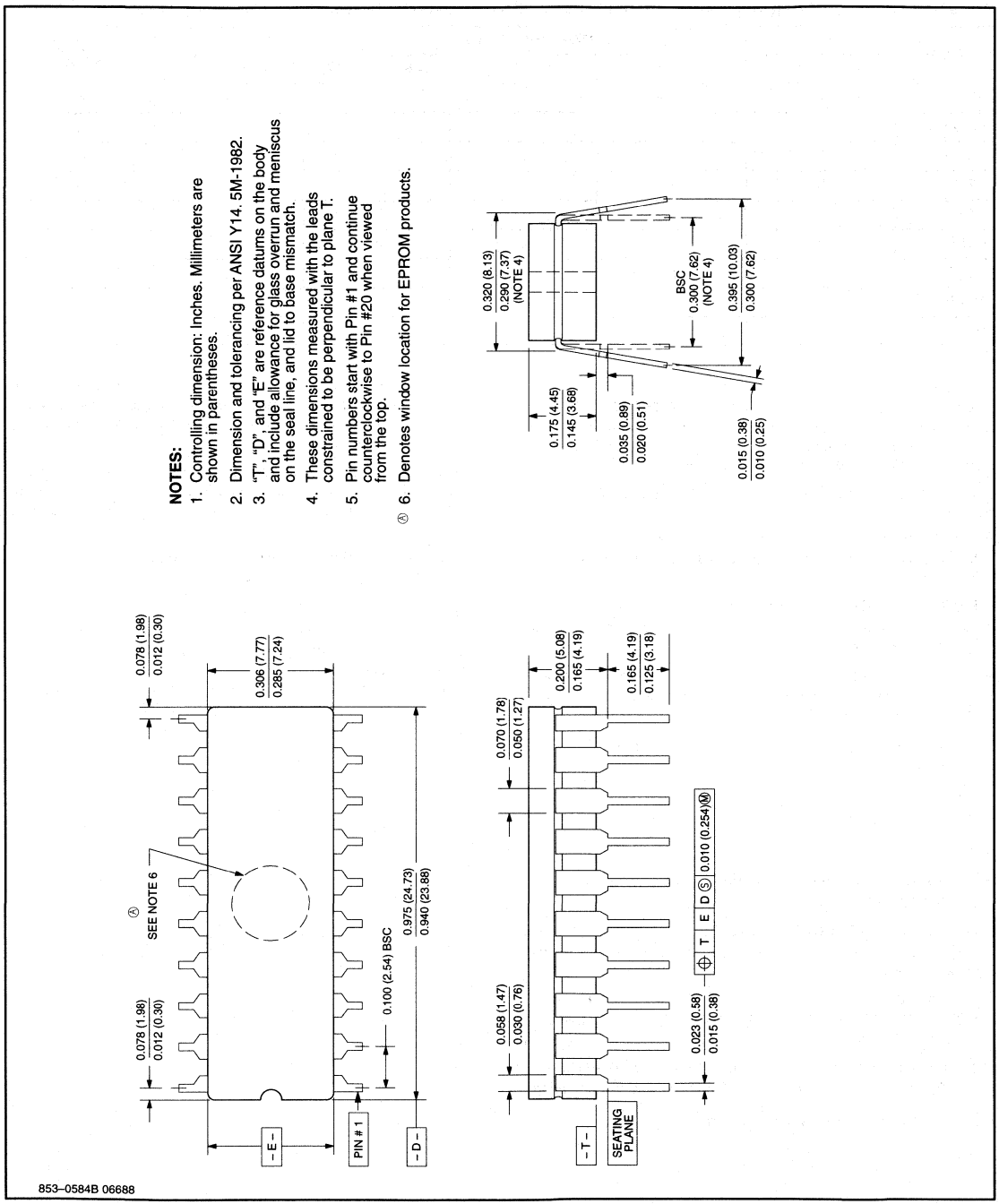
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320°C.

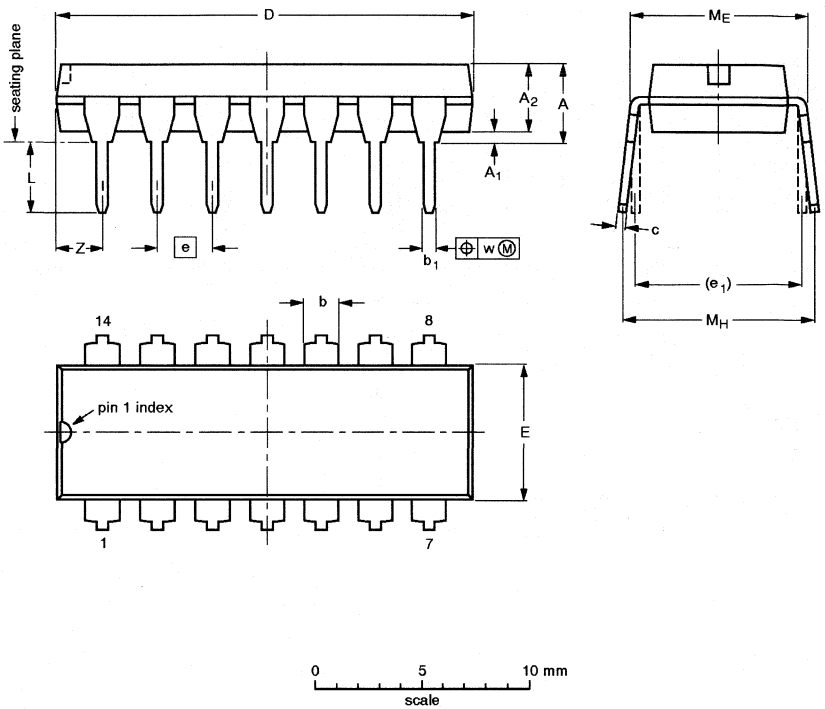
Package outlines

0584B 20-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE (WITH WINDOW (FA) PACKAGE)



Package outlines

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

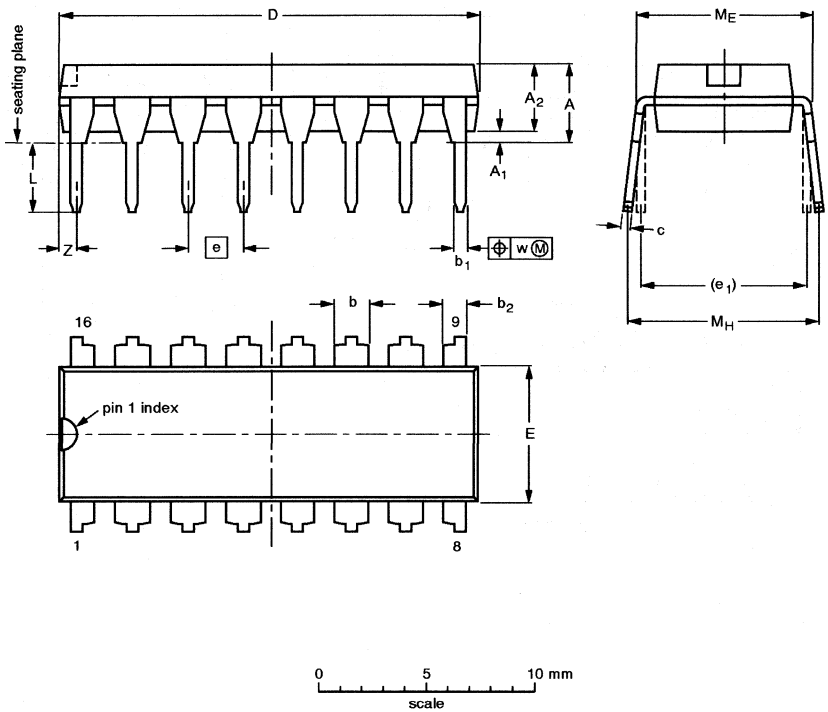
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

Package outlines

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

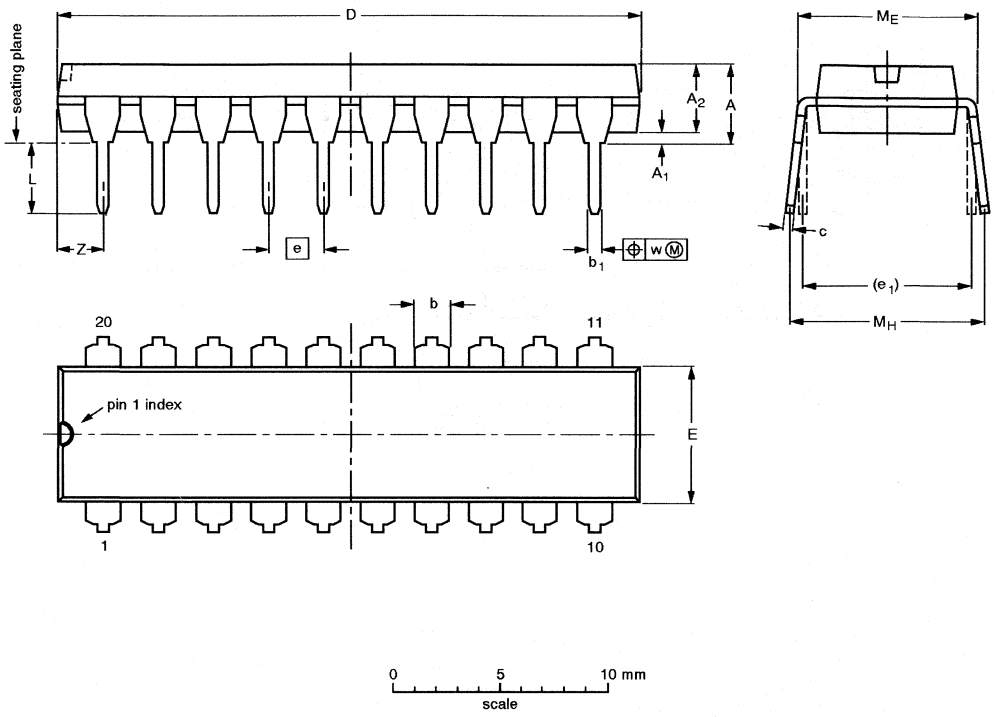
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

Package outlines

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

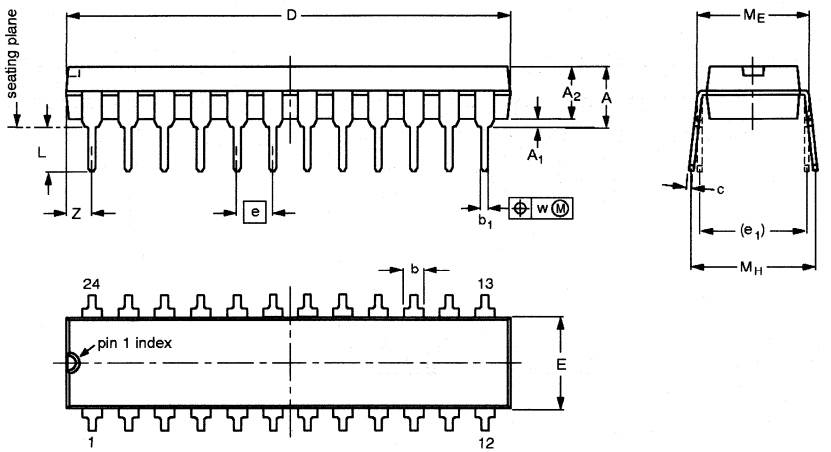
Note

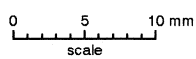
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

Package outlines

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

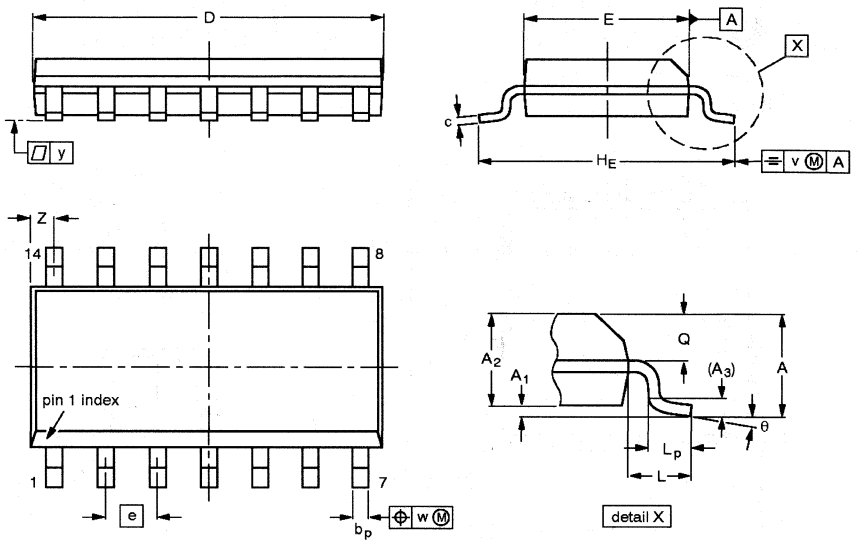
Note

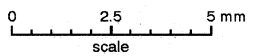
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

Package outlines

SO14: plastic small outline package; 14 leads; body width 3.9 mm — SOT108-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

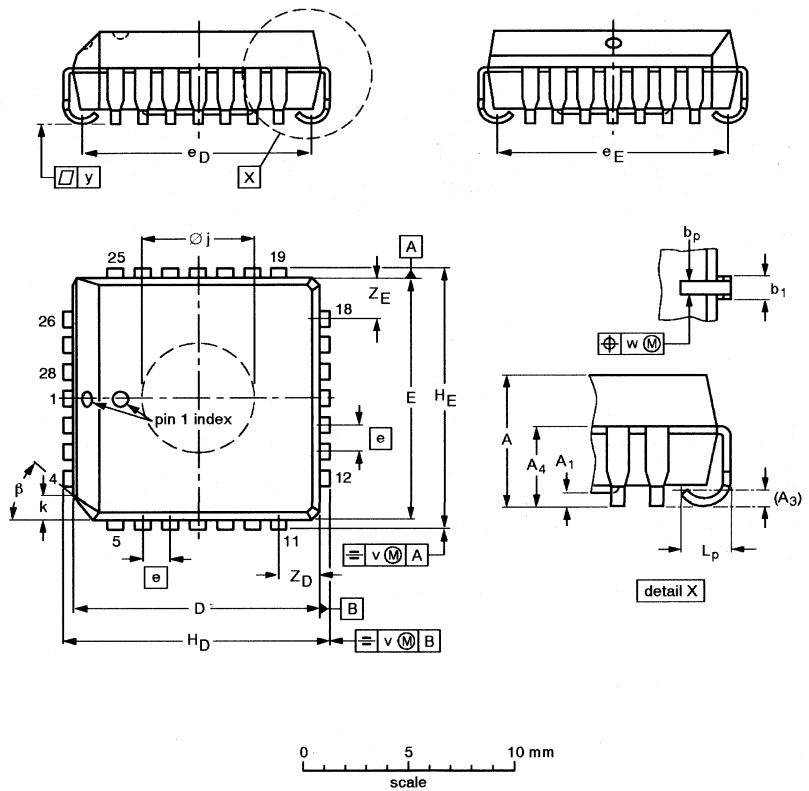
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

Package outlines

PLCC28: plastic leaded chip carrier; 28 leads; pedestal — SOT261-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

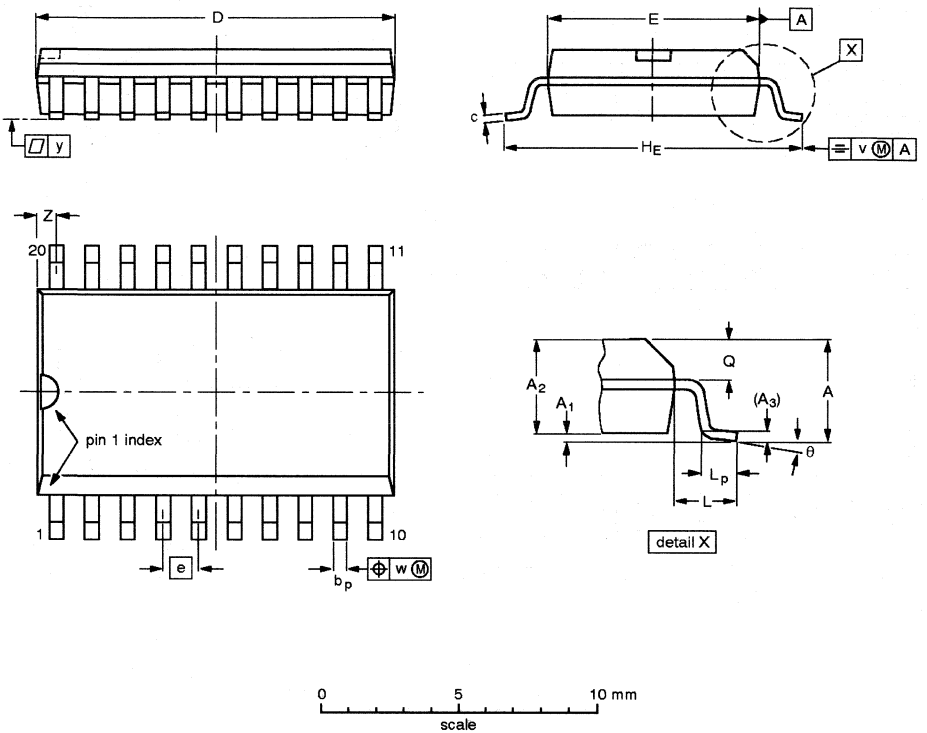
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-3		MO-047AB				~~95-02-25~~ 97-12-16

Package outlines

SO20: plastic small outline package; 20 leads; body width 7.5 mm — SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

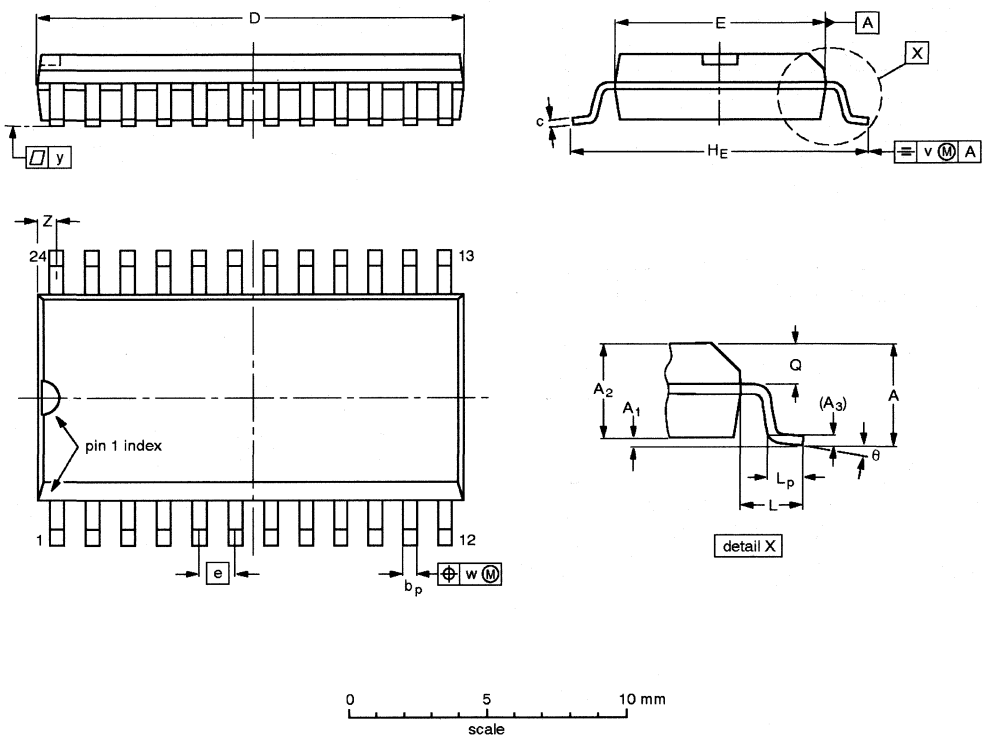
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

Package outlines

SO24: plastic small outline package; 24 leads; body width 7.5 mm — SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

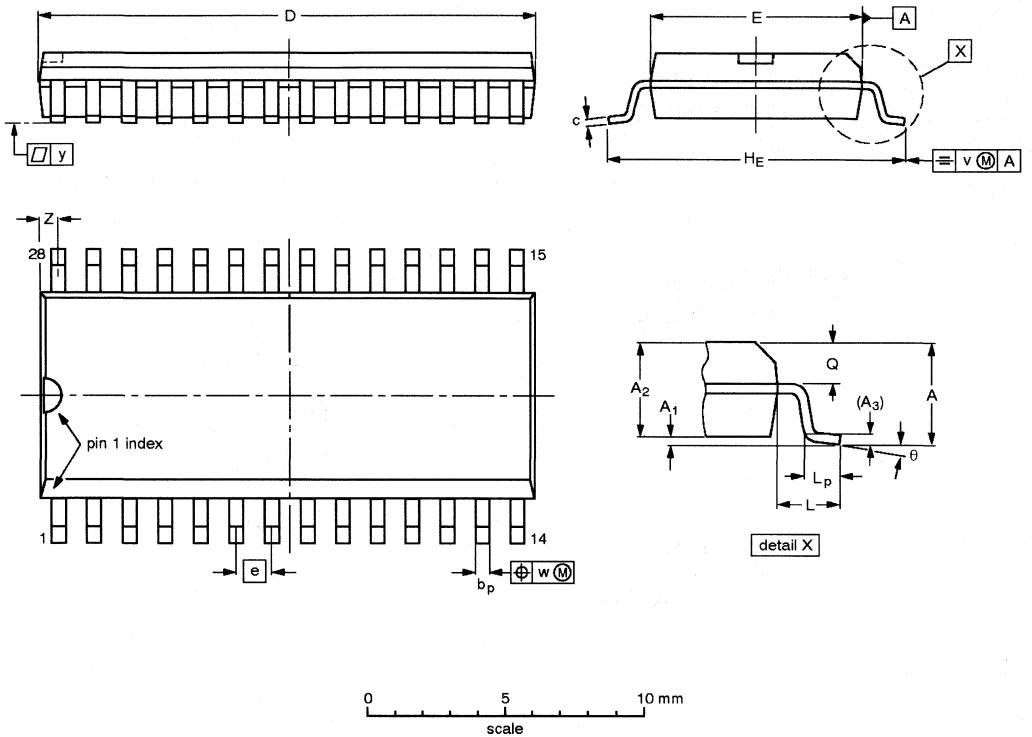
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

Package outlines

SO28: plastic small outline package; 28 leads; body width 7.5mm — SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

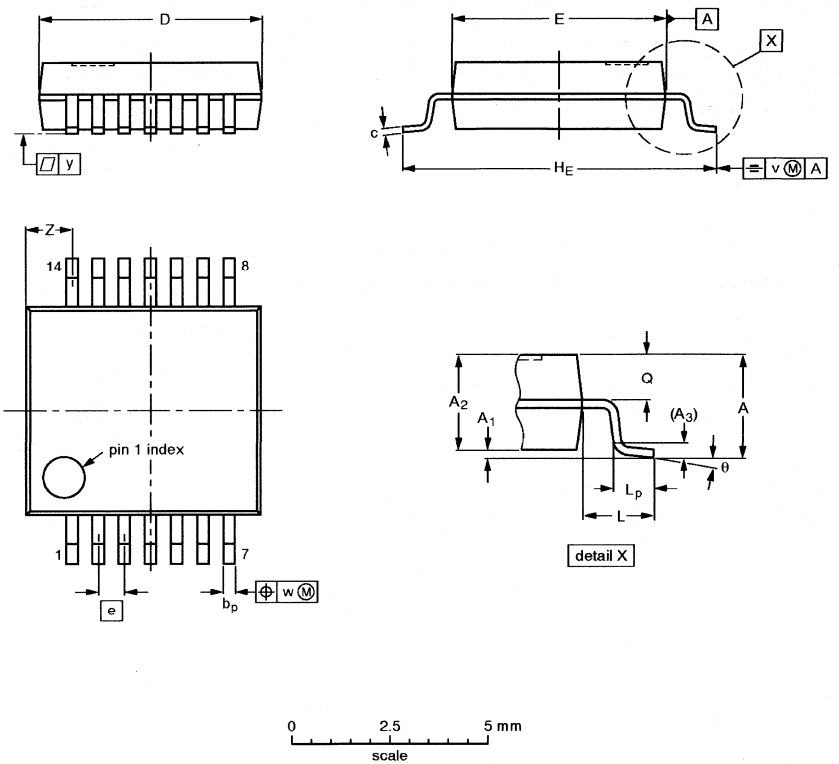
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

Package outlines

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm — SOT337-1



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

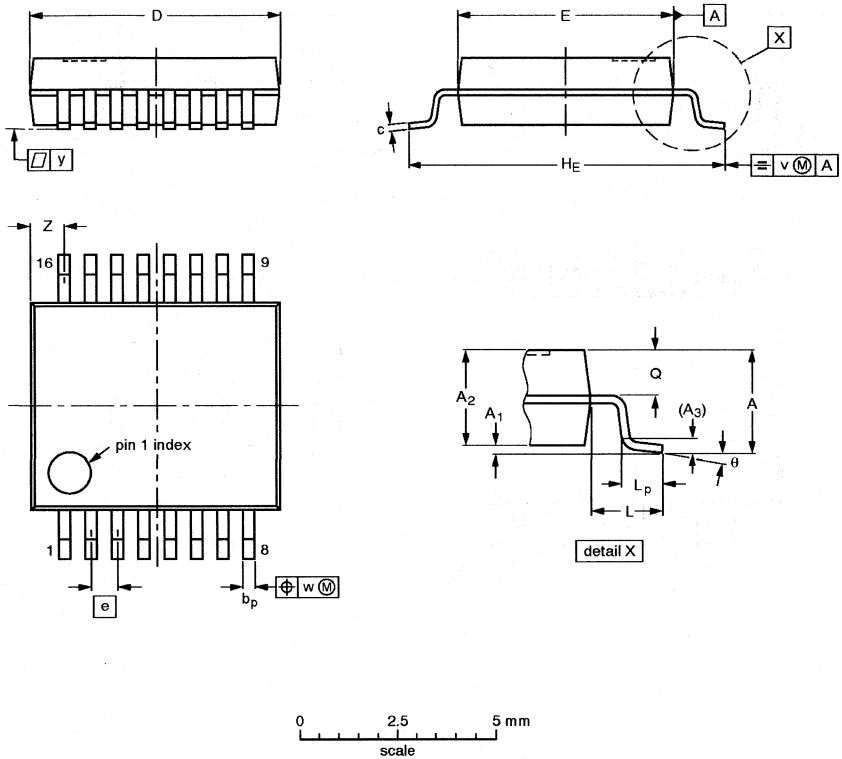
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~95-02-04~~ 96-01-18

Package outlines

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm — SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

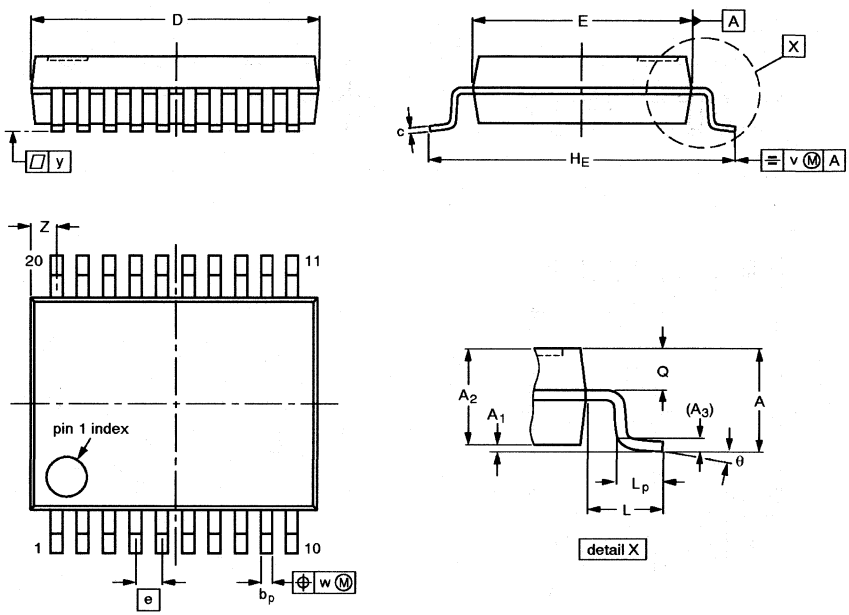
Note

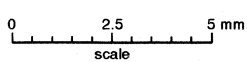
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

Package outlines

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm — SOT339-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

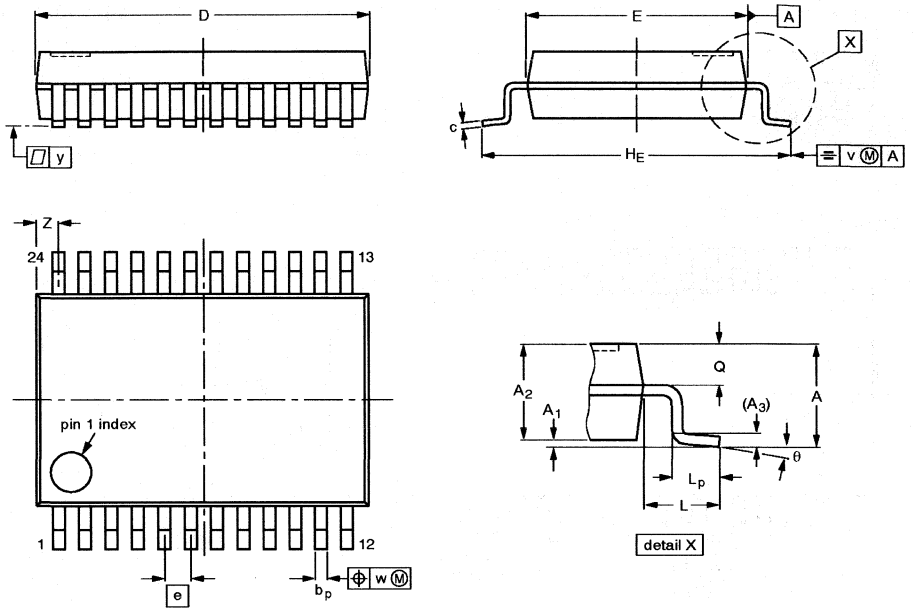
Note

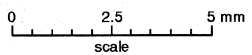
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

Package outlines

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm — SOT340-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

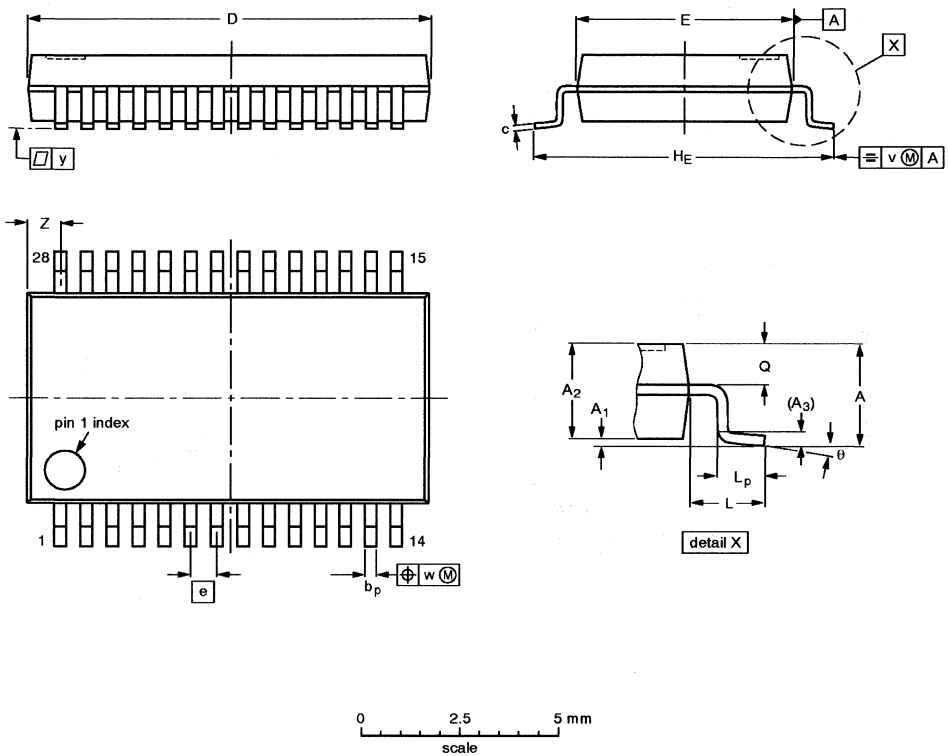
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

Package outlines

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3mm — SOT341-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

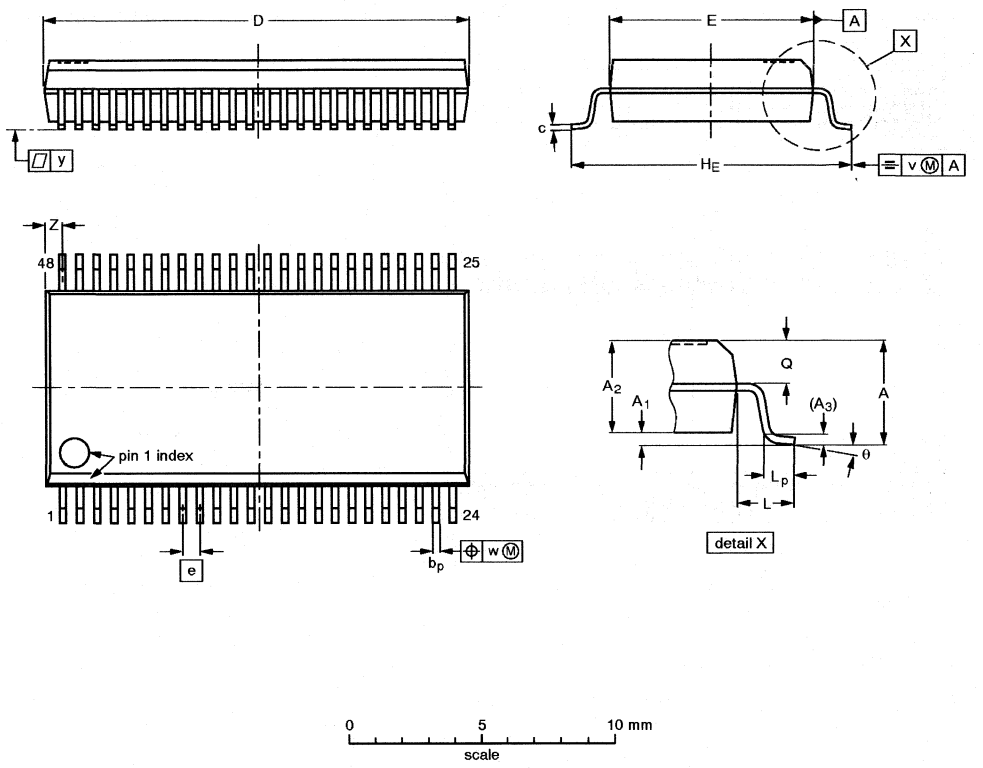
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

Package outlines

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm — SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

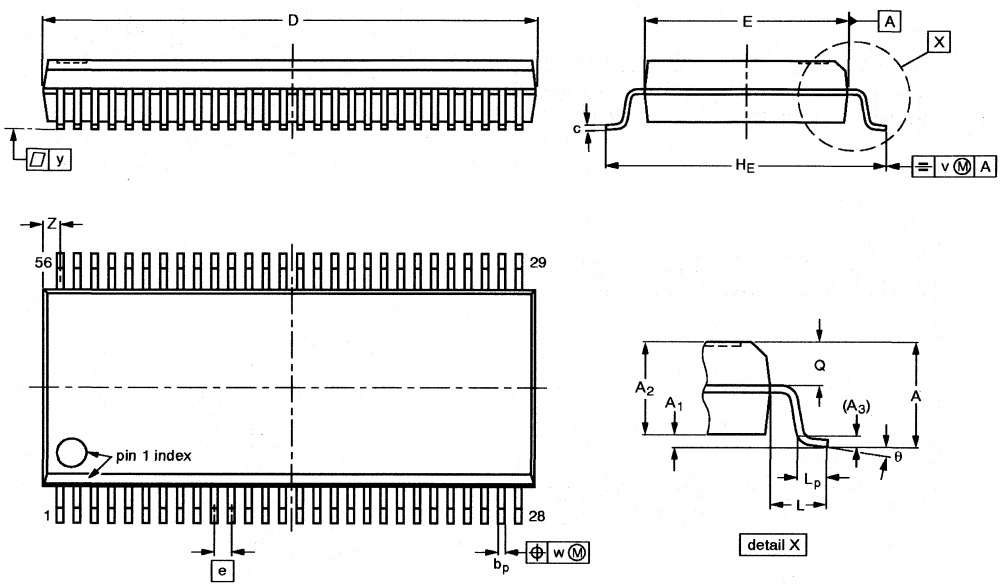
Note

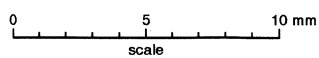
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

Package outlines

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm — SOT371-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

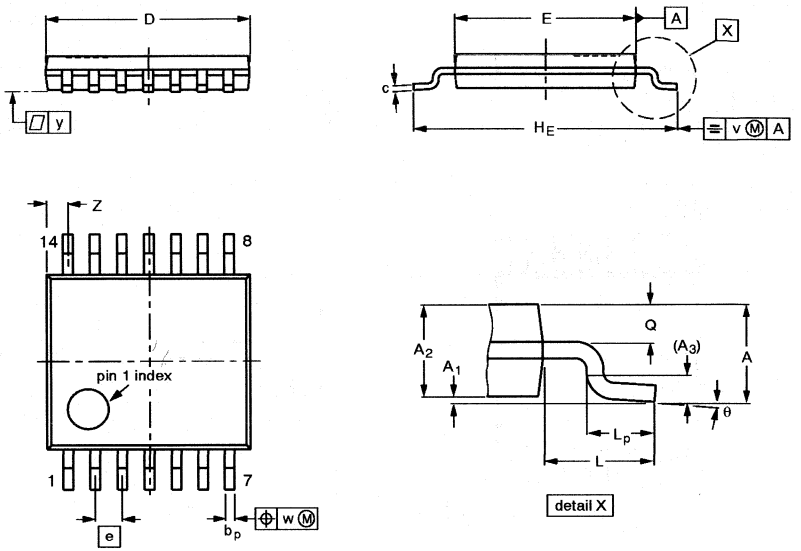
Note

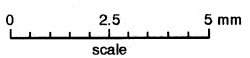
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

Package outlines

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm — SOT402-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

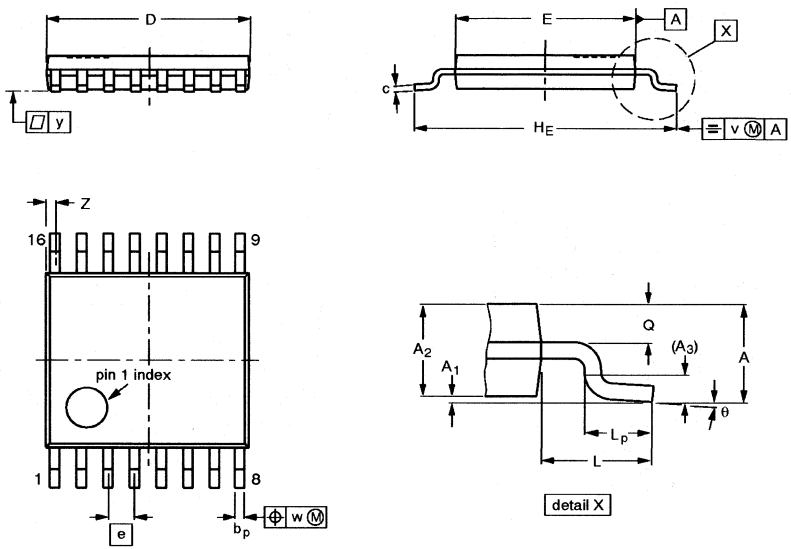
Notes

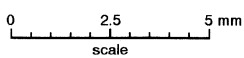
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~94-07-12~~ 95-04-04

Package outlines

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm — SOT403-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

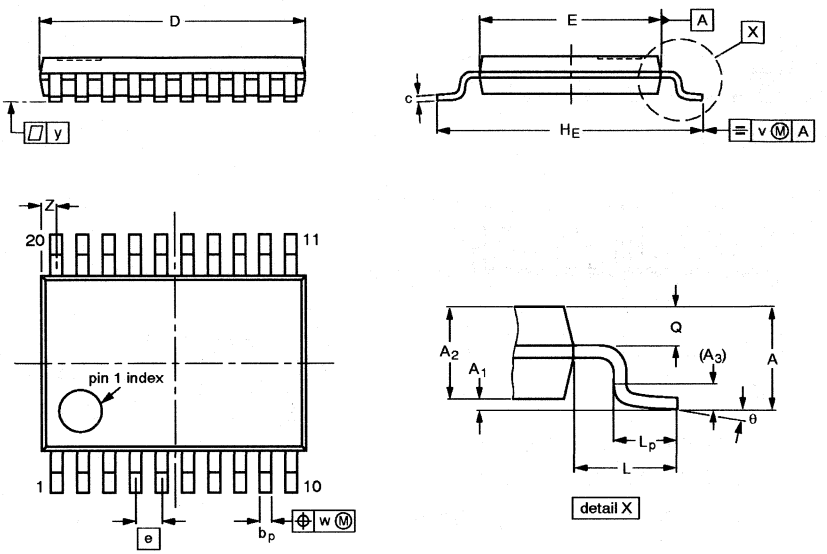
Notes

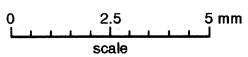
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

Package outlines

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm — SOT360-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

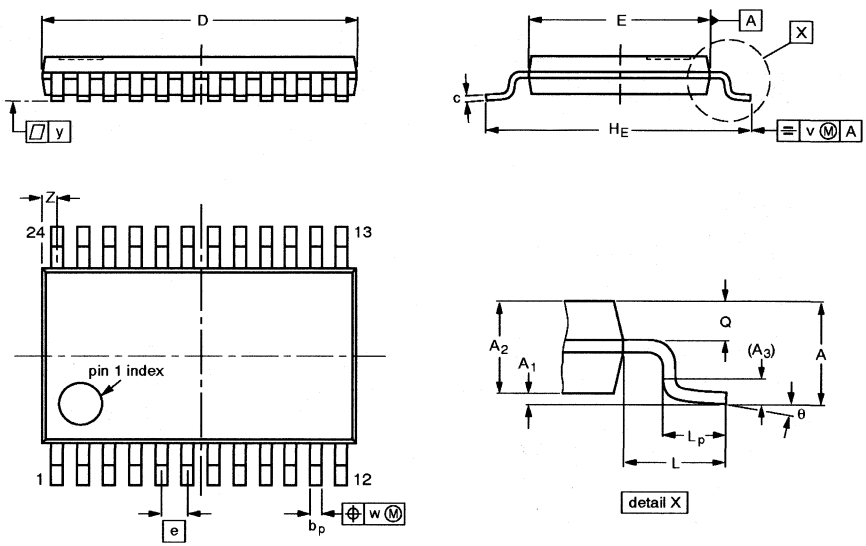
Notes

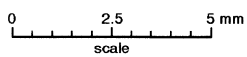
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

Package outlines

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm — SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

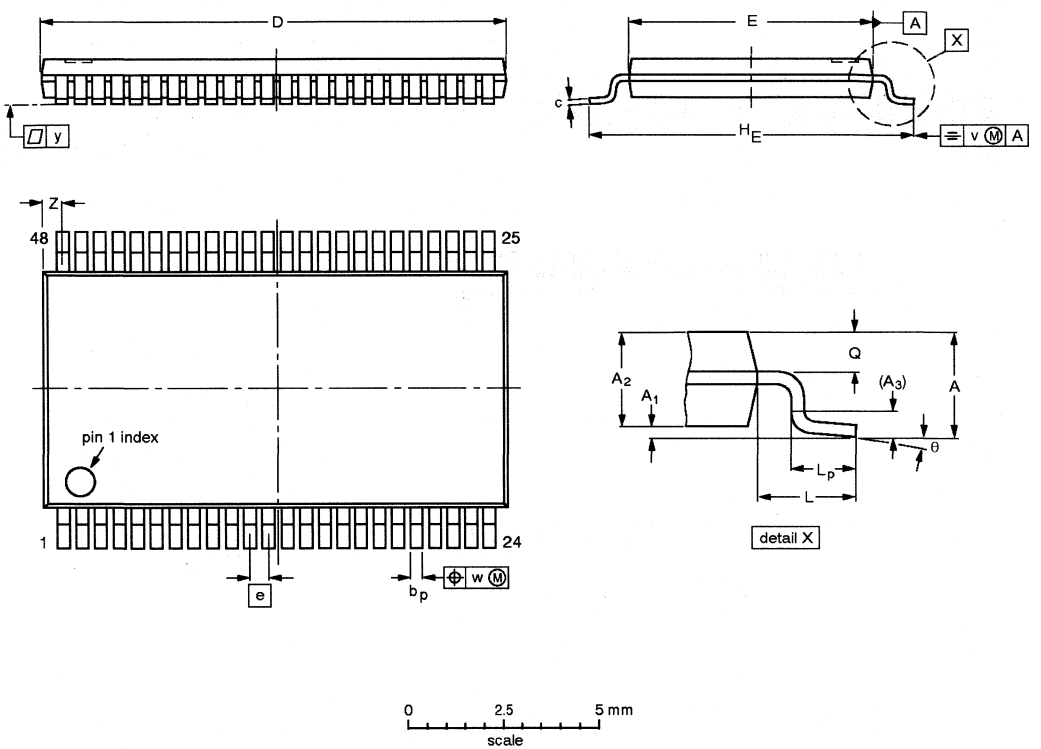
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

Package outlines

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

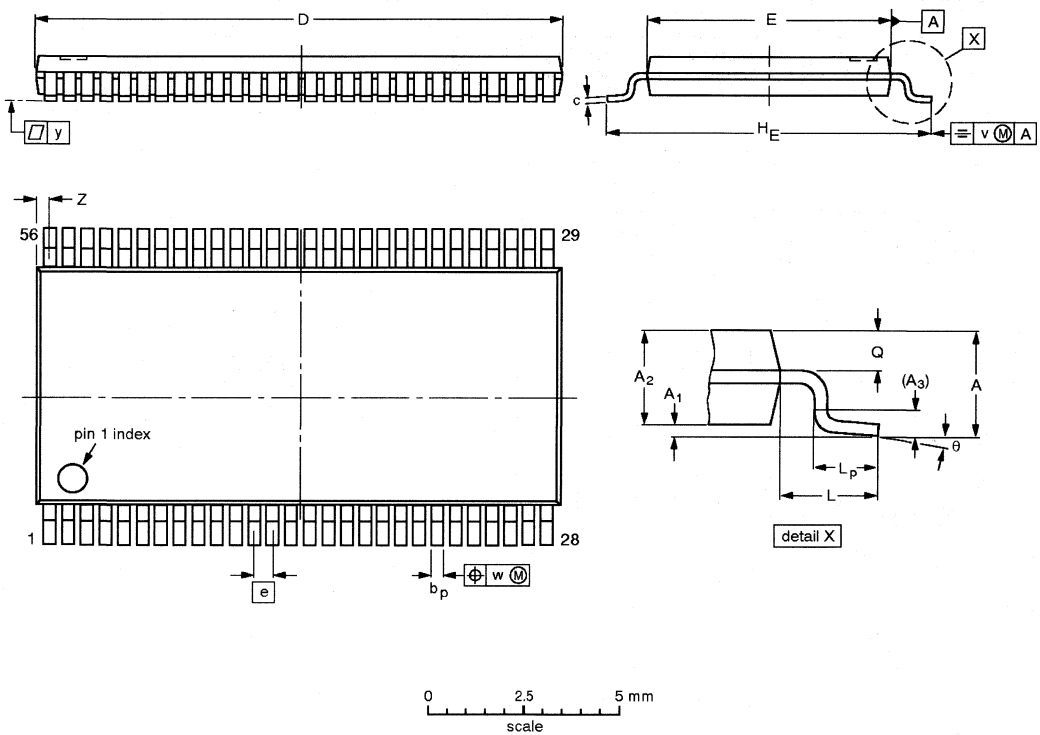
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					~~93-02-03~~ 95-02-10

Package outlines

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm — SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

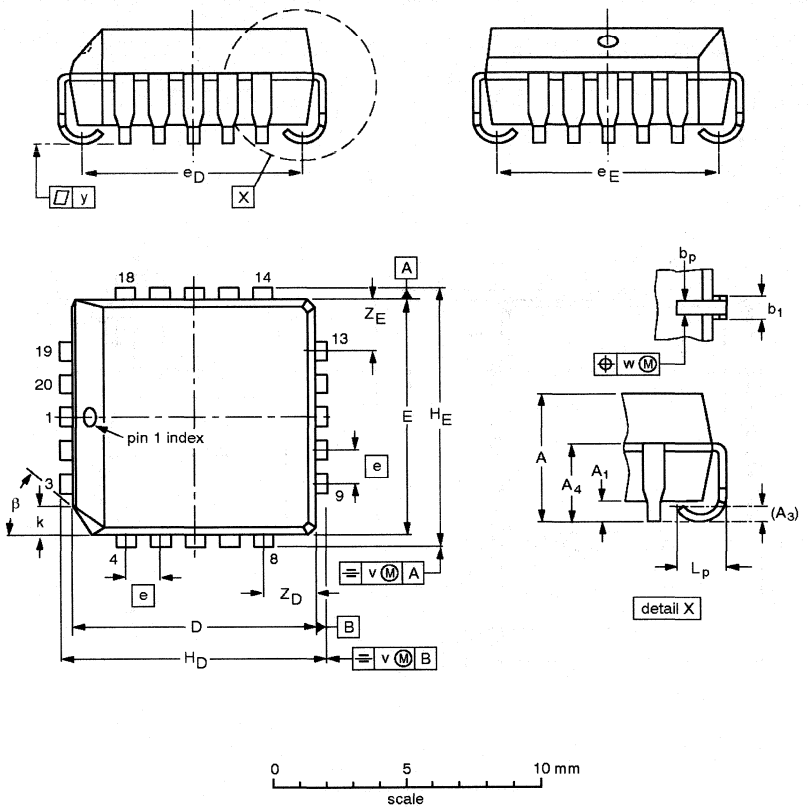
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153EE					~~93-02-03~~ 95-02-10

Package outlines

PLCC20: plastic leaded chip carrier; 20 leads — SOT380-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	9.04 8.89	9.04 8.89	1.27	8.38 7.37	8.38 7.37	10.03 9.78	10.03 9.78	1.22 1.07	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.356 0.350	0.356 0.350	0.05	0.330 0.290	0.330 0.290	0.395 0.385	0.395 0.385	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

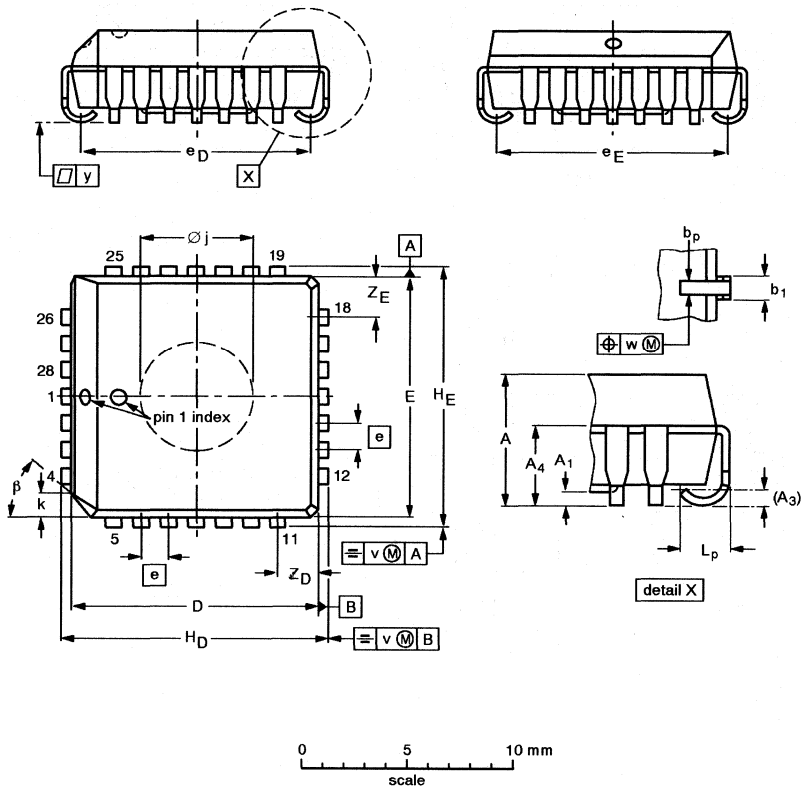
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT380-1		MO-047AA				~~95-02-25~~ 97-12-16

Package outlines

PLCC28: plastic leaded chip carrier; 28 leads; pedestal — SOT261-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	Øj	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-3		MO-047AB				~~95-02-25~~ 97-12-16

APPENDIX A

DATA HANDBOOK SYSTEM

Data handbook system

Appendix A

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

Our data handbook titles are listed here.

Integrated Circuits

Book	*Title*
IC01	Semiconductors for Radio, Audio and CD/DVD Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Wired Telecom Systems
IC04	HE4000B Logic Family CMOS
IC05	Advanced Low-power Schottky (ALS) Logic
IC06	High-speed CMOS Logic Family
IC11	General-purpose/Linear ICs
IC12	I^2C Peripherals
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	CMOS ICs for Clocks, Watches and Real Time Clocks
IC17	Semiconductors for Wireless Communications
IC18	Semiconductors for In-Car Electronics
IC19	ICs for Data Communications
IC20	80C51-based 8-bit Microcontrollers
IC22	Multimedia ICs
IC23	BiCMOS Bus Interface Logic
IC24	Low Voltage CMOS & BiCMOS Logic
IC25	16-bit 80C51XA Microcontrollers (eXtended Architecture)
IC26	Integrated Circuit Packages
IC27	Complex Programmable Logic Devices

Discrete Semiconductors

Book	*Title*
SC01	Small-signal and Medium-power Diodes
SC02	Power Diodes
SC03	Power Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Video Transistors and Modules for Monitors
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC13	Power MOS Transistors
SC14	RF Wideband Transistors
SC16	Wideband Hybrid Amplifier Modules for CATV
SC17	Semiconductor Sensors
SC18	Discrete Semiconductor Packages
SC19	RF & Microwave Power Transistors, RF Power Modules and Circulators/Isolators

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For more information about Philips Semiconductors data handbooks, catalogs and subscriptions, contact your nearest Philips Semiconductors national organization, select from the **address list on the back cover of this handbook.** Product specialists are at your service and inquiries are answered promptly.

OVERVIEW OF PHILIPS COMPONENTS DATA HANDBOOKS

Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

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Book	*Title*
DC01	Colour Television Tubes
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC04	Colour Monitor and Multimedia Tubes
DC05	Wire Wound Components

Magnetic Products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites
MA04	Dry-reed Switches

Passive Components

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
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PA06b	Leaded Ceramic Capacitors
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PA11	Quartz Oscillators

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